DATA ACQUISITION IC HANDBOOK

TSC911
TSC826
TSC805
TSC7106

TELEDYNE SEMICONDUCTOR

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DATA ACQUISITION IC HANDBOOK

1300 Terra Bella Avenue • P.O. Box 7267 • Mountain View, California USA 94039-7267 • Tel: 415/968-9241

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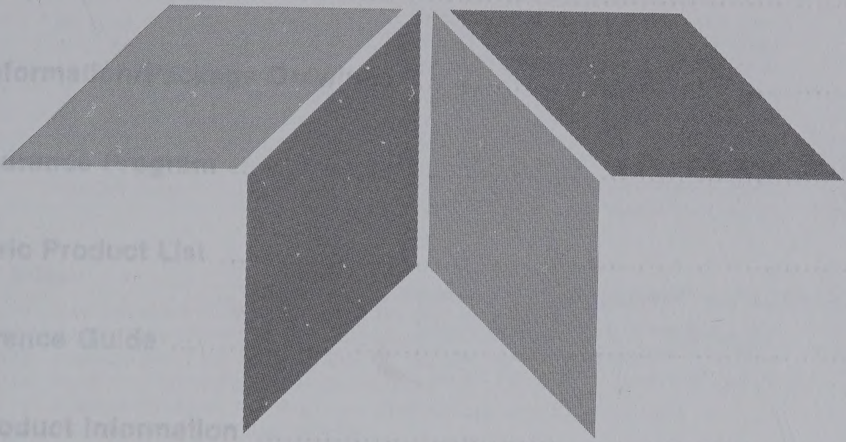

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SECTION 2

Ordering Information
Package Information

The Device Identification Codes for Device Numbers of TSC8700, TSC9400 and TSC14433 Family are as Follows:

PACKAGED DEVICES **TSC XXXXX X X X X**

1. **TELEDYNE SEMICONDUCTOR DEVICE**
2. **DEVICE NUMBER**
3. **ELECTRICAL GRADE (if applicable)**
4. **R — REVERSE LEAD CONFIGURATION (if applicable)**
5. **OPERATING TEMPERATURE RANGE**
   - C — Commercial Temperature Range (0 to 70°C)
   - E — Extended Temperature Range (—40 to +85°C)
   - B — Military Temperature Range (—55 to +125°C)
6. **PACKAGE TYPE**
   - J — Plastic Package
   - N — Ceramic Package
   - L — CerDIP
   - Y — Dice
   - E — Metal Can (TO—99)
   - M — Metal Can (TO—18)

EXAMPLE: TSC8701CL Operates Over the Commercial Temperature Range and is a CerDIP Package

PRODUCT STATUS

Three Classes of Data Sheets are Shown in this Data Book. These are Identified by the Presence or Absence of a "Banner" on the First Page.

DATA SHEET INDENTIFICATION	PRODUCT STATUS	COMMENTS
No Identification	Production	Delivery Subject to Product Demand.
Preliminary	Initial Production	Data Sheet Electrical Limits Established. Limited Production Quantities Available. Samples Available.
Advance Product Information	In Design	Data Sheet Gives Design Goal, Electrical Specifications and Major Product Features. Contact Teledyne Marketing for Samples and Information.

Note: Teledyne Semiconductor Reserves the Right to Make Changes at Any Time Without Notice in Order to Improve Performance and Supply.

All Other CMOS ICs
Ordering Information (Except 87XX/94XX/14433 Products)

The Device Identification Codes for All Other CMOS Products and All Products in 60-Pin Flat Packages are as Follows:

PACKAGED DEVICES **TSC XXXXXX X X X X / XXX**

1. TELEDYNE SEMICONDUCTOR DEVICE

2. DEVICE NUMBER

3. ELECTRICAL PERFORMANCE GRADE OPTION (if applicable)
R – Reversed Pin Layout

4. OPERATING TEMPERATURE RANGE
M – Military Temperature Range (–55°C to +125°C)
I* – Industrial Temperature Range (–25°C to +85°C)
C – Commercial Temperature Range (0°C to +70°C)
* – May Be –40°C to +85°C. Refer to Specific Device Specification

5. PACKAGE TYPE
J – CerDIP Dual-In-Line (non side brazed)
P – Plastic Dual-In-Line
T – TO–99 Type (round metal can)
B – Plastic Flat Package (formed leads)
S – Plastic Flat Package (unformed (straight) leads)
O – Plastic "SO" Surface Mount
L – Plastic Leaded Chip Carrier (PLCC)

6. NUMBER OF PACKAGE PINS
A – 8
D – 14
E – 16
F – 22
N – 18
G – 24
I – 28
L – 40
Y – 8 (pin 4 connected to case)
Q – 60
W – 44
S – 68

7. PROCESSING OPTION
883 – MIL-STD-883B, Class B Processing *
BI – 100% Burn-In at 125°C for 160 Hours

*Contact Teledyne Semiconductor Marketing for MIL–STD 883C status.

PACKAGED DEVICES TSC XXX X X

1. TELEDYNE SEMICONDUCTOR DEVICE
2. DEVICE NUMBER
3. ELECTRICAL GRADE AND TEMPERATURE RANGE
   - A — Industrial Temperature Range, 15 V, (−30 to +70°C)
   - B — Military Temperature Range, 12 V, (−55 to +125°C)
   - C — Industrial Temperature Range, 12 V, (−30 to +85°C)
   - M — Military Temperature Range, 15 V, (−55 to +125°C)
4. PACKAGE TYPE
   - G — Metal Can (TO−8)
   - H — Flatpack
   - J — Plastic Package
   - L — Ceramic Package (CerDIP)
   - Y — Dice

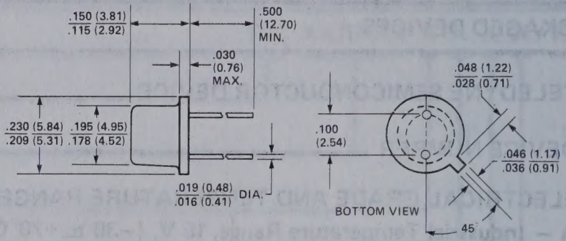
EXAMPLE: 303AL Operates Over an Industrial Temperature Range at 15 V and is a CerDIP Package

Product List — Digital Logic

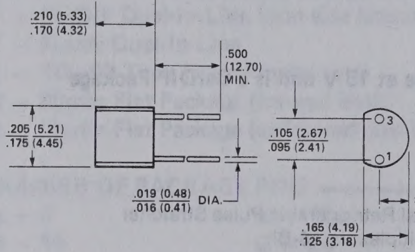
301	Power NAND Gates Dual 5-Input
302	Power NAND Gates Quad 2-Input
303	Power NAND Gates Quad 2-Input
304	Power NAND Gates Triple 4, 3, 4-Input
306	NOR Gate Quad 2, 2, 3, 3-Input
307	NOR Gate Quad 2, 2, 3, 3-Input
311	Flip Flops Master/Slave RST
312	Flip Flops Dual J-K Edge Triggered
313	Flip Flops Dual J-K Master/Slave
321	NAND Gates Quad 2-Input
322	NAND Gates Dual 5-Input
323	NAND Gates Quad 2-Input
324	NAND Gates Quad 2-Input
325	NAND Gates 2, 2, 3, 3-Input
326	NAND Gates 2, 2, 3, 3-Input
331	Gate Expander Dual 5-Input
332	Hex Inverter Gates 4-Inverter, 2-NAND
333	Hex Inverter Gates 4-Inverter, 2-NAND
334	Hex Inverter Gates Strobed Hex NAND
335	Hex Inverter Gates Strobed Hex NAND
341	Multifunction Gates Dual 2-Wide, 2-Input and/or Invert
342	Dual Monostable Multivibrator
343	Digital Comparator 4-Bit
344	Multifunction Gates Dual Expandable AND-NOR
347	Dual Retriggerable Monostable Multivibrator
349	Dual Retriggerable Pulse Stretcher
350	Multiplexers 8-Bit
351	Multiplexers Dual 4-Bit
355	Timer
361	Dual 11-16V to 5V Interface Voltage Translator
362	5V to 11-16V Interface Dual Translator
363	5V to 11-16V Interface Quad 2-Input NAND
367	Schmitt Trigger Quad(Active Pullup)
368	Schmitt Trigger Quad(Open Collector)
370	Flip Flop Quad D
371	Counters Decade
372	Counters Hexadecimal
373	Up-Down Counters Decade
374	Up-Down Counters Hexadecimal
375	Shift Register 4-Bit
380	BCD-to-Decade Decoder/Drivers Lamp Driver
381	BCD-to-Decade Decoder/Drivers Logic Driver
382	BCD-to-Decade Decoder/Drivers Gas Tube Driver
383	Decoder/Driver BCD-to-7 Segment
390	Dual Interface Buffers 4-Input Expandable AND
391	Dual Interface Buffers 2-Input AND
392	Dual Interface Buffers 2-Input NAND
393	Dual Interface Buffers 2-Input OR
394	Dual Interface Buffers 2-Input NOR
395	Dual Interface Buffers 4-Input Expandable NAND
396	Line Driver/Receiver Dual Differential

Package Information

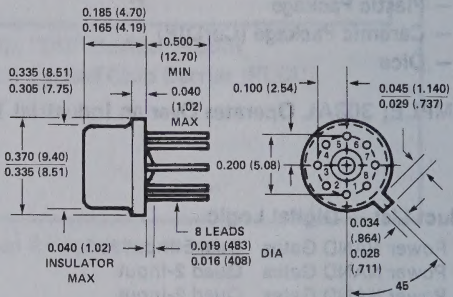
(Package #1)
TO-18 (2-Pin)


.150 (3.81)
.115 (2.92)
.500
(12.70)
MIN.
.030
(0.76)
MAX.
.048 (1.22)
.028 (0.71)
.230 (5.84)
.209 (5.31)
.195 (4.95)
.178 (4.52)
.100
(2.54)
.046 (1.17)
.036 (0.91)
.019 (0.48)
.016 (0.41)
DIA.
BOTTOM VIEW
45°

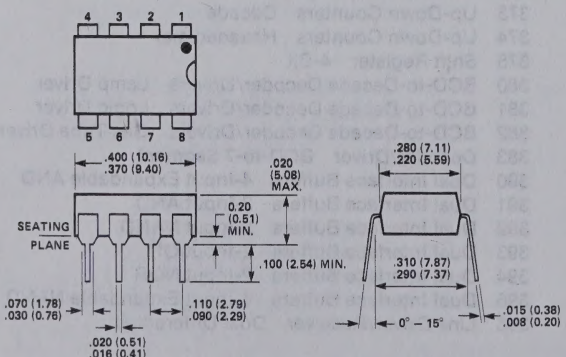
(Package #2)
TO-92 (2-Pin)


.210 (5.33)
.170 (4.32)
.500
(12.70)
MIN.
.205 (5.21)
.175 (4.45)
.105 (2.67)
.095 (2.41)
3
1
.019 (0.48)
.016 (0.41)
DIA.
.105 (2.67)
.080 (2.03)
.165 (4.19)
.125 (3.18)

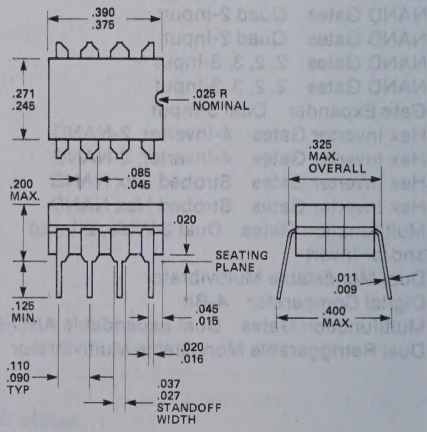
(Package #3)
TO-99 (8-Pin)


0.185 (4.70)
0.165 (4.19)
0.500
(12.70)
MIN
0.335 (8.51)
0.305 (7.75)
0.040
(1.02)
MAX
0.100 (2.54)
0.045 (1.140)
0.029 (.737)
0.370 (9.40)
0.335 (8.51)
0.200 (5.08)
1
2
3
4
5
6
7
8
8 LEADS
0.019 (483)
0.016 (408)
DIA
0.040 (1.02)
INSULATOR
MAX
0.034
(.864)
0.028
(.711)
45°

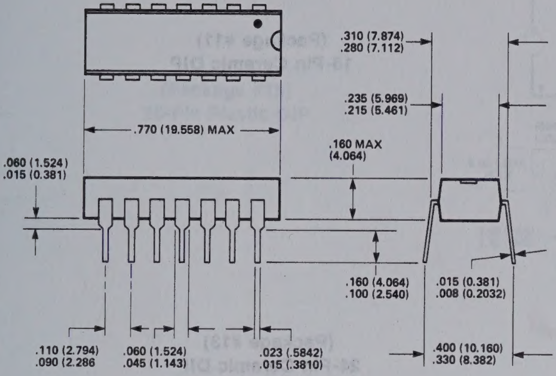
(Package #4)
8-Pin Plastic DIP


4
3
2
1
5
6
7
8
.400 (10.16)
.370 (9.40)
.020
(5.08)
MAX.
.280 (7.11)
.220 (5.59)
SEATING
PLANE
0.20
(0.51)
MIN.
.100 (2.54) MIN.
.310 (7.87)
.290 (7.37)
.070 (1.78)
.030 (0.76)
.110 (2.79)
.090 (2.29)
0° – 15°
.015 (0.38)
.008 (0.20)
.020 (0.51)
.016 (0.41)

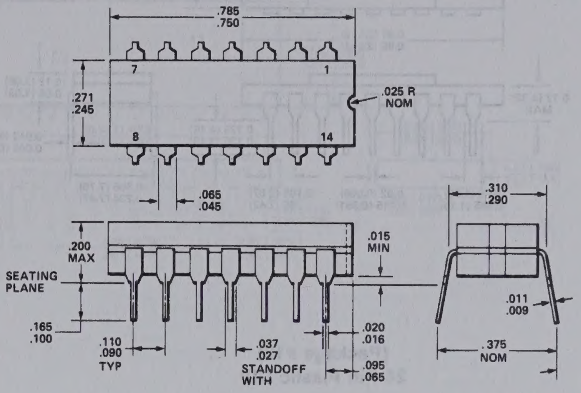
(Package #5)
8-Pin CerDIP


.390
.375
.271
.245
.025 R
NOMINAL
.325
MAX.
OVERALL
.065
.045
.200
MAX.
.020
SEATING
PLANE
.011
.009
.125
MIN.
.045
.015
.400
MAX.
.020
.016
.110
.090
TYP
.037
.027
STANDOFF
WIDTH

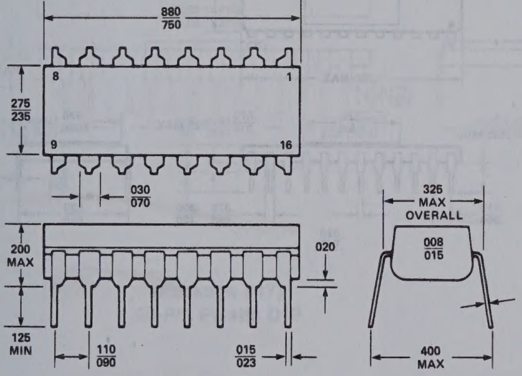
(Package #6)
14-Pin Plastic DIP


.310 (7.874)
.280 (7.112)
.235 (5.969)
.215 (5.461)
.770 (19.558) MAX
.160 MAX
(4.064)
.060 (1.524)
.015 (0.381)
.160 (4.064)
.100 (2.540)
.015 (0.381)
.008 (0.2032)
.110 (2.794)
.090 (2.286)
.060 (1.524)
.045 (1.143)
.023 (.5842)
.015 (.3810)
.400 (10.160)
.330 (8.382)

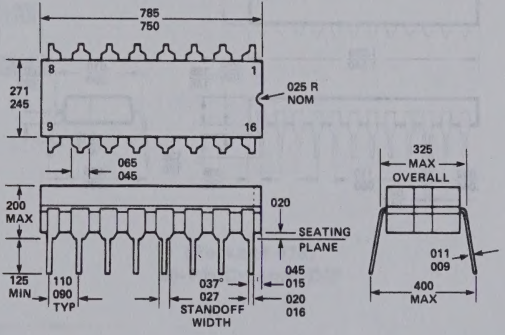
(Package #7)
14-Pin CerDIP

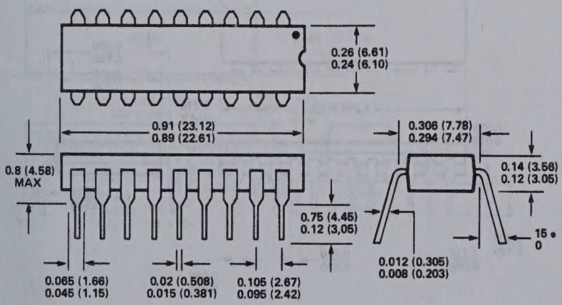

.785
.750
7
1
.271
.245
.025 R
NOM
8
14
.065
.045
.310
.290
.200
MAX
.015
MIN
SEATING
PLANE
.011
.009
.165
.100
.110
.090
TYP
.037
.027
STANDOFF
WITH
.020
.016
.095
.065
.375
NOM

(Package #8)
16-Pin Plastic DIP

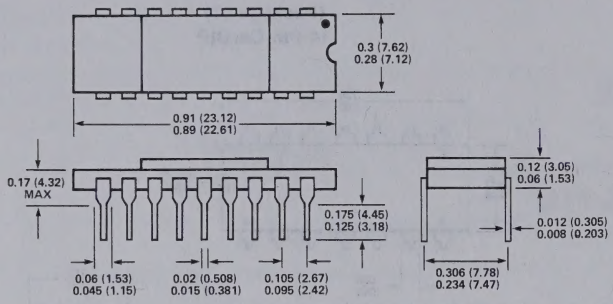

880
750
8
1
275
235
9
16
030
070
325
MAX
OVERALL
200
MAX
020
008
015
125
MIN
110
090
015
023
400
MAX

(Package #9)
16-Pin CerDIP


785
750
8
1
271
245
025 R
NOM
9
16
065
045
325
MAX
OVERALL
200
MAX
020
SEATING
PLANE
011
009
125
MIN
110
090
TYP
037°
027
STANDOFF
WIDTH
045
015
020
016
400
MAX

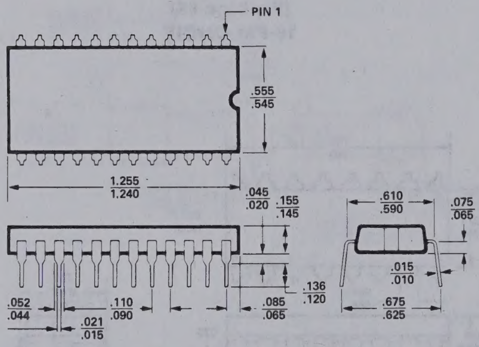

0.26 (6.61)
0.24 (6.10)
0.91 (23.12)
0.89 (22.61)
0.306 (7.78)
0.294 (7.47)
0.8 (4.58)
MAX
0.14 (3.56)
0.12 (3.05)
0.75 (4.45)
0.12 (3,05)
15 •
0
0.065 (1.66)
0.045 (1.15)
0.02 (0.508)
0.015 (0.381)
0.105 (2.67)
0.095 (2.42)
0.012 (0.305)
0.008 (0.203)

(Package #10)
18-Pin Plastic DIP

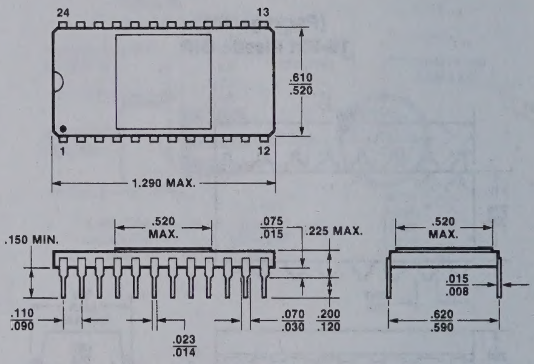

0.3 (7.62)
0.28 (7.12)
0.91 (23.12)
0.89 (22.61)
0.17 (4.32)
MAX
0.175 (4.45)
0.125 (3.18)
0.12 (3.05)
0.06 (1.53)
0.012 (0.305)
0.008 (0.203)
0.06 (1.53)
0.045 (1.15)
0.02 (0.508)
0.015 (0.381)
0.105 (2.67)
0.095 (2.42)
0.306 (7.78)
0.234 (7.47)

(Package #11)
18-Pin Ceramic DIP

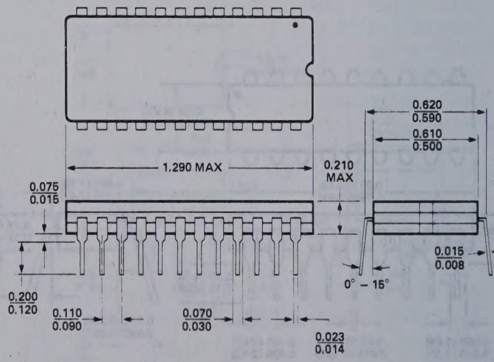
(Package #12)
24-Pin Plastic DIP


PIN 1
.555
.545
1.255
1.240
.045
.020
.155
.145
.610
.590
.075
.065
.015
.010
.136
.120
.052
.044
.110
.090
.021
.015
.085
.065
.675
.625

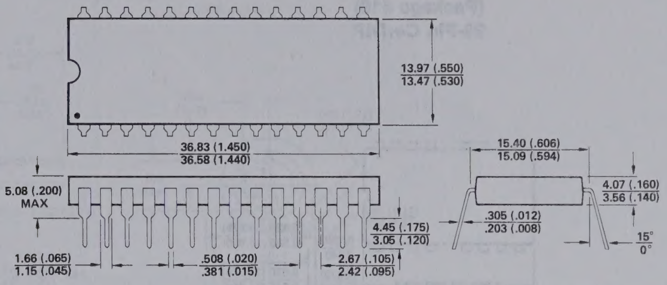
(Package #13)
24-Pin Ceramic DIP

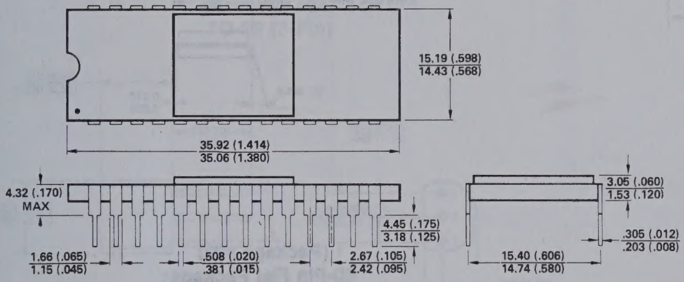

24
13
.610
.520
1
12
1.290 MAX.
.520
MAX.
.075
.015
.225 MAX.
.520
MAX.
.150 MIN.
.015
.008
.110
.090
.070
.030
.200
.120
.620
.590
.023
.014

(Package #14)
24-Pin CerDIP


0.620
0.590
0.610
0.500
1.290 MAX
0.210
MAX
0.075
0.015
0.015
0.008
0° – 15°
0.200
0.120
0.110
0.090
0.070
0.030
0.023
0.014

(Package #15)
28-Pin Plastic DIP

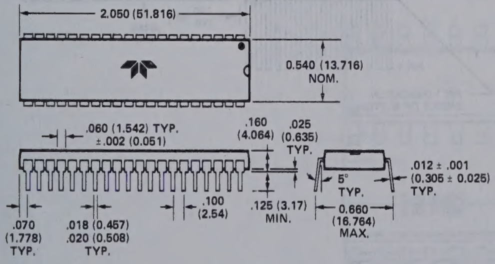

13.97 (.550)
13.47 (.530)
36.83 (1.450)
36.58 (1.440)
15.40 (.606)
15.09 (.594)
5.08 (.200)
MAX
4.07 (.160)
3.56 (.140)
.305 (.012)
.203 (.008)
4.45 (.175)
3.05 (.120)
15°
0°
1.66 (.065)
1.15 (.045)
.508 (.020)
.381 (.015)
2.67 (.105)
2.42 (.095)

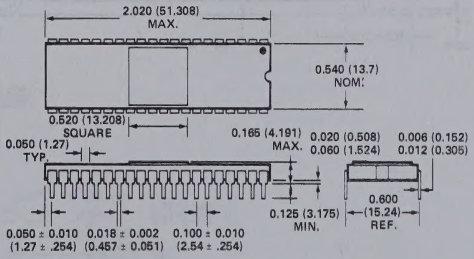

15.19 (.598)
14.43 (.568)
35.92 (1.414)
35.06 (1.380)
4.32 (.170)
MAX
3.05 (.060)
1.53 (.120)
4.45 (.175)
3.18 (.125)
.305 (.012)
.203 (.008)
1.66 (.065)
1.15 (.045)
.508 (.020)
.381 (.015)
2.67 (.105)
2.42 (.095)
15.40 (.606)
14.74 (.580)

(Package #16)
28-Pin Ceramic DIP

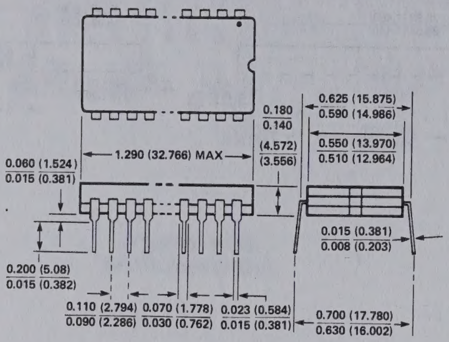
(Package #17)
40-Pin Plastic DIP

(Package #18)
40-Pin Ceramic DIP

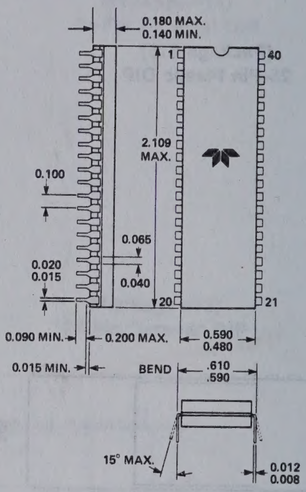

2.050 (51.816)
0.540 (13.716)
NOM.
.060 (1.542) TYP.
±.002 (0.051)
.160
(4.064)
.025
(0.635)
TYP.
5°
TYP.
.012 ± .001
(0.305 ± 0.025)
TYP.
.100
(2.54)
.125 (3.17)
MIN.
0.660
(16.764)
MAX.
.070
(1.778)
TYP.
.018 (0.457)
.020 (0.508)
TYP.


2.020 (51.308)
MAX.
0.540 (13.7)
NOM.
0.520 (13.208)
SQUARE
0.165 (4.191)
MAX.
0.020 (0.508)
0.060 (1.524)
0.006 (0.152)
0.012 (0.305)
0.050 (1.27)
TYP.
0.600
(15.24)
REF.
0.125 (3.175)
MIN.
0.050 ± 0.010
(1.27 ± .254)
0.018 ± 0.002
(0.457 ± 0.051)
0.100 ± 0.010
(2.54 ± .254)

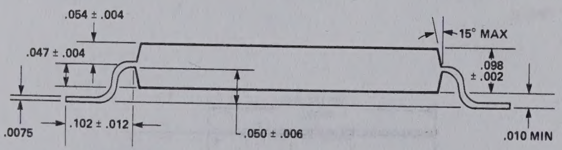
(Package #19)
28-Pin CerDIP


0.625 (15.875)
0.590 (14.986)
0.180
0.140
(4.572)
(3.556)
0.550 (13.970)
0.510 (12.964)
1.290 (32.766) MAX
0.060 (1.524)
0.015 (0.381)
0.015 (0.381)
0.008 (0.203)
0.200 (5.08)
0.015 (0.382)
0.110 (2.794)
0.090 (2.286)
0.070 (1.778)
0.030 (0.762)
0.023 (0.584)
0.015 (0.381)
0.700 (17.780)
0.630 (16.002)

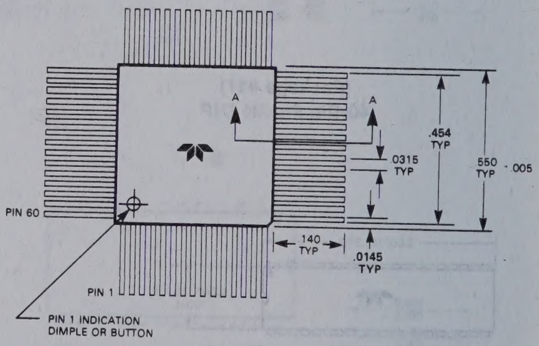
(Package #20)
40-Pin CerDIP


0.180 MAX.
0.140 MIN.
1
40
2.109
MAX.
0.100
0.065
0.020
0.015
0.040
20
21
0.090 MIN.
0.200 MAX.
0.590
0.480
0.015 MIN.
BEND
.610
.590
15° MAX.
0.012
0.008

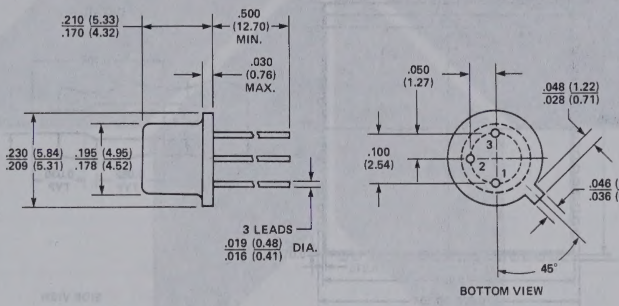
(Package #21)
60-Pin Flat Package
Formed Leads


.054 ± .004
.047 ± .004
15° MAX
.098
± .002
.0075
.102 ± .012
.050 ± .006
.010 MIN

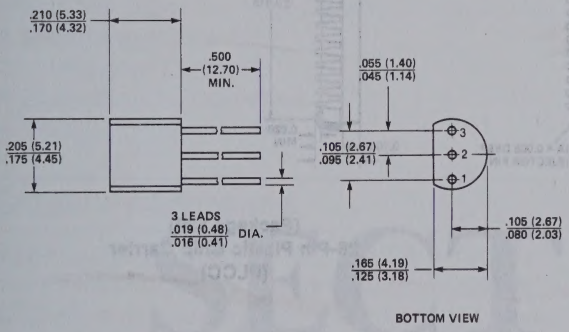
(Package #22)
60-Pin Flat Package
Unformed Leads


A
A
.454
TYP
.0315
TYP
.550
TYP
± .005
PIN 60
140
TYP
.0145
TYP
PIN 1
PIN 1 INDICATION
DIMPLE OR BUTTON

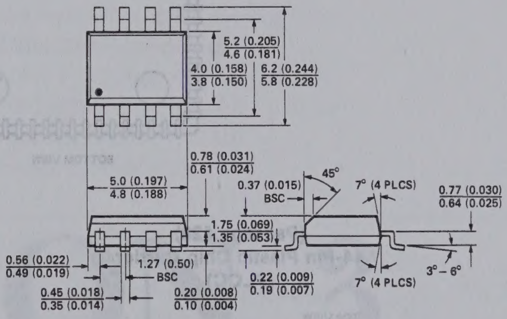
(Package #23)
TO-18 (3-Pin)


.210 (5.33)
.170 (4.32)
.500
(12.70)
MIN.
.030
(0.76)
MAX.
.050
(1.27)
.048 (1.22)
.028 (0.71)
.230 (5.84)
.209 (5.31)
.195 (4.95)
.178 (4.52)
.100
(2.54)
3
2
1
.046 (1.17)
.036 (0.91)
3 LEADS
.019 (0.48)
.016 (0.41)
DIA.
45°
BOTTOM VIEW

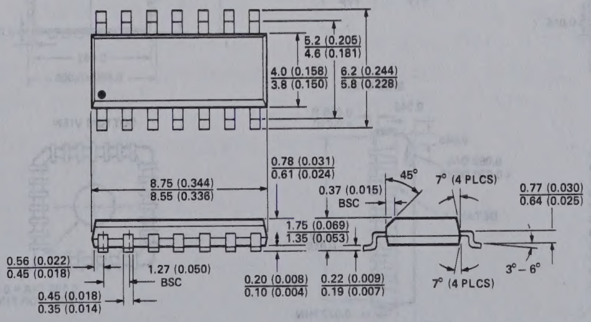
(Package #24)
TO-92 (3-Pin)


.210 (5.33)
.170 (4.32)
.500
(12.70)
MIN.
.055 (1.40)
.045 (1.14)
.205 (5.21)
.175 (4.45)
.105 (2.67)
.095 (2.41)
3
2
1
3 LEADS
.019 (0.48)
.016 (0.41)
DIA.
.105 (2.67)
.080 (2.03)
.165 (4.19)
.125 (3.18)
BOTTOM VIEW

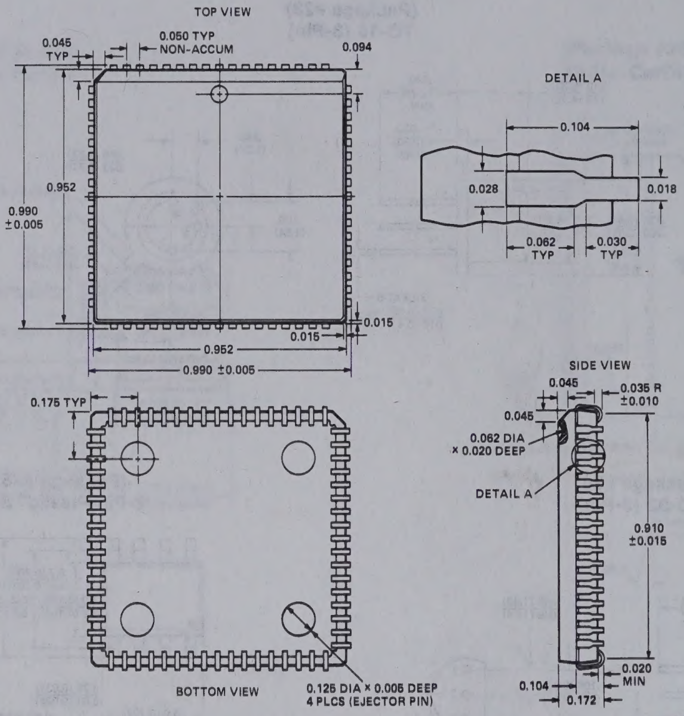
(Package #25)
8-Pin Plastic "SO"


5.2 (0.205)
4.6 (0.181)
4.0 (0.158)
3.8 (0.150)
6.2 (0.244)
5.8 (0.228)
0.78 (0.031)
0.61 (0.024)
5.0 (0.197)
4.8 (0.188)
0.37 (0.015)
BSC
45°
7° (4 PLCS)
0.77 (0.030)
0.64 (0.025)
1.75 (0.069)
1.35 (0.053)
0.56 (0.022)
0.49 (0.019)
1.27 (0.50)
BSC
0.22 (0.009)
0.19 (0.007)
7° (4 PLCS)
3° – 6°
0.45 (0.018)
0.35 (0.014)
0.20 (0.008)
0.10 (0.004)

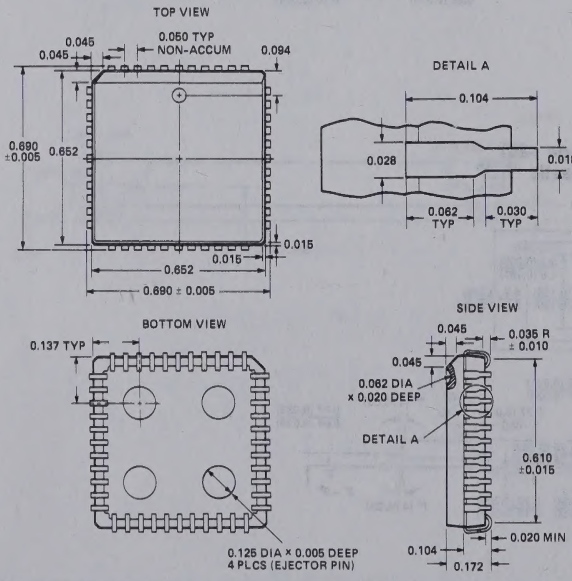
(Package #26)
14-Pin Plastic "SO"


5.2 (0.205)
4.6 (0.181)
4.0 (0.158)
3.8 (0.150)
6.2 (0.244)
5.8 (0.228)
0.78 (0.031)
0.61 (0.024)
8.75 (0.344)
8.55 (0.336)
45°
7° (4 PLCS)
0.37 (0.015)
BSC
0.77 (0.030)
0.64 (0.025)
1.75 (0.069)
1.35 (0.053)
0.56 (0.022)
0.45 (0.018)
1.27 (0.050)
BSC
0.20 (0.008)
0.10 (0.004)
0.22 (0.009)
0.19 (0.007)
3° – 6°
7° (4 PLCS)
0.45 (0.018)
0.35 (0.014)

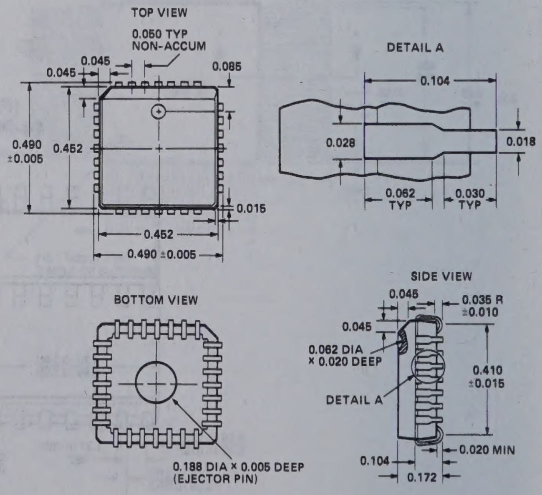
(Package #27)
68-Pin Plastic Chip Carrier (PLCC)


TOP VIEW
0.045 TYP
0.050 TYP NON-ACCUM
0.094
0.952
0.990 ±0.005
0.015
0.015
0.952
0.990 ±0.005
DETAIL A
0.104
0.028
0.018
0.062 TYP
0.030 TYP
0.175 TYP
BOTTOM VIEW
0.125 DIA × 0.005 DEEP 4 PLCS (EJECTOR PIN)
SIDE VIEW
0.045
0.035 R ±0.010
0.045
0.062 DIA × 0.020 DEEP
DETAIL A
0.910 ±0.015
0.020 MIN
0.104
0.172

(Package #28)
44-Pin Plastic Chip Carrier (PLCC)


TOP VIEW
0.045
0.045
0.050 TYP NON-ACCUM
0.094
0.690 ±0.005
0.652
0.015
0.015
0.652
0.690 ± 0.005
DETAIL A
0.104
0.028
0.018
0.062 TYP
0.030 TYP
BOTTOM VIEW
0.137 TYP
0.125 DIA × 0.005 DEEP 4 PLCS (EJECTOR PIN)
SIDE VIEW
0.045
0.035 R ± 0.010
0.045
0.062 DIA × 0.020 DEEP
DETAIL A
0.610 ±0.015
0.020 MIN
0.104
0.172

(Package #29)
28-Pin Plastic Chip Carrier (PLCC)


TOP VIEW
0.050 TYP NON-ACCUM
0.045
0.045
0.085
0.490 ±0.005
0.452
0.015
0.452
0.490 ±0.005
DETAIL A
0.104
0.028
0.018
0.062 TYP
0.030 TYP
BOTTOM VIEW
0.188 DIA × 0.005 DEEP (EJECTOR PIN)
SIDE VIEW
0.045
0.035 R ±0.010
0.045
0.062 DIA × 0.020 DEEP
DETAIL A
0.410 ±0.015
0.020 MIN
0.104
0.172

SECTION 3

Quality Assurance Program

Teledyne Semiconductor Product Assurance Program

Teledyne Semiconductor's Product Assurance Program is based on four major blocks:

- **Quality Control**
- **Quality Assurance**
- **Reliability**
- **Quality Circles**

Quality Control

The Quality Control function handles continuous monitoring of production, from incoming inspection of raw materials to wafer and assembly processing. This includes surveillance of documentation, calibration, and environmental processing.

The three major areas of Quality Control are:

- Incoming Inspection
- In-Process Control
- Operation Surveillance
- Vendor Qualification

Quality Assurance

After devices are subjected to 100% testing in manufacturing, they are formed into lots and submitted to Quality Assurance acceptance testing. Three types of tests are performed on samples: Visual/Mechanical, Parametric, and Functional. The sampling is based on a plan equivalent to a .07 AQL with a .5% AOQL. (All TSC sample plans are in accordance with MIL-M-38510 appendix B or MIL-HDB 105D.) Testing is done at room and elevated temperature. Lower temperature testing is performed when required by the specification, or when a potential problem is known to exist.

The Quality function at TSC is directed at providing a continually improving product that meets or exceeds the customer expectations. This stated goal is being achieved at Teledyne, which is evident in Figure 1 and Figure 2. These show constant improvement both in outgoing percent defective and customer return rate.

Reliability

The Reliability Group is responsible for the following functions:

- New Process Qualification
- Process Change Qualification
- Process Monitoring
- New Device Qualification
- Device Change Qualification
- Device Monitoring
- New Package Qualification
- Package Change Qualification
- Package Monitoring
- Failure Analysis

Quality Control Circles

Quality Control Circles are a vital part of the quality loop at Teledyne Semiconductor. The concept allows each employee directly involved in manufacturing to have a voice in how to build a quality product. Volunteers within a group meet weekly to determine and solve problems. Some solutions to problems may be implemented on the job. Others require management support, and to this end, circle members are trained in management presentation. The goal is total employee involvement with an emphasis on building-in quality.

Product Assurance Program

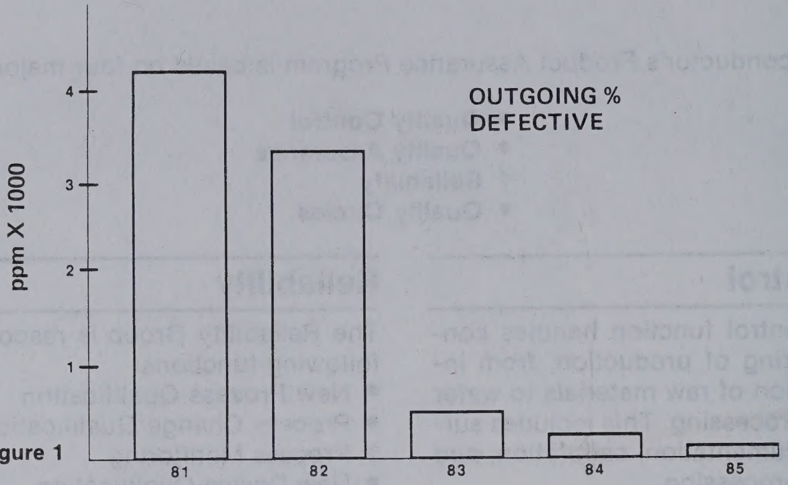


Figure 1

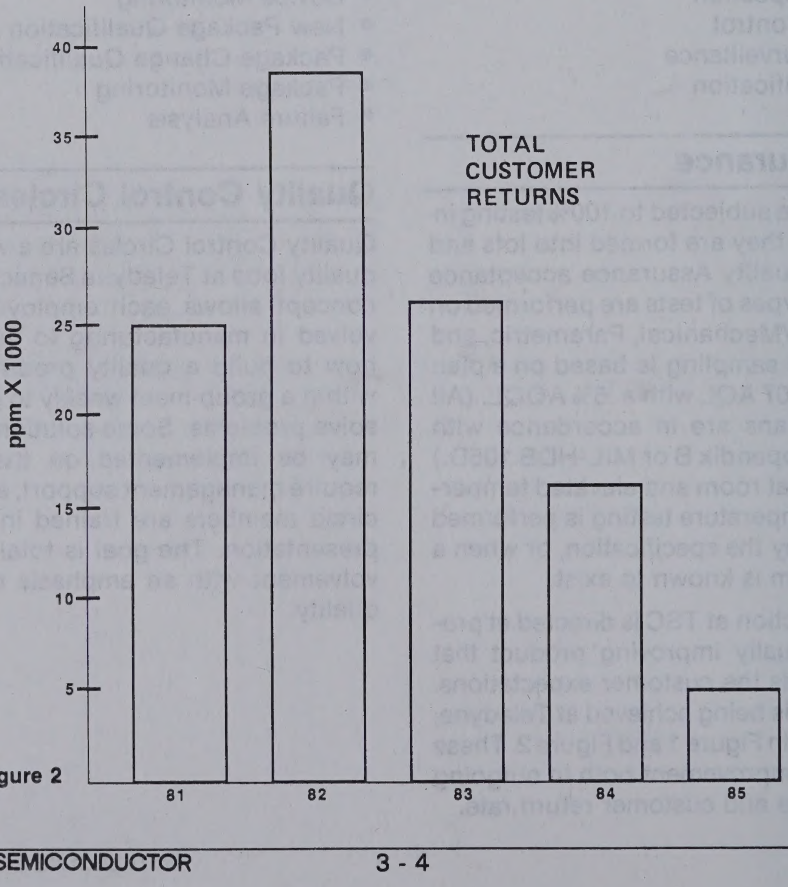
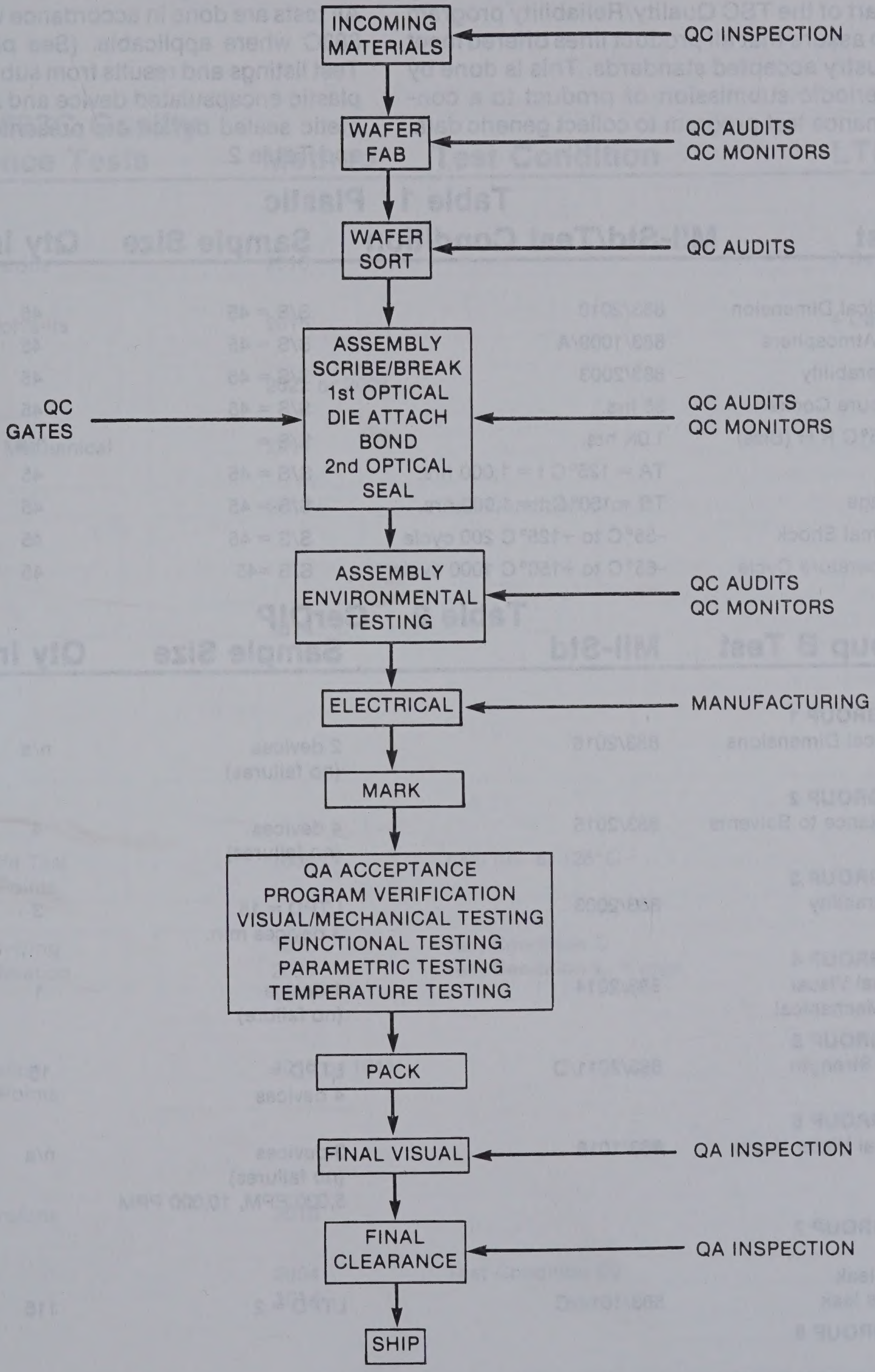


Figure 2

Product Assurance Program


INCOMING MATERIALS
QC INSPECTION
WAFER FAB
QC AUDITS
QC MONITORS
WAFER SORT
QC AUDITS
QC GATES
ASSEMBLY
SCRIBE/BREAK
1st OPTICAL
DIE ATTACH
BOND
2nd OPTICAL
SEAL
QC AUDITS
QC MONITORS
ASSEMBLY ENVIRONMENTAL TESTING
QC AUDITS
QC MONITORS
ELECTRICAL
MANUFACTURING
MARK
QA ACCEPTANCE
PROGRAM VERIFICATION
VISUAL/MECHANICAL TESTING
FUNCTIONAL TESTING
PARAMETRIC TESTING
TEMPERATURE TESTING
PACK
FINAL VISUAL
QA INSPECTION
FINAL CLEARANCE
QA INSPECTION
SHIP

Quality Conformance

A part of the TSC Quality/Reliability program is to assure that all product lines offered meet industry accepted standards. This is done by a periodic submission of product to a conformance test program to collect generic data. All tests are done in accordance with MIL-STD 883C where applicable. (See pages 3-7/3-8) Test listings and results from submissions for a plastic encapsulated device and a CerDIP hermetic sealed device are presented in Table 1 and Table 2.

Table 1 Plastic

Test	Mil-Std/Test Condition	Sample Size	Qty In	Qty Out
Physical Dimension	883/2010	S/S = 45	45	45
Salt Atmosphere	883/1009/A	S/S = 45	45	45
Solderability	883/2003	S/S = 45	45	45
Pressure Cooker	96 hrs.	S/S = 45	45	45
85/85° C R H (Bias)	1.0K hrs.	S/S =	n/a	n/a
SSL	TA = 125° C t = 1,000 hrs.	S/S = 45	45	45
Storage	TS = 150° C t = 1,000 hrs.	S/S = 45	45	45
Thermal Shock	-55° C to +125° C 200 cycle	S/S = 45	45	45
Temperature Cycle	-65° C to +150° C 1000 cycle	S/S =45	45	45

Table 2 CerDIP

Group B Test	Mil-Std	Sample Size	Qty In	Qty Out
SUBGROUP 1 Physical Dimensions	883/2016	2 devices (no failures)	n/a	n/a
SUBGROUP 2 Resistance to Solvents	883/2015	4 devices (no failures)	4	4
SUBGROUP 3 Solderability	883/2003	LTPD = 15 3 devices min.	3	3
SUBGROUP 4 Internal Visual And Mechanical	883/2014	1 device (no failure)	1	1
SUBGROUP 5 Bond Strength	883/2011/D	LTPD = 4 devices	15	15
SUBGROUP 6 Internal Water Vapor	883/1018	3 devices (no failures) 5,000 PPM, 10,000 PPM	n/a	n/a
SUBGROUP 7 Seal Fine leak Gross leak	883/1014/C	LTPD = 2	116	116
SUBGROUP 8 NA				

Conformance Flow

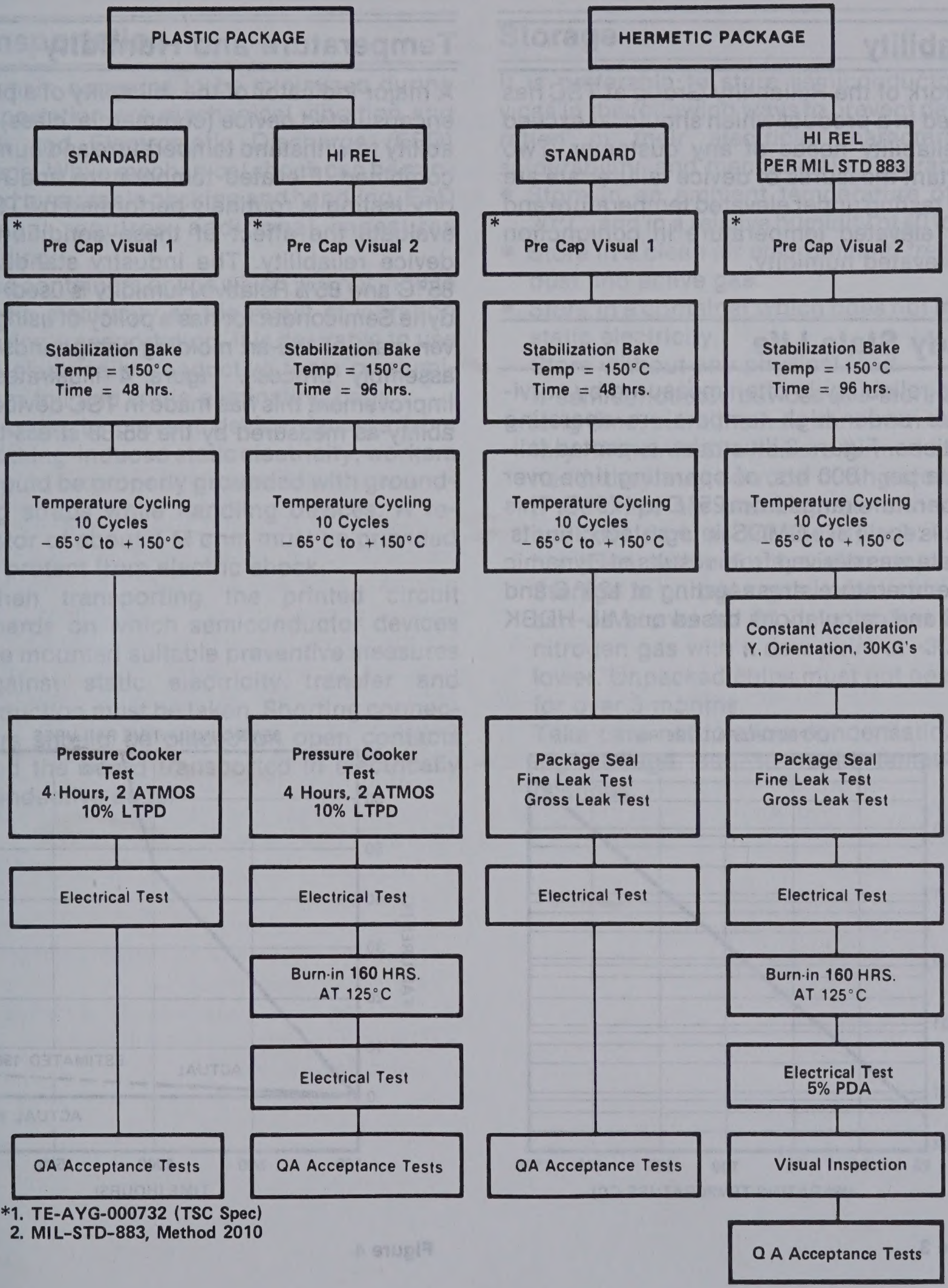
Generic Data is generated on a periodic basis for the following test.

MIL-STD-883C Quality Conformance Tests	Method	Test Condition	LTPD
GROUP B			
SUBGROUP 1			
Physical Dimensions	2016		2 Devices
SUBGROUP 2			
Resistance to Solvents	2015		4 Devices
SUBGROUP 3			
Solderability	2022 or 2003		15
SUBGROUP 4			
Internal Visual: Mechanical	2014		1 Device
SUBGROUP 5			
Bond Strength	2011	Test Condition C or D	15
SUBGROUP 6			
NA			
SUBGROUP 7			
Seal	1014		5
Fine			
Gross			
SUBGROUP 8			
NA			
GROUP C			
SUBGROUP 1			5
Steady State Life Test	1005	1000 hrs. at 125°C	
Electrical End Points			
SUBGROUP 2			
Temperature Cycling	1010	Test Condition C	15
Constant Acceleration	2001	Test Condition E, Y only	
Seal	1014		
Fine			
Gross			
Visual Examination	1010 or 1011		
Electrical End Points			
GROUP D			
SUBGROUP 1			15
Physical Dimensions	2016		
SUBGROUP 2			15
Lead Integrity	2004	Test Condition B2	
Seal	1014		
Fine			
Gross			

Conformance Flow (Cont.)

MIL-STD-883C Quality Conformance Tests	Method	Test Condition	LTPD
GROUP D (Cont.)			
SUBGROUP 3			15
Thermal Shock	1011	Test Condition B, 15 Cycles	
Temperature Cycling	1010	Test Condition C, 100 Cycles	
Moisture Resistance	1004		
Seal	1014		
Fine			
Gross			
Visual Examination			
Electrical End Points			
SUBGROUP 4			15
Mechanical Shock	2002	Test Condition B	
Vibration Variable Frequency	2007	Test Condition A	
Constant Acceleration	2001	Test Condition E, Y1 only	
Seal	1014		
Fine			
Gross			
Visual Examination	1010 or 1011		
Electrical End Points			
SUBGROUP 5			15
Salt Atmosphere	1009	Test Condition A	
Seal	1014		
Fine			
Gross			
Visual Examination	1009		
SUBGROUP 6			
Internal Water-Vapor Content	1018	5,000 PPM — CerDIP only	3 Devices
SUBGROUP 7			15
Adhesion of Lead Finish	2025		
SUBGROUP 8			
Lid Torque	2024		5 Devices

Quality Assurance
Integrated Circuit Screening


PLASTIC PACKAGE
STANDARD
HI REL
* Pre Cap Visual 1
* Pre Cap Visual 2
Stabilization Bake Temp = 150°C Time = 48 hrs.
Stabilization Bake Temp = 150°C Time = 96 hrs.
Temperature Cycling 10 Cycles – 65°C to + 150°C
Temperature Cycling 10 Cycles – 65°C to + 150°C
Pressure Cooker Test 4 Hours, 2 ATMOS 10% LTPD
Pressure Cooker Test 4 Hours, 2 ATMOS 10% LTPD
Electrical Test
Electrical Test
Burn-in 160 HRS. AT 125°C
Electrical Test
QA Acceptance Tests
QA Acceptance Tests
HERMETIC PACKAGE
STANDARD
HI REL PER MIL STD 883
* Pre Cap Visual 1
* Pre Cap Visual 2
Stabilization Bake Temp = 150°C Time = 48 hrs.
Stabilization Bake Temp = 150°C Time = 96 hrs.
Temperature Cycling 10 Cycles – 65°C to + 150°C
Temperature Cycling 10 Cycles – 65°C to + 150°C
Constant Acceleration Y, Orientation, 30KG's
Package Seal Fine Leak Test Gross Leak Test
Package Seal Fine Leak Test Gross Leak Test
Electrical Test
Electrical Test
Burn-in 160 HRS. AT 125°C
Electrical Test 5% PDA
QA Acceptance Tests
Visual Inspection
Q A Acceptance Tests

*1. TE-AYG-000732 (TSC Spec)
2. MIL-STD-883, Method 2010

Device Reliability

Reliability

The work of the Reliability Group at TSC has resulted in a product which should far exceed the reliability needs of any customer. Two important measures of device failure rate are stress testing under elevated temperature and under elevated temperature in conjunction with elevated humidity.

Steady State Life

Device reliability is often measured by survival rate under high temperature operating conditions. Figure 3 illustrates expected failure rate per 1000 hrs. of operating time over a temperature range from 25° C to 175° C. This graph is for TSC CMOS integrated circuits. The data was derived from results of Dynamic high temperature stress testing at 125° C and 150° C and calculations based on MIL-HDBK 217D.

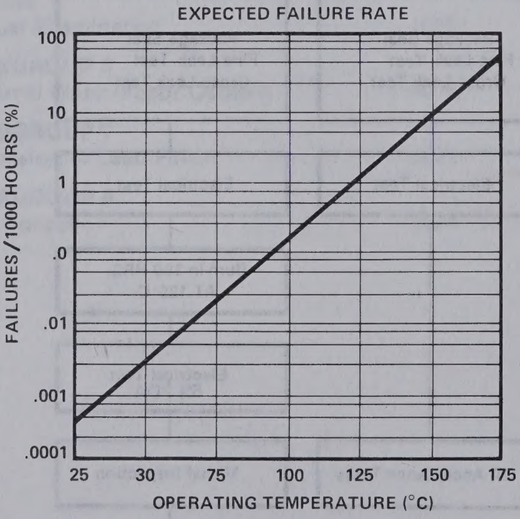


Figure 3

Temperature and Humidity

A major indicator of the reliability of a plastic encapsulated device (commercial class) is its ability to withstand temperature and humidity combined. Elevated temperature and humidity testing is routinely performed by TSC to evaluate the affect of these conditions on device reliability. The industry standard of 85° C and 85% Relative Humidity is used. Teledyne Semiconductor has a policy of using proven state-of-the-art molding compounds in its assembly process. Figure 4 illustrates the improvement this has made in TSC device reliability as measured by the 85/85 stress test.

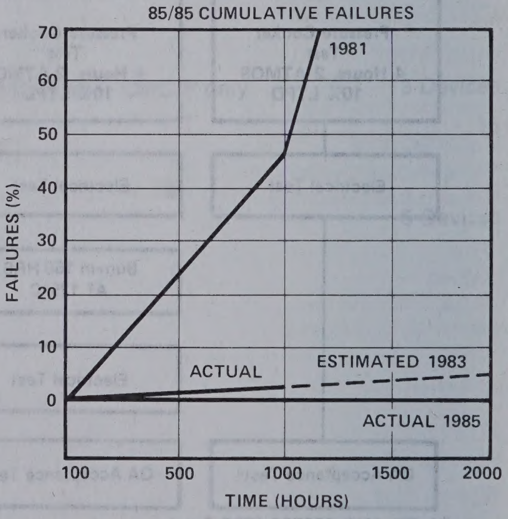


Figure 4

I.C. Handling Precautions

Transportation

Two main concerns to be minimized during transportation are mechanical vibration and shock and Electrostatic Discharge (ESD) damage. While mechanical shock can be minimized by suitable packing and handling, ESD damage requires additional measures including:

- Use containers or jigs which will not induce static electricity as the result of vibration during transportation. It is desirable to use an electrically conductive foam or aluminum foil and static eliminating bags.
- In order to prevent device damage from clothing-induced static electricity, workers should be properly grounded with grounding straps while handling devices. A resistor of about 1 M ohm must be provided to protect from electric shock.
- When transporting the printed circuit boards on which semiconductor devices are mounted suitable preventive measures against static electricity transfer and induction must be taken. Shorting connectors should be placed on open contacts and the board transported in electrically conductive bags.

Storage

It is preferable to store semiconductor devices in the following ways to prevent deterioration in their electrical characteristics, solderability, and mechanical appearance.

- Store in an ambient temperature of 5 to 30° C, and in a relative humidity of 40 to 60%.
- Store in a clean air environment, free from dust and active gas.
- Store in a container which does not induce static electricity.

  Store without any physical load.

  If semiconductor devices are stored for a long time, store them as sent from the factory. If their lead wires are formed beforehand, they may corrode during storage.

  If the chips are unsealed, store them in a cool, dry, dark, and dustless place. Assemble them within 5 days after unpacking. Storage in nitrogen gas is desirable. They can be stored for 20 days or less in dry nitrogen gas with a dew point at −30° C or lower. Unpacked chips must not be stored for over 3 months.

  Take care not to allow condensation during storage due to rapid temperature changes.

I.C. Handling Precautions (cont.)

Testing

Avoid ESD, noise or voltage surges when testing ICs. The device is in its least protected state during handling, insertion and testing. Any test equipment that leaks current or is allowed to attain only a few hundred volts of ESD can destroy CMOS ICs. All equipment must be grounded and periodically tested for leakage.

Soldering

Semiconductor devices should not be left at high temperatures for a long time. Regardless of the soldering method, soldering must be done in a short time and at the lowest possible temperature. Soldering work must meet soldering heat test conditions, namely, 260° C for 10 seconds and 350° C for 3 seconds at a point 1 to 1.5 mm away from the end of the device package.

Use of a strong alkali or acid flux may corrode the leads, deteriorating reliabilty and device characteristics. The recommended soldering iron is the type that is operated with a secondary voltage supplied by a transformer and grounded to protect from lead current. Solder the leads at the farthest point from the device package.

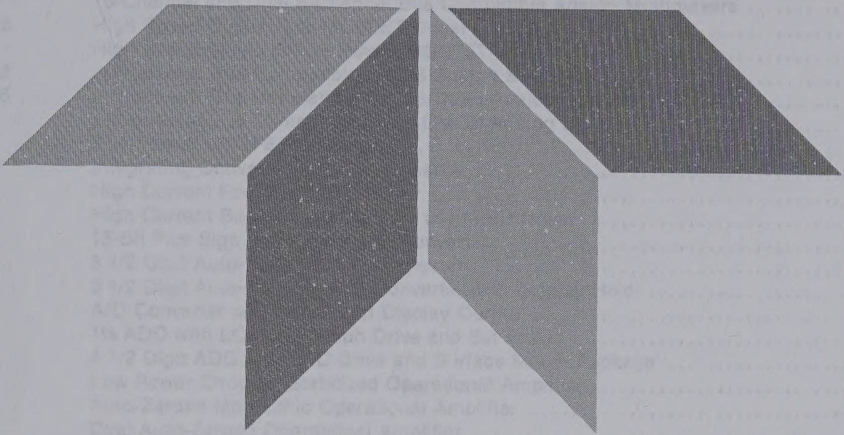
Personnel

- All personnel handling or in close proximity to ICs must wear anti-static clothing and shoes.
- Handling personnel must wear grounding straps.
- Work surfaces and straps should be earth grounded through a 1 M ohm resistor.
- Floors and carpets should be treated so as not to generate static electricity.
- Unrelated sources of RF or static electrical fields (e.g., plastic boxes, plastic wrappers) should be kept away from device handling areas.

Removing Residual Flux

To insure the reliability of electronic systems, residual flux must be removed from circuit boards. Detergent or ultrasonic cleaning is usually applied. If chloric detergent is used for the plastic molded devices, package corrosion may occur. Since cleaning over extended periods or at high temperatures may cause swollen chip coating due to solvent permeation, select the type of detergent and cleaning condition carefully. Do not use trichloroethylene. For ultrasonic cleaning, the following conditions are advisable:

- Frequency: 28 to 29 kHz (to avoid device resonation)
- Ultrasonic output: 15W/ℓ
- Keep the devices out of direct contact with the power generator.
- Cleaning time: Less than 30 seconds
- Clean Freon™ is recommended if other conditions permit.



SECTION 4

Alphanumeric Product List

Alphanumeric Product List

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SECTION 5

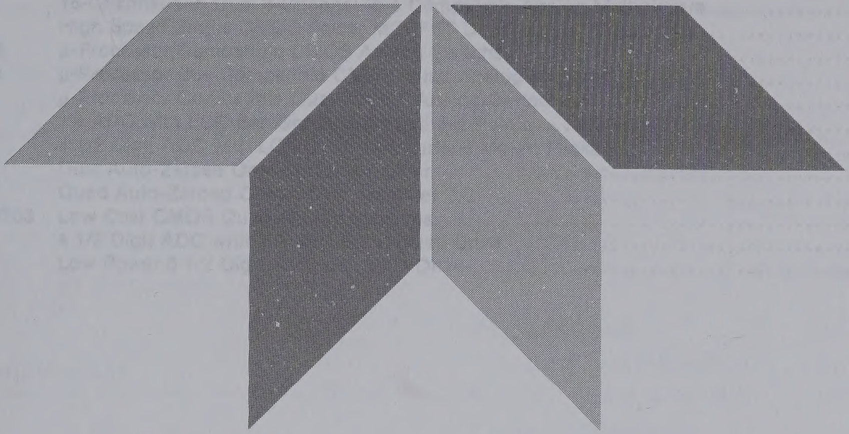
Cross Reference Guide

All TSC Products Cross-Referenced Are Plug-In Replacements

Part Number	TSC Number	Comments
ADC-EK10B	TSC8701CJ	
ADC-EK12B	TSC8702CN	
ADC-EK12DC	TSC8750CJ	
ADC-EK12DM	TSC8750BN	
ADC-EK12DR	TSC8750CN	
ADC-EK08B	TSC8700CJ	
ADC-ET10BC	TSC8704CJ	
ADC-ET10BM	TSC8704BN	
ADC-ET10BR	TSC8704CN	
ADC-ET12BC	TSC8705CJ	
ADC-ET12BM	TSC8705BN	
ADC-ET12BR	TSC8705CN	
ADC-ET8BC	TSC8703CJ	
ADC-ET8BM	TSC8703BL	
ADC-ET8BR	TSC8703CL	
CD22104AE	TSC7211AIPL	
CD22105AE	TSC7211AMIPL	
DS0026CJ-8	TSC4261JA	Pin Compatible, Functional Upgrade
DS0026CN-8	TSC426CPA	Pin Compatible, Functional Upgrade
DS0026J-8	TSC426MJA	Pin Compatible, Functional Upgrade
HLCD7211-2	TSC7211AIPL	
HLCD7211-4	TSC7211AMIPL	
ICL7106CJL	TSC7106CJL	TSC7106ACPL Has Improved Reference Voltage
ICL7106CPL	TSC7106CPL	TSC7106ACPL Offers Improved Reference Tempco
ICL7106RCPL	TSC7106RCPL	TSC7106ARCPL Offers Improved Reference Tempco
ICL7107CJL	TSC7107CJL	TSC7107ACJL Offers Improved Reference Tempco
ICL7107CPL	TSC7107CPL	TSC7107ACPL Offers Improved Reference Tempco
ICL7107RCPL	TSC7107RCPL	TSC7107ARCPL Offers Improved Reference Tempco
ICL7109CPL	TSC7109CPL	Exact Replacement. TSC7109BCPL For Lower Cost
ICL7109IJL	TSC7109IJL	
ICL7109MJL	TSC7109MJL	
ICL7116CJL	TSC7116CJL	TSC7116ACJL Offers Improved Reference Tempco
ICL7116CPL	TSC7116CPL	TSC7116ACPL Offers Improved Reference Tempco
ICL7117CJL	TSC7117CJL	TSC7117ACJL Offers Improved Reference Tempco
ICL7117CPL	TSC7117CPL	TSC7117ACPL Offers Improved Reference Tempco

All TSC Products Cross-Referenced Are Plug-In Replacements (Cont.)

Part Number	TSC Number	Comments
ICL7126CJL	TSC7126CJL	TSC7126ACJL Offers Improved Reference Tempco
ICL7126CPL	TSC7126CPL	TSC7126ACPL Offers Improved Reference Tempco
ICL7136CJL	TSC7126CJL	TSC7126CJL and TSC7126ACJL Are Plug-In Replacements
ICL7136CPL	TSC7126CPL	TSC7126CPL and TSC7126ACPL Are Plug-In Replacements
ICL7650CPA	TSC7650CPA	TSC900ACPA is a Low-Power Plug-In Upgrade
ICL7650CPD	TSC7650CPD	TSC900ACPD is a Low-Power Plug-In Upgrade
ICL7650IJA	TSC7650IJA	TSC900AIJA is a Low-Power Plug-In Upgrade
ICL7650IJD	TSC7650IJD	TSC900AIJD is a Low-Power Plug-In Upgrade
ICL7660CPA	TSC7660CPA	
ICL7660IJA	TSC7660IJA	
ICL7660MJA	TSC7660MJA	
ICL8069CCZR	TSC9491AJ	
ICL8069CMSQ	TSC9491AM	
ICL8069DCZR	TSC9491BJ	
ICL8069DMSQ	TSC9491BM	
ICM7211AIPL	TSC7211AIPL	
ICM7211AMIPL	TSC7211AMIPL	
ICM7212AIJL	TSC7212AIJL	TSC700AIJL is a Higher LED Current Upgrade for "Brighter" Displays
ICM7212AIPL	TSC7212AIPL	TSC700AIJL is a Higher LED Current Upgrade for "Brighter" Displays
ICM7212AMIJL	TSC7212AMIJL	TSC700AMIJL is a Higher LED Current Upgrade for "Brighter" Displays
ICM7212AMIPL	TSC7212AMIPL	TSC701AMIJL is a Higher LED Current Upgrade for "Brighter" Displays
MC14433L	TSC14433CL	TSC14433ACL Offers Guaranteed Roll-Over Spec.
MC14433P	TSC14433CJ	TSC14433ACJ Offers Guaranteed Roll-Over Spec.
MMH0026CP1	TSC426CPA	Pin Compatible, Functional Upgrade
MMH0026CU	TSC426IJA	Pin Compatible, Functional Upgrade
MP5531C	TSC9495CJ	
MP5532C	TSC9496CJ	
REF01CP	TSC9495CJ	
REF02CP	TSC9495CJ	
TP4780	TSC9400CJ	
TP4781	TSC9401CJ	
VFQ-1C	TSC9400CJ	
VFQ-1R	TSC900CL	



SECTION 6

Advance Product Information

Section 6

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TELEDYNE SEMICONDUCTOR

Advance Product Information

TSC04/1.2 V
TSC05/2.5 V
Band-Gap Reference

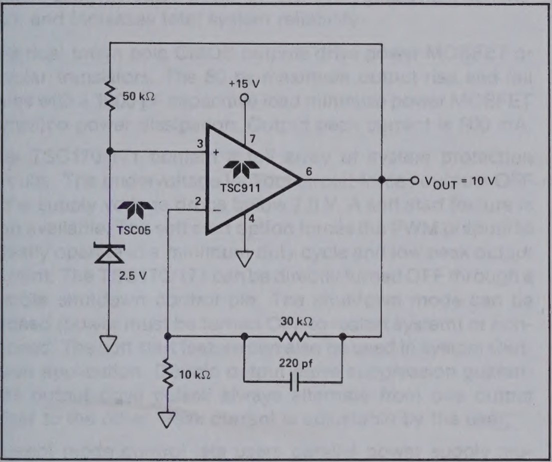
6

General Description

The TSC04 (1.2 V Output) and TSC05 (2.5 V Output) bipolar two terminal band-gap voltage references offer precision performance without a premium price. The TSC04/05 do not use thin film resistors. This greatly lowers manufacturing complexity and cost.

A 50 ppm/°C output temperature coefficient and 25 μA to 10 mA operating current range make the devices attractive multimeter, data acquisition converter, and telecommunication voltage references

Typical Application



50 kΩ
+15 V
3
7
+
6
V_OUT = 10 V
TSC911
2
−
4
TSC05
2.5 V
30 kΩ
220 pf
10 kΩ

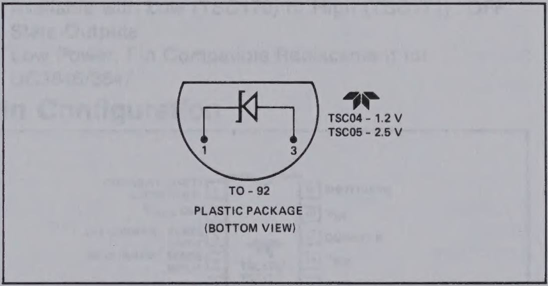
Features

- 50 ppm/°C Temperature Coefficient
- 25 μA to 10 mA Operating Current Range
- 1 Ω Dynamic Impedance
- Low Cost TO-92 Plastic Package
- 1% Output Tolerance
- 1.2 V (TSC04) and 2.5 V (TSC05) Output Voltage Option

Applications

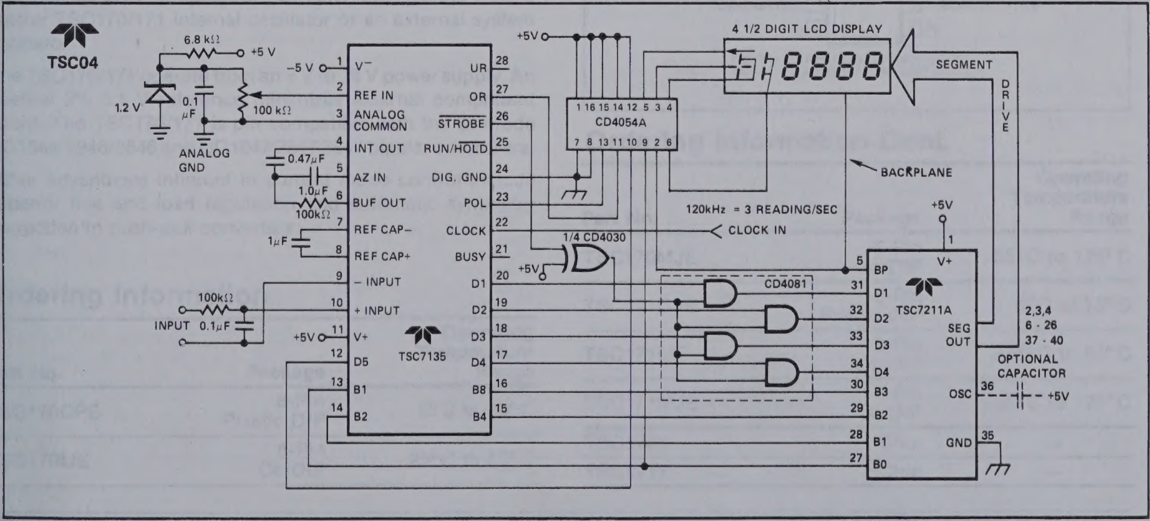
- ADC and DAC Reference
- Current Source Generation
- Threshold Detectors
- Power Supplies
- Multimeters

Pin Configuration



1
3
TSC04 - 1.2 V
TSC05 - 2.5 V
TO - 92
PLASTIC PACKAGE
(BOTTOM VIEW)

Typical 4 1/2 Digit DVM with LCD Display



TSC04
6.8 kΩ
+5 V
1.2 V
0.1 μF
100 kΩ
ANALOG GND
−5 V
0.47μF
1.0μF
100kΩ
1μF
100kΩ
INPUT
0.1μF
+5V
1 V−
2 REF IN
3 ANALOG COMMON
4 INT OUT
5 AZ IN
6 BUF OUT
7 REF CAP−
8 REF CAP+
9 − INPUT
10 + INPUT
11 V+
12 D5
13 B1
14 B2
28 UR
27 OR
26 STROBE
25 RUN/HOLD
24 DIG. GND
23 POL
22 CLOCK
21 BUSY
20 D1
19 D2
18 D3
17 D4
16 B8
15 B4
TSC7135
+5V
1 16 15 14 12 5 3 4
CD4054A
7 8 13 11 10 9 2 6
4 1/2 DIGIT LCD DISPLAY
SEGMENT DRIVE
BACKPLANE
120kHz = 3 READING/SEC
CLOCK IN
1/4 CD4030
+5V
CD4081
+5V
1
5 BP
V+
31 D1
32 D2
33 D3
34 D4
30 B3
29 B2
28 B1
27 B0
TSC7211A
SEG OUT
2,3,4
6 - 26
37 - 40
OPTIONAL CAPACITOR
OSC 36
+5V
GND 35

Notes

TELEDYNE SEMICONDUCTOR

Advance Product Information

TSC170/TSC171
CMOS Current Mode SMPS Controller

- 3.8 mA Max. Supply Current
- 50 ns Output Rise/Fall Time
- 500 mA Output Drive

General Description

The TSC170/171 bring low power CMOS technology to the current mode switching power supply controller market. Maximum supply current is 3.8 mA. Bipolar current mode control integrated circuits require five times more operating current. Low power supply current eliminates auxiliary power transformers. In off line powering schemes where a simple zener diode circuit provides device supply voltage, power dissipation is greatly reduced. CMOS technology decreases system cost, increases power efficiency, reduces heat generation, and increases total system reliability.

The dual totem pole CMOS outputs drive power MOSFET or bipolar transistors. The 50 ns maximum output rise and fall times with a 1000 pF capacitive load minimize power MOSFET transition power dissipation. Output peak current is 500 mA.

The TSC170/171 contain a full array of system protection circuits. The undervoltage lockout circuit forces outputs OFF if the supply voltage drops below 7.0 V. A soft start feature is also available. The soft start option forces the PWM outputs to initially operate at a minimum duty cycle and low peak output current. The TSC170/171 can be directly turned OFF through a remote shutdown control pin. The shutdown mode can be latched (power must be turned OFF to restart system) or non-latched. The soft start feature can also be used in system shutdown application. Double output pulse suppression guarantees output drive pulses always alternate from one output driver to the other. Peak current is adjustable by the user.

Current mode control lets users parallel power supply modules. Two or more TSC170/171 controllers can be slaved together for parallel operation. Circuits can operate from a master TSC170/171 internal oscillator or an external system oscillator.

The TSC170/171 operate from an 8 V to 16 V power supply. An internal 2% 5.1 V reference minimizes external component count. The TSC170/171 is pin compatible with the Unitrode UC1846/2846/3846 and UC1847/2847/3847 bipolar controllers.

Other advantages inherent in current mode control include superior line and load regulation and automatic symmetry correction in push-pull converters.

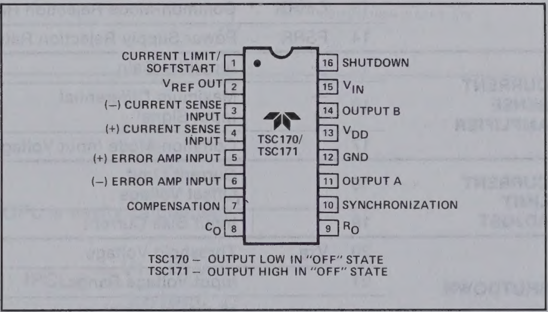
Ordering Information

Part No.	Package	Operating Temperature Range
TSC170CPE	8-Pin Plastic DIP	0° C to 70° C
TSC170IJE	8-Pin CerDIP	-25° C to 85° C

Features

- Low Supply Current with CMOS Technology .... 3.8 mA Maximum
- Current Mode Control
- Internal Reference .... 5.1 V
- Fast Output Rise/Fall Time (C_L = 1000 pF) ...... 50 ns
- Dual Push-Pull Outputs
- Direct Power MOSFET Drive
- High Totem Pole Output Drive .... 500 mA
- Differential Current Sense Amplifier
- Programmable Current Limit
- Soft start Operation
- Double Pulse Suppression
- Under-Voltage Lockout
- Wide Supply Voltage Operation .... 8 to 16 V
- High Frequency Operation .... 200 kHz
- Plastic and CerDIP Package
- Available with Low (TSC170) or High (TSC171) "OFF" State Outputs
- Low Power, Pin Compatible Replacement for UC3846/3847

Pin Configuration



TSC170 – OUTPUT LOW IN "OFF" STATE
TSC171 – OUTPUT HIGH IN "OFF" STATE

Ordering Information Cont.

Part No.	Package	Operating Temperature Range
TSC170MJE	8-Pin CerDIP	-55° C to 125° C
TSC171CPE	8-Pin Plastic DIP	0° C to 70° C
TSC171IJE	8-Pin CerDIP	-25° C to 85° C
TSC171MJE	8-Pin CerDIP	-55° C to 125° C
TSC170Y	Chip	—
TSC171Y	Chip	—

©1985

TSC170/171

CMOS Current Mode SMPS Controller

- **3.8 mA Max. Supply Current**
- **50 ns Output Rise/Fall Time**
- **500 mA Output Drive**

Absolute Maximum Ratings

Input Voltage (Pin 15) .... 18 V
Output Voltage (Pin 13) .... V_{IN} (18 V)
Analog Inputs (Pins 3, 4, 5, 6, 16) .. -0.3 V to V_{IN} + 0.3 V
Storage Temperature Range .... -65 °C to +150 °C
Lead Temperature (Soldering, 10 Seconds) ..... +300 °C
Maximum Chip Temperature .... 150 °C

CerDIP Package Thermal Resistance:
(Junction to Ambient) .... 105 °C/W
(Junction to Case) .... 60 °C/W
Plasting Package Thermal Resistance:
(Junction to Ambient) .... 140 °C/W
(Junction to Case) .... 70 °C/W
Operating Temp. Range
Commercial .... 0 °C to +85 °C
Industrial .... -25 °C to +85 °C

Electrical Characteristics: V_{IN} = 16 V, R_O = 24 kΩ, C_O = 1 nF, T_A = 25 °C Unless otherwise indicated.

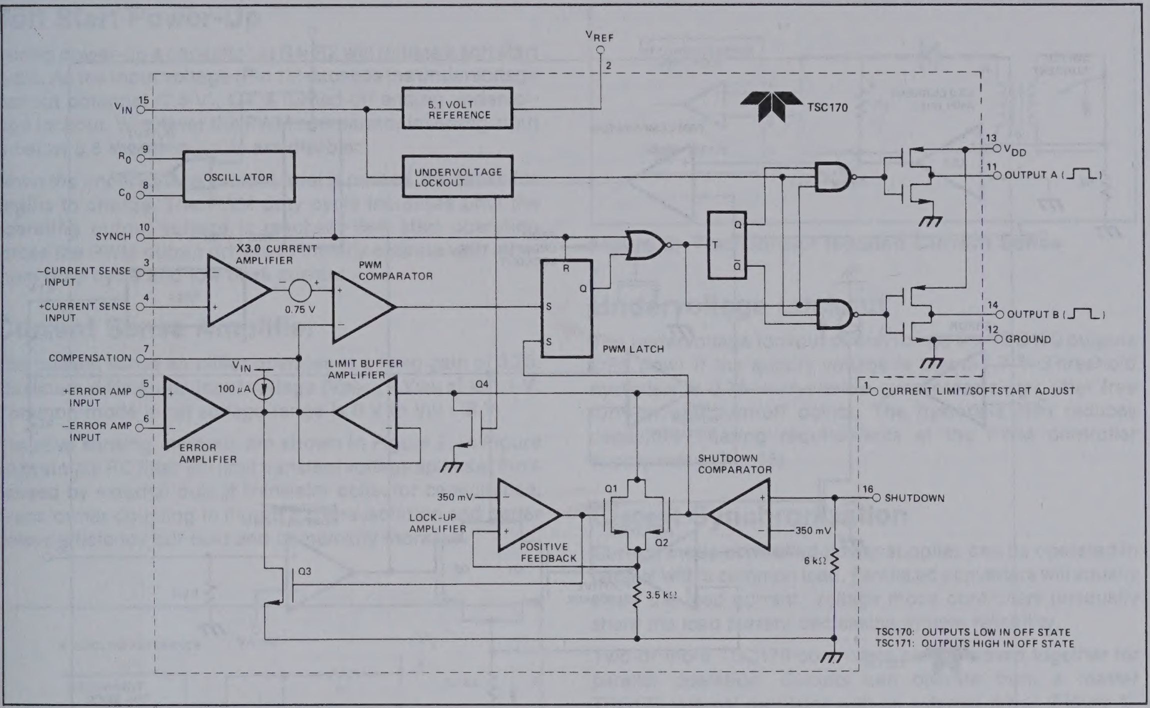
TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITION	TSC170/171 MIN	TSC170/171 TYP	TSC170/171 MAX	UNIT
REFERENCE VOLTAGE	1	V_{REF}	Output Voltage	I_{OUT} = 1 mA	5.0	5.1	5.2	V
	2	—	Line Regulation	V_{IN} = 8 V to 16 V	—	5	15	mV
	3		Load Regulation	I_{OUT} = 1 mA to 10 mA	—	3	15	mV
	4	V_{RTC}	Temperature Coefficient	Over Operating Temp. Range	—	0.4	0.5	mV/°C
OSCILLATOR	5	—	Initial Frequency	—	38	42	46	kHz
	6	—	Voltage Stability	V_{IN} = 8 V to 16 V	—	1.1	1.5	°/°/V
	7	—	Temperature Stability	Over Operating Temp. Range	—	5	10	%
ERROR AMPLIFIER	8	V_{EOS}	Input Offset Voltage		—	—	20	mV
	9	I_B	Input Bias Current		—	—	1	nA
	10	V_{CMRR}	Common-Mode Input Voltage	V_{IN} = 8 V to 16 V	0	—	V_{IN} -2 V	V
	11	A_{VOL}	Open-Loop Voltage Gain	V_{OUT} = 1 V to 6 V	70	—	—	dB
	12	BW	Unity Gain Bandwidth		—	1.2	—	MHz
	13	CMRR	Common-Mode Rejection Ratio	V_{CMV} = 0 to 14 V	60	—	—	dB
	14	PSRR	Power Supply Rejection Ratio	V_{IN} = 8 V to 16 V	60	—	—	dB
CURRENT SENSE AMPLIFIER	15	—	Amplifier Gain	Pin 3 = 0 to 1.1 V	2.5	3.0	3.5	V/V
	16	—	Maximum Differential Input Signal	V_{PIN4} - V_{PIN3}	1.1	—	—	V
	17		Common-Mode Input Voltage		0	—	V_{IN} -3 V	V
CURRENT LIMIT ADJUST	18		Current Limit Offset Voltage		0.5	—	1	V
	19		Input Bias Current		—	—	1	nA
SHUTDOWN TERMINAL	20	V_{TB}	Threshold Voltage		0.3	0.35	0.4	V
	21		Input Voltage Range		0	—	V_{IN}	V
	22		Minimum Latching Current at Pin 1		125	—	—	μA
	23		Maximum Non-Latching Current at Pin 1		—	—	50	μA
OUTPUT STAGE	24	V_{DD}	Output Voltage	Pin 13	—	—	V_{IN}	V
	25	V_{OL}	Output Low Level	I_{SINK} = 20 mA	—	—	0.4	V
	26	V_{OL}	Output Low Level	I_{SINK} = 100 mA	—	—	2.0	V
	27	V_{OH}	Output High Level	I_{SOURCE} = 20 mA	V_{IN} - 1 V	—	—	V
	28	V_{OH}	Output High Level	I_{SOURCE} = 100 mA	V_{IN} -3.5 V	—	—	V
	29	t_R	Output Rise Time	C_L = 1000 pF	—	50	150	ns
	30	t_F	Output Fall Time	C_L = 1000 pF	—	50	150	ns
UNDERVOLTAGE LOCKOUT	31		Start-up	Threshold	—	7.7	8.25	V
	32		Threshold Hysteresis		0.5	0.75	1.0	V
SUPPLY	33	I_S	Standby Supply Current		—	2.7	3.8	mA

1. Advance Product Information.

CMOS Current Mode SMPS Controller

- **3.8 mA Max. Supply Current**
- **50 ns Output Rise/Fall Time**
- **500 mA Output Drive**

TSC170/171


V_REF
2
15
V_IN
5.1 VOLT REFERENCE
TSC170
9
R_0
OSCILLATOR
8
C_0
UNDERVOLTAGE LOCKOUT
13
V_DD
11
OUTPUT A
10
SYNCH
X3.0 CURRENT AMPLIFIER
3
−CURRENT SENSE INPUT
PWM COMPARATOR
R
Q
T
Q
Q̄
4
+CURRENT SENSE INPUT
0.75 V
S
S
14
OUTPUT B
12
GROUND
PWM LATCH
7
COMPENSATION
V_IN
LIMIT BUFFER AMPLIFIER
5
+ERROR AMP INPUT
100 µA
Q4
1
CURRENT LIMIT/SOFTSTART ADJUST
6
−ERROR AMP INPUT
ERROR AMPLIFIER
SHUTDOWN COMPARATOR
350 mV
Q1
16
SHUTDOWN
LOCK-UP AMPLIFIER
Q2
350 mV
POSITIVE FEEDBACK
6 kΩ
Q3
3.5 kΩ
TSC170: OUTPUTS LOW IN OFF STATE
TSC171: OUTPUTS HIGH IN OFF STATE

Block Diagram

Peak Current Limit Setup

Resistors R1 and R2 at the current limit input (Pin 1) set the TSC170 peak current limit (Figure 1). The potential at Pin 1 is easily calculated:

$$V1 = V_{REF} \frac{R2}{R1 + R2}$$

R1 should be selected first. The shutdown circuit feature is not latched for (VREF - 0.35)/R1<50 µA and is latched for currents greater than 125 µA.

The error amplifier output voltage is clamped from going above V1 through the limit buffer amplifier. Peak current is sensed by RS and amplified by the current amplifier which has a fixed gain of 3.0.

IPCL, the peak current limit, is the current that causes the PWM comparator non-inverting input to exceed V1; the potential at the inverting input. Once the comparator trip point is exceeded both outputs are disabled.

ICPL is easily calculated:

1) $IPCL = \frac{V1 - .75\ V}{3.0\ (RS)}$

where:

a) $V1 = REF \frac{R2}{R1 + R2}$

b) VREF = Internal voltage reference = 5.1 V

c) 3.0 V = Voltage gain of current sense amplifier

d) 0.75 V = Current limit offset

Both driver outputs (Pin 11 and Pin 14) are OFF (low) when the peak current limit is exceeded. When the sensed current goes below IPCL the circuit operates normally.

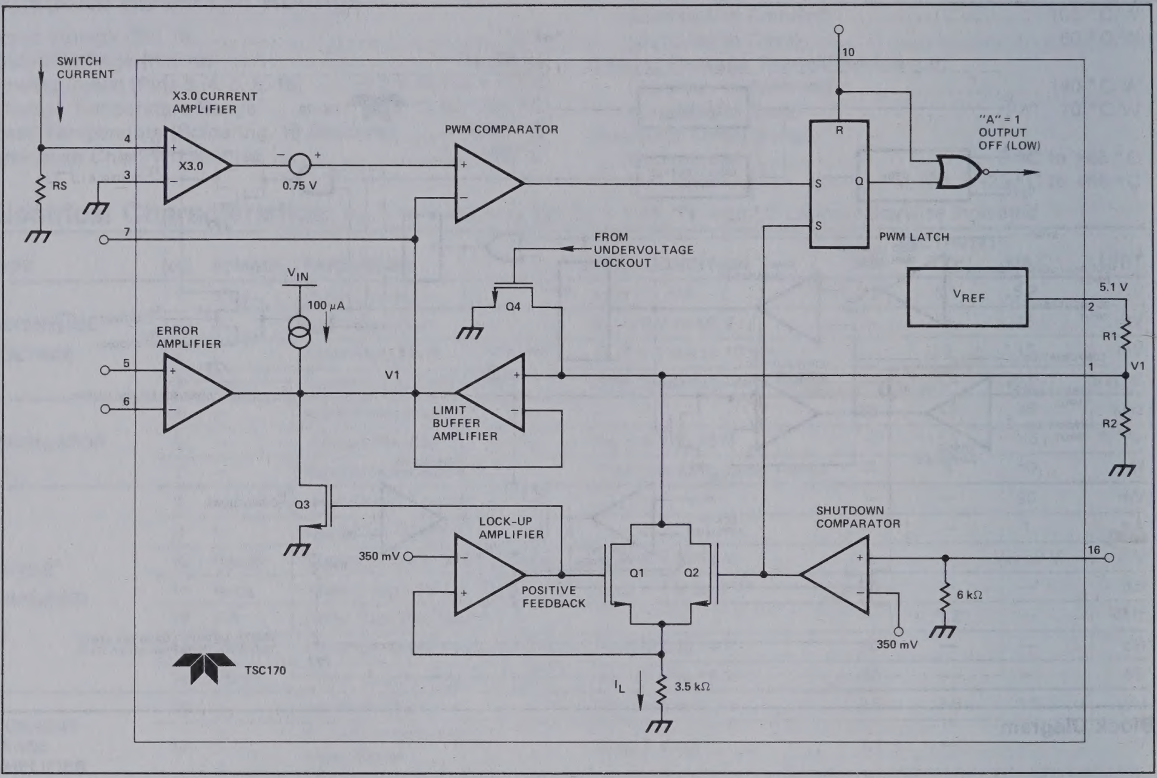

SWITCH CURRENT
X3.0 CURRENT AMPLIFIER
X3.0
RS
4
3
7
0.75 V
PWM COMPARATOR
R
S
Q
S
PWM LATCH
10
"A" = 1 OUTPUT OFF (LOW)
FROM UNDERVOLTAGE LOCKOUT
Q4
V_{IN}
100 μA
ERROR AMPLIFIER
5
6
V1
LIMIT BUFFER AMPLIFIER
V_{REF}
5.1 V
2
R1
1
V1
R2
Q3
LOCK-UP AMPLIFIER
350 mV
POSITIVE FEEDBACK
Q1
Q2
SHUTDOWN COMPARATOR
16
6 kΩ
350 mV
TSC170
I_L
3.5 kΩ

Figure 1: R1 and R2 Set Maximum Peak Output Current

Output Shutdown

The TSC170 outputs can be turned off quickly through the shutdown input (Pin 16). A signal greater than 350 mV at Pin 16 forces the shutdown comparator output high. The PWM latch is held set disabling the outputs.

Q2 is also turned on. If VREF/R1 is greater than 125 μA, positive feedback through the lock-up amplifier and Q1 keeps the inverting PWM comparator inverting input below 0.75 V. Q3 remains on even after the shutdown input signal is removed because of the positive feedback. The state can be cleared only through a power-up cycle. Outputs will be disabled whenever the potential at Pin 1 is below 0.75 V.

The shutdown terminal gives a fast, direct way to disable the TSC170 output transistors. System protection and remote shutdown applications are possible.

Soft Restart from Shutdown

A soft restart can be programmed if non-latched shutdown operation is used.

A capacitor at Pin 1 will cause a gradual increase in potential toward V1. When the voltage at Pin 1 reaches 0.75 V the PWM latch set input is removed and the circuit establishes a regulated output voltage. The soft start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak currents.

Soft Start Power-Up

During power-up a capacitor at R1, R2 will initiate a soft start cycle. As the input voltage (Pin 15) exceeds the undervoltage lockout potential (7.5 V), Q4 is turned off ending undervoltage lockout. Whenever the PWM comparator inverting input is below 0.5 V both outputs are disabled.

When the undervoltage lockout level is passed, the capacitor begins to charge. The PWM duty cycle increases until the operating output voltage is reached. Soft start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak current.

Current Sense Amplifier

The current sense amplifier operates at a fixed gain of 3.25. Maximum differential input voltage ($V_{PIN\ 4} - V_{PIN\ 3}$) is 1.1 V. Common-mode input voltage range is 0 V to V_{IN} - 3 V.

Resistive sensing methods are shown in Figure 2. In Figure 2A, a simple RC filter will limit transient voltage spikes at Pin 4 caused by external output transistor collector capacitance. Transformer coupling in Figure 3 offers isolation and better power efficiency but cost and complexity increase.

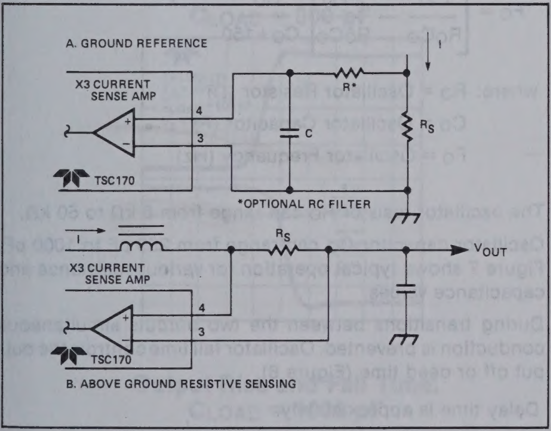


Figure 2: Resistive Sensing

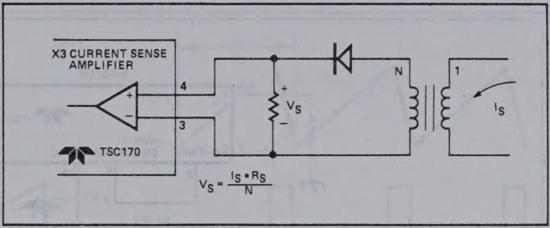


Figure 3: Transformer Isolated Current Sense

Undervoltage Lockout

The undervoltage lockout circuit forces the TSC170 outputs OFF (low) if the supply voltage is below 7.7 V. Threshold hysterisis is 0.75 V. Hysterisis guarantees clean, jitter free turn-on and turn-off points. The hysterisis also reduces capacitive filtering requirements at the PWM controller supply input (Pin 15).

Circuit Synchronization

Current mode controlled power supplies can be operated in parallel with a common load. Paralleled converters will equally share the load current. Voltage mode controllers unequally share the load current decreasing system reliability.

Two or more TSC170 controllers can be slaved together for parallel operation. Circuits can operate from a master TSC170 internal oscillator with an external driver (Figure 4). Devices can also be slaved to an external oscillator (Figure 5). Disable internal slave device oscillators by grounding Pin 8. Slave controllers derive an oscillator from the bi-directional synchronization output signal at Pin 10.

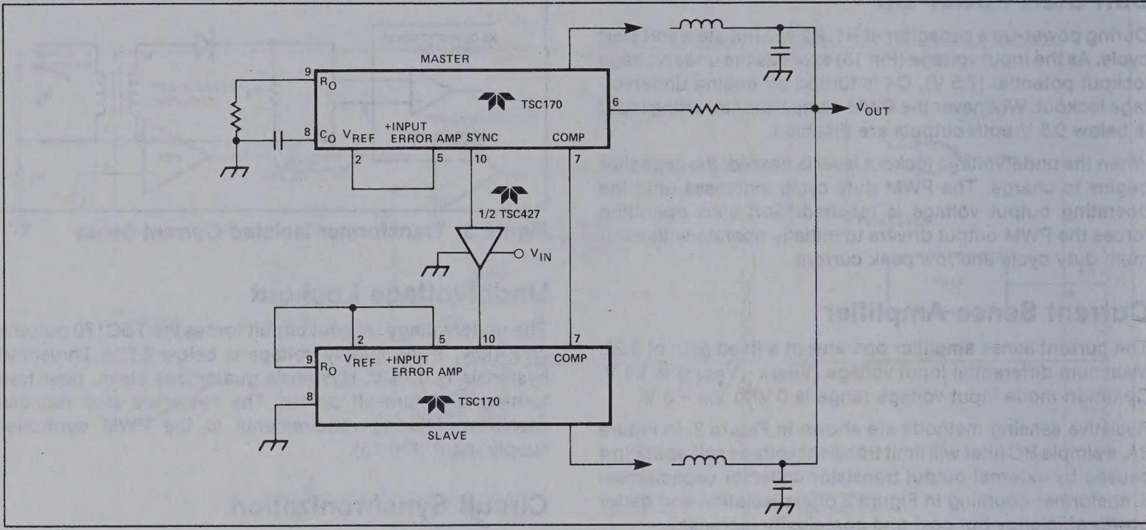

MASTER
9
RO
TSC170
6
8
CO
VREF
+INPUT
ERROR AMP SYNC
COMP
2
5
10
7
VOUT
1/2 TSC427
VIN
2
5
10
7
9
RO
VREF
+INPUT
ERROR AMP
COMP
8
TSC170
SLAVE

Figure 4: Master/Slave Parallel Operation

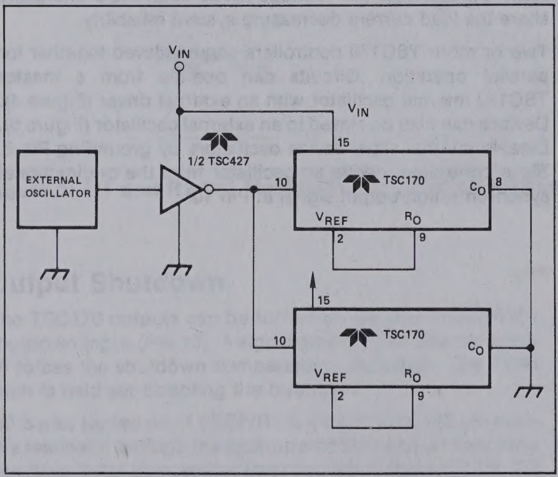

VIN
VIN
15
1/2 TSC427
EXTERNAL OSCILLATOR
10
TSC170
CO
8
VREF
RO
2
9
15
10
TSC170
CO
VREF
RO
2
9

Figure 5: External Clock Synchronization

Oscillator Frequency and Output Dead Time

The oscillator frequency for $R_O = 24\ k\Omega$ and $C_O = 1000$ pF is:

$$F_O = \left[\frac{1.27}{R_O C_O} - \frac{2800}{R_O^2 C_O}\right] \frac{C_O}{C_O + 150}$$

where: R_O = Oscillator Resistor (Ω)

C_O = Oscillator Capacitor (F)

F_O = Oscillator Frequency (Hz)

The oscillator resistor R_O can range from 5 kΩ to 50 kΩ.

Oscillator capacitor C_O can range from 250 pF to 1000 pF. Figure 7 shows typical operation for various resistance an capacitance values.

During transitions between the two outputs simultaneou conduction is prevented. Oscillator fall time controls the output off or dead time (Figure 6).

Delay time is approximately:

$$T_D = \frac{2000\ [C_O]}{1 - \left(\frac{2.3}{R_O}\right)}$$

Where: R_O = Oscillator Resistor (kΩ)

C_O = Oscillator Capacitor (F)

T_D = Output Dead Time (sec.)

Maximum possible duty cycle is set by the delay time.

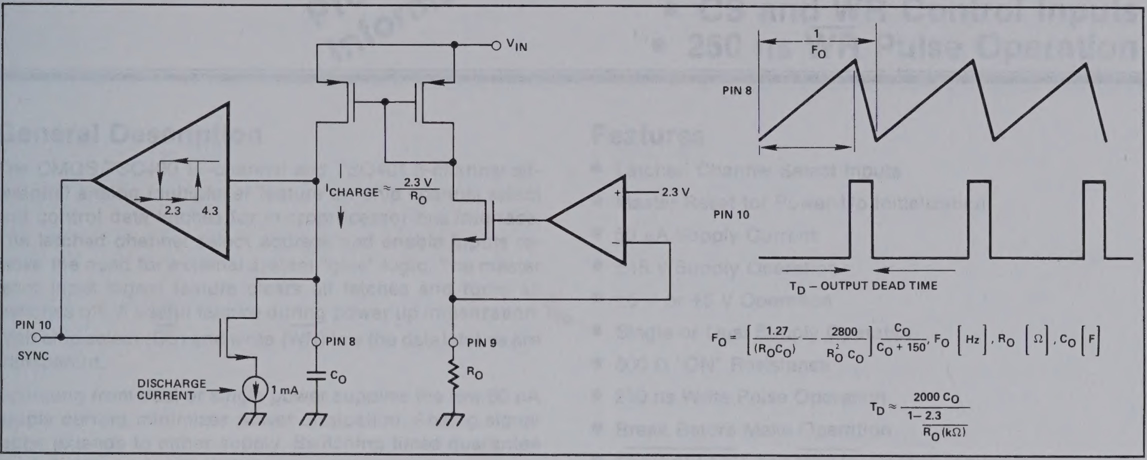
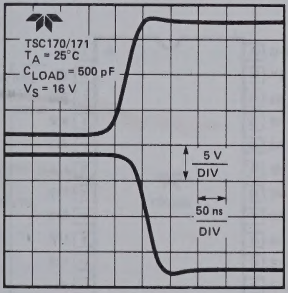

V_{IN}
$I_{CHARGE} \approx \frac{2.3\ V}{R_O}$
2.3
4.3
2.3 V
+
−
PIN 10
SYNC
DISCHARGE CURRENT
1 mA
PIN 8
C_O
PIN 9
R_O
$\frac{1}{F_O}$
PIN 8
PIN 10
T_D – OUTPUT DEAD TIME
$F_O = \left[\frac{1.27}{(R_O C_O)} - \frac{2800}{R_O^2 C_O}\right] \frac{C_O}{C_O + 150}$, F_O [Hz], R_O [Ω], C_O [F]
$T_D \approx \frac{2000\ C_O}{1 - \frac{2.3}{R_O (k\Omega)}}$

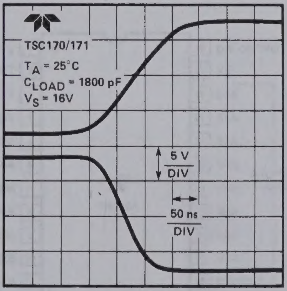
Figure 6: TSC170 Oscillator Circuit

Typical Characteristic Curves

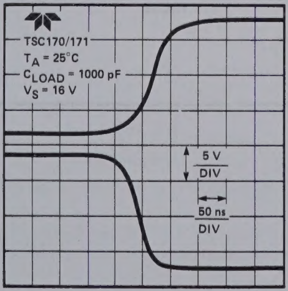
Output Rise and Fall Time: C_{LOAD} = 500 pF



Output Rise and Fall Time: C_{LOAD} = 1800 pF

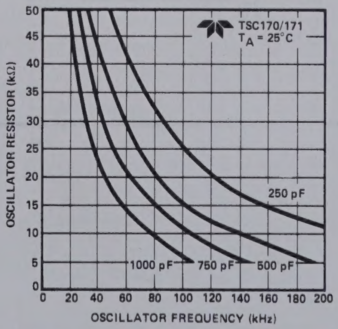


Output Rise and Fall Time: C_{LOAD} = 1000 pF



(Figure 7)

Oscillator Frequency vs Oscillator Resistance



Notes

TELEDYNE SEMICONDUCTOR

TSC400/401

16-Channel and Dual 8-Channel Bus Compatible Analog Multiplexers

- ±15 V Dual Supply or Single Supply Operation
- $\overline{\text{CS}}$ and $\overline{\text{WR}}$ Control Inputs
- 250 ns $\overline{\text{WR}}$ Pulse Operation

Advance Product Information

General Description

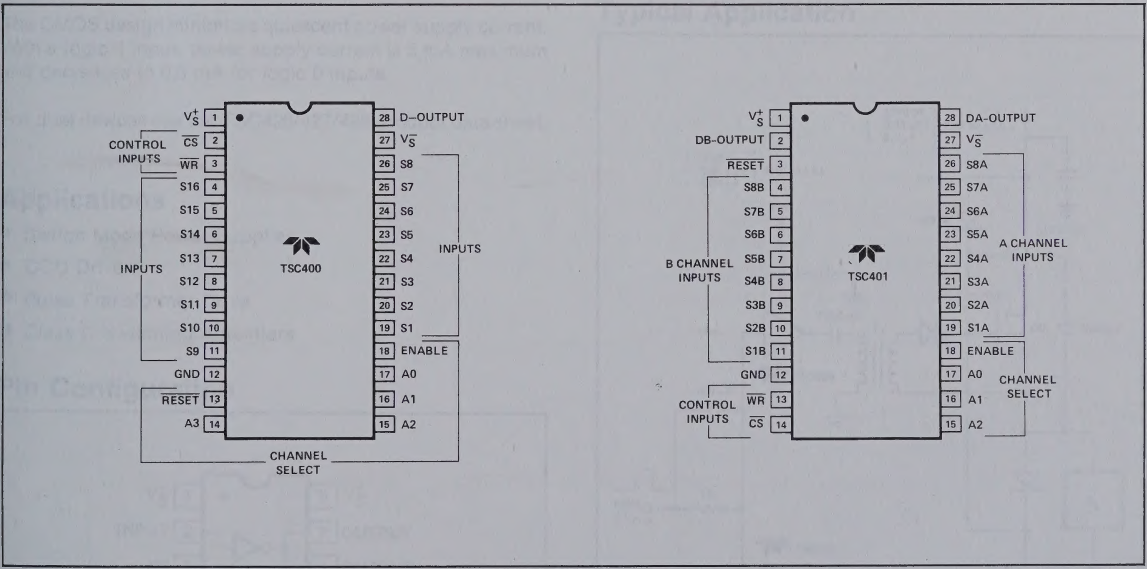
The CMOS TSC400 16-channel and TSC401 8-channel differential analog multiplexer feature on-chip channel select and control data latches for microprocessor bus interface. The latched channel select address and enable inputs remove the need for external system "glue" logic. The master reset input signal feature clears all latches and turns all switches off. A useful feature during power up initialization. With chip select ($\overline{\text{CS}}$) and write ($\overline{\text{WR}}$) low the datalatches are transparent.

Operating from dual or single power supplies the low 50 μA supply current minimizes power dissipation. Analog signal range extends to either supply. Switching times guarantee break before make operation.

Features

- Latched Channel Select Inputs
- Master Reset for Power-Up Initialization
- 50 μA Supply Current
- ±15 V Supply Operation
- ±5 V or +5 V Operation
- Single or Dual Supply Operation
- 500 Ω "ON" Resistance
- 250 ns Write Pulse Operation
- Break Before Make Operation
- $\overline{\text{CHIP SELECT}}$ and $\overline{\text{WRITE}}$ Control Inputs

Pin Configuration



TSC400
V+S 1
CONTROL INPUTS
CS 2
WR 3
S16 4
S15 5
S14 6
S13 7
S12 8
S11 9
S10 10
S9 11
GND 12
RESET 13
A3 14
INPUTS
28 D–OUTPUT
27 V−S
26 S8
25 S7
24 S6
23 S5
22 S4
21 S3
20 S2
19 S1
18 ENABLE
17 A0
16 A1
15 A2
INPUTS
CHANNEL SELECT
TSC401
V+S 1
DB-OUTPUT 2
RESET 3
S8B 4
S7B 5
S6B 6
S5B 7
S4B 8
S3B 9
S2B 10
S1B 11
GND 12
WR 13
CS 14
B CHANNEL INPUTS
CONTROL INPUTS
28 DA-OUTPUT
27 V−S
26 S8A
25 S7A
24 S6A
23 S5A
22 S4A
21 S3A
20 S2A
19 S1A
18 ENABLE
17 A0
16 A1
15 A2
A CHANNEL INPUTS
CHANNEL SELECT

Notes

TELEDYNE SEMICONDUCTOR

Advance Product Information

TSC429

High Speed Single CMOS Power MOSFET Driver

- 25 ns Rise/Fall Time with $C_L = 2500$ pF
- 3.5 A Peak Drive Current
- 2.5 Ω Output Resistance

General Description

The TSC429 is a single high speed CMOS level translator and driver. Designed specifically to drive highly capacitive power MOSFET gates, the TSC429 features a 2.5 Ω output impedance and 3.5 A peak output current drive.

A 2500 pF capacitive load will be driven 18 V in 25 ns. Delay time through the device is 25 ns. The rapid switching times with large capacitive loads minimize power MOSFET transition power loss.

A TTL/CMOS input logic level is translated into an output voltage swing that equals the supply. The output will swing to within 25 mV of ground or V_S^+. Input voltage swing may equal the supply. Logic input current is under 1 μA making direct interface to CMOS/Bipolar switch mode power supply controllers easy. Input "speed-up" capacitors are not required.

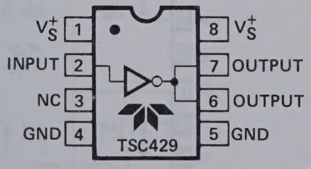
The CMOS design minimizes quiescent power supply current. With a logic 1 input, power supply current is 5 mA maximum and decreases to 0.5 mA for logic 0 inputs.

For dual devices see the TSC426/427/428 product data sheet.

Applications

- Switch Mode Power Supplies
- CCD Drivers
- Pulse Transformer Drive
- Class D Switching Amplifiers

Pin Configuration

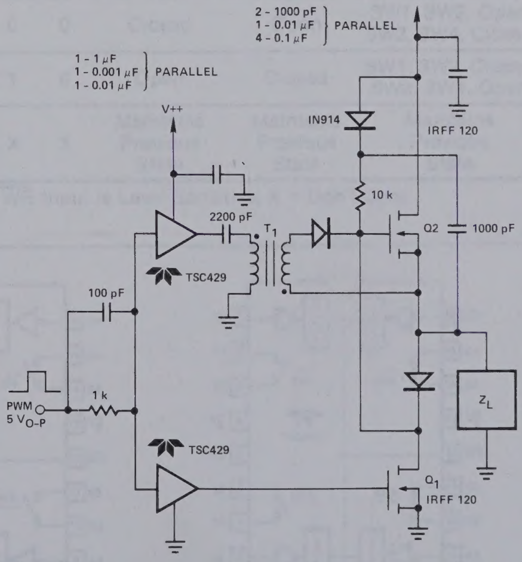

V_S^+ 1
INPUT 2
NC 3
GND 4
8 V_S^+
7 OUTPUT
6 OUTPUT
5 GND
TSC429

NC = NO INTERNAL CONNECTION

Features

- Wide Operating Range .... 4.5 V to 18 V
- High Impedance CMOS Logic Input
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
  - — 5 mA Maximum with Logic 1 Input
  - — 0.5 mA Maximum with Logic 0 Input
- Output Voltage Swing Within 25 mV of Ground or V_S^+.
- Low Delay Time .... 25 ns
- High Capacitive Load Drive Capability
  - — t_{RISE}, t_{FALL} = 25 ns with C_{LOAD} = 2500 pF
- Single +5 V Supply Operation

Typical Application


2 - 1000 pF
1 - 0.01 μF
4 - 0.1 μF
PARALLEL
1 - 1 μF
1 - 0.001 μF
1 - 0.01 μF
PARALLEL
V++
IN914
IRFF 120
10 k
2200 pF
T_1
Q2
1000 pF
TSC429
100 pF
1 k
PWM
5 V_{O-P}
Z_L
TSC429
Q_1
IRFF 120

Notes

TELEDYNE SEMICONDUCTOR

TSC441/442/443

μ-Processor Compatible CMOS Analog Switches

• Data Latches
• Low Power CMOS
• 200 ns Write Pulse Operation

Advance Product Information

General Description

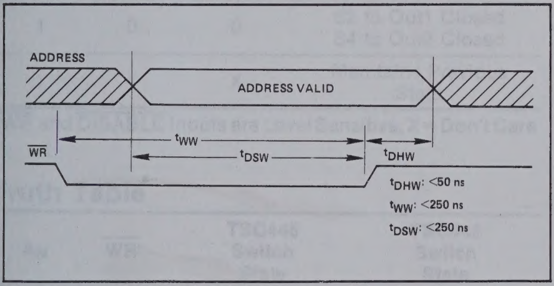
The TSC441, TSC442, and TSC443 are quad SPST analog switches with data address latches. The pin out matches the "201" analog switch configuration. Pin 12, which is unused on the 201, is the write enable ($\overline{WR}$) input. With $\overline{WR}$ tied low the data address latch is transparent.

The family features single or dual power supply operation with analog input voltage range equal to the supply voltage. Power supply current is a low 300 μA.

The TSC441/442 have opposite input logic polarity. The TSC443, with two normally open and two normally closed switches, can be configured as a quad SPST, dual SPDT, DPDT or dual DPST switch.

For devices pin compatible with the AD7590/7591/7592 see the TSC444/445/456 specifications.

Timing Diagram



Features

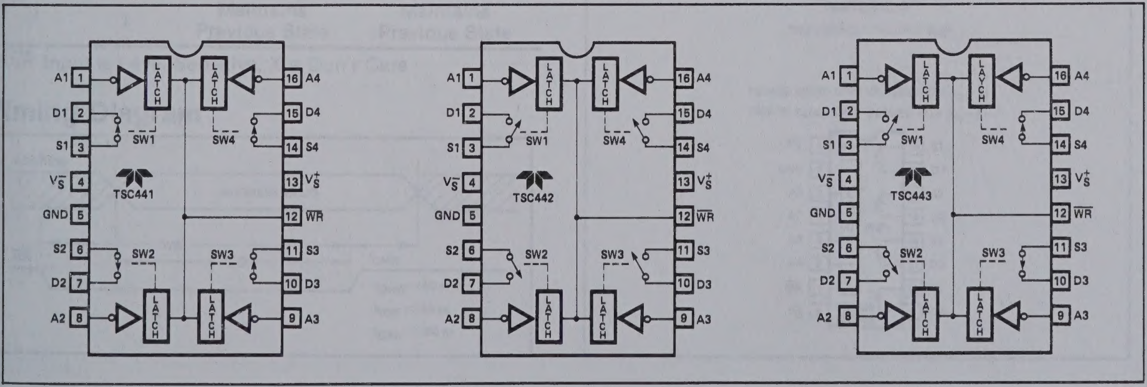
- Data Address Latch On-Chip
- Latch Transparent with $\overline{WR} = 0$
- < 250 ns Write Pulse Operation
- < 50 ns Address Hold Time
- Dual ±5 V or Single +5 to +15 V Supply Operation
- 300 μA Supply Current
- 120 Ω ON Resistance
- 1 nA Analog Input Leakage Current
- Analog Signal Range Equal to Supply Voltage
- TTL/CMOS Compatible, Low Current Logic Input
- TSC441: Pin Compatible to DG221
- "201" Pin Out Compatible (Pin 12 = $\overline{\text{WRITE ENABLE}}$)
- TSC443: SPST, SPDT, DPDT, DPST Configuration

Truth Table

A_N	$\overline{WR}$*	TSC441 Switch State	TSC442 Switch State	TSC443 Switch State
0	0	Closed	Open	SW1, SW2, Open SW3, SW4, Closed
1	0	Open	Closed	SW1, SW2, Closed SW3, SW4, Open
X	1	Maintains Previous State	Maintains Previous State	Maintains Previous State

* $\overline{WR}$ Input is Level Sensitive, X = Don't Care

Pin Configuration



TELEDYNE SEMICONDUCTOR

TSC444/445/446

μ-Processor Bus Compatible CMOS Quad Analog Switches

• Data Latches

• Low Power CMOS

• 200 ns Write Pulse Operation

Advance Product Information

General Description

The TSC444, TSC445, and TSC446 μ-processor compatible analog switch family combine four analog switches with a data address latch. Quad SPST devices (445/446) and dual SPDT (444) devices feature 120 Ω ON resistance and 1 nA analog input leakage currents. Analog input signal range extends to the power supply rails. A low 300 μA supply current and single or dual supply operation make the family ideal for battery operated systems. Break before make operation is guaranteed. Input logic signals are TTL/CMOS compatible.

Truth Table

$\overline{\text{DISABLE}}$*	$\overline{\text{WR}}$*	A1 or A2	TSC444 Switch State
0	X	X	All Switches Open
1	0	1	S1 to Out1 Closed S3 to Out2 Closed
1	0	0	S2 to Out1 Closed S4 to Out2 Closed
1	1	X	Maintains Previous State

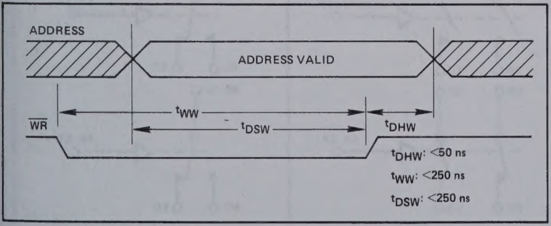
* $\overline{\text{WR}}$ and $\overline{\text{DISABLE}}$ Inputs are Level Sensitive, X = Don't Care

Truth Table

A_N	$\overline{\text{WR}}$*	TSC445 Switch State	TSC446 Switch State
0	0	Open	Closed
1	0	Closed	Open
X	1	Maintains Previous State	Maintains Previous State

* $\overline{\text{WR}}$ Input is Level Sensitive, X = Don't Care

Timing Diagram

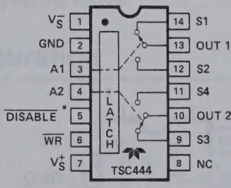

ADDRESS
ADDRESS VALID
$\overline{\text{WR}}$
t_{WW}
t_{DSW}
t_{DHW}
t_{DHW}: <50 ns
t_{WW}: <250 ns
t_{DSW}: <250 ns

Features

- Data Address Latch On-Chip
- Latch Transparent with $\overline{\text{WR}}$ = 0
- SPST and SPDT Options
- Dual ±5 V Supply Operation
- Single +5 V to +15 V Supply Operation
- 300 μA Supply Current
- 120 Ω ON Resistance
- 1 nA Analog Input Leakage Current
- < 250 ns Write Pulse Operation
- < 50 ns Address Hold Time
- TTL/CMOS Compatible, Low Current Logic Input
- Analog Signal Range Equal to Supply Voltage
- TSC445 Pin Compatible to AD7590
- TSC446 Pin Compatible to AD7591
- TSC444 Pin Compatible to AD7592

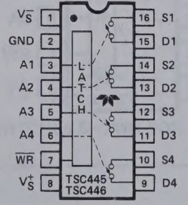
Pin Configuration

TSC444: DUAL SPDT


V_S^- 1
GND 2
A1 3
A2 4
$\overline{\text{DISABLE}}$* 5
$\overline{\text{WR}}$ 6
V_S^+ 7
14 S1
13 OUT 1
12 S2
11 S4
10 OUT 2
9 S3
8 NC
LATCH
TSC444

*INTERNALLY PULLED HIGH

TSC445: QUAD SPST (CLOSED FOR A_N = 1)
TSC446: QUAD SPST (CLOSED FOR A_N = 0)


V_S^- 1
GND 2
A1 3
A2 4
A3 5
A4 6
$\overline{\text{WR}}$ 7
V_S^+ 8
16 S1
15 D1
14 S2
13 D2
12 S3
11 D3
10 S4
9 D4
LATCH
TSC445
TSC446

Notes

TELEDYNE SEMICONDUCTOR

Advance Product Information

TSC447

μ-Processor Compatible Quad CMOS Analog Switch

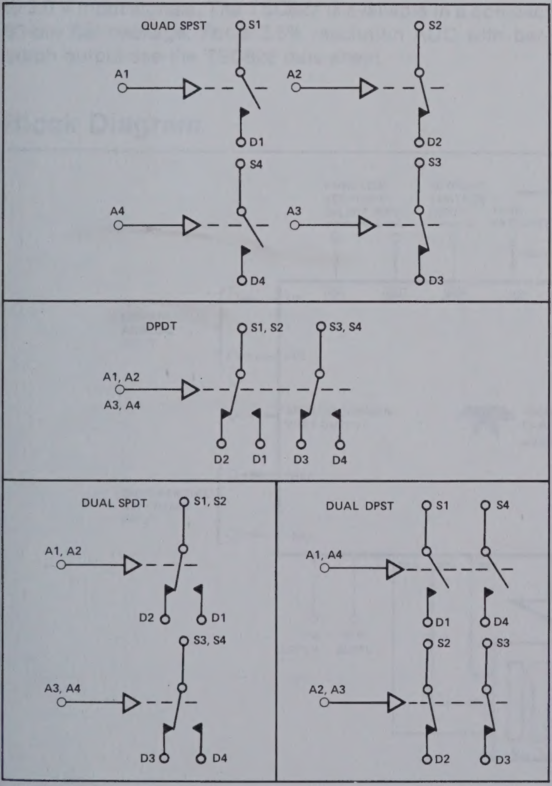
- **Data Latch**
- **Two Normally ON and Two Normally OFF Switches**
- **+15 V, ±5 V, +5 V Operation**

General Description

The TSC447 μ-processor compatible analog switch contains four analog switches with a data address latch. Two devices are normally ON and two normally OFF. Analog input signal range extends to the power supply rails. Input leakage current is a low 1 nA. The 300 μA supply current and single or dual supply operation make the TSC447 ideal for battery operated systems. The TSC447 operates with +15 V, ±5 V or a single +5 V supply.

Break before make operation is guaranteed. The TSC447 can be connected as a latched Quad SPST, Dual SPDT, DPDT or Dual DPST analog switch. Input logic signals are TTL/CMOS compatible.

Application Configurations


QUAD SPST
A1
S1
D1
A2
S2
D2
S4
A4
D4
A3
S3
D3
DPDT
S1, S2
S3, S4
A1, A2
A3, A4
D2
D1
D3
D4
DUAL SPDT
S1, S2
A1, A2
D2
D1
S3, S4
A3, A4
D3
D4
DUAL DPST
S1
S4
A1, A4
D1
D4
S2
S3
A2, A3
D2
D3

ADDRESS INPUTS (A_N) = 0 (LATCHES NOT SHOWN)

Features

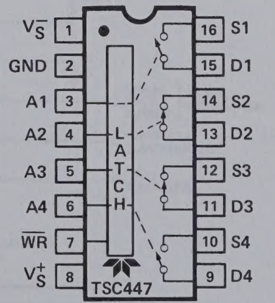
- Data Address Latch On-Chip
- Latch Transparent with $\overline{WR} = 0$
- Two Normally Open and Two Normally Closed Switches
- Dual ±5 V or +15 V Supply Operation
- Single +5 V to +15 V Supply Operation
- 300 μA Supply Current
- 120 Ω On Resistance
- 1 nA Analog Input Leakage Current
- <250 ns Write Pulse Operation
- <50 ns Address Hold Time
- TTL/CMOS Compatible, Low Current Logic Input
- Analog Signal Range Equal to Supply Voltage

TSC447 Truth Table

A_N	$\overline{WR}$*	Switch 1 & 4 State	Switch 2 & 3 State
0	0	Open	Closed
1	0	Closed	Open
X	1	Maintains Previous State	Maintains Previous State

$\overline{WR}$* Input is Level Sensitive

Pin Configuration


V_S^- 1
GND 2
A1 3
A2 4
A3 5
A4 6
$\overline{WR}$ 7
V_S^+ 8
16 S1
15 D1
14 S2
13 D2
12 S3
11 D3
10 S4
9 D4
LATCH
TSC447

SWITCHES SHOWN FOR $A_N = 0$

Notes

TELEDYNE SEMICONDUCTOR

TSC827
1% ADC with LCD Bar-Graph Drive

Advance Product Information

- Two Selectable Set Points
- 10-Bit Serial Data Output
- 20 mW Power Dissipation

General Description

The TSC827 is a complete integrating analog-to-digital converter with triplex liquid crystal (LCD) display drive. A 101 element LCD bar-graph directly connects to the TSC827.

Two user selected set points can be programmed and displayed. LCD annunciators distinguish between set points. Set point annunciators are activated when a set point has been reached. An input overrange LCD annunciator is also present. Set point and overrange logic outputs are provided for control applications.

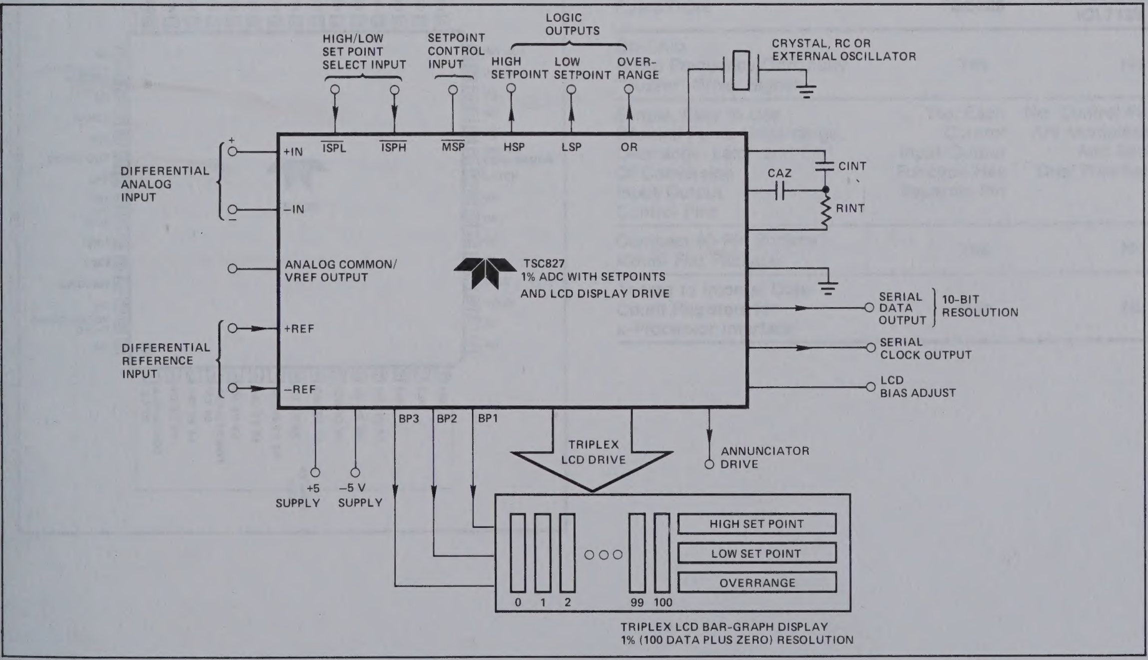
A 10-bit serial output with clock allows data to be transmitted at 0.1% resolution to a remote computer or display.

Operating from ±5 V supplies, the CMOS TSC827 dissipates only 20 mW. Included on-chip is a precision 75ppm/°C low drift voltage reference. The differential inputs accept 40 mV to 2.0 V input signals. The TSC827 is available in a compact 60-pin flat package. For a 2.5% resolution ADC with bar-graph output see the TSC826 data sheet.

Features

- 1% LCD Bar-Graph Readout
  - — Triplex LCD Display
  - — 101 Data Segments
  - — Overrange and Set Point Annunciators
- Two Selectable Set Points
- Low and High Set Point and Overrange Logic Output Signals
- Differential Analog Input
- Differential Reference for Ratiometric Measurements
- 40 mV to 2.0 V Full-Scale
- 10-Bit Serial Data Output
- ±5 V Supply Operation
- 20 mW Power Dissipation
- Compact 60-Pin Flat Package

Block Diagram


HIGH/LOW SET POINT SELECT INPUT
SETPOINT CONTROL INPUT
LOGIC OUTPUTS
HIGH SETPOINT
LOW SETPOINT
OVER-RANGE
CRYSTAL, RC OR EXTERNAL OSCILLATOR
+IN
ISPL
ISPH
MSP
HSP
LSP
OR
DIFFERENTIAL ANALOG INPUT
+
−
−IN
CAZ
CINT
RINT
ANALOG COMMON/ VREF OUTPUT
TSC827 1% ADC WITH SETPOINTS AND LCD DISPLAY DRIVE
SERIAL DATA OUTPUT
10-BIT RESOLUTION
SERIAL CLOCK OUTPUT
LCD BIAS ADJUST
DIFFERENTIAL REFERENCE INPUT
+REF
−REF
BP3
BP2
BP1
+5 SUPPLY
−5 V SUPPLY
TRIPLEX LCD DRIVE
ANNUNCIATOR DRIVE
HIGH SET POINT
LOW SET POINT
OVERRANGE
0
1
2
99
100
TRIPLEX LCD BAR-GRAPH DISPLAY 1% (100 DATA PLUS ZERO) RESOLUTION

Notes

TELEDYNE SEMICONDUCTOR

Advance Product Information

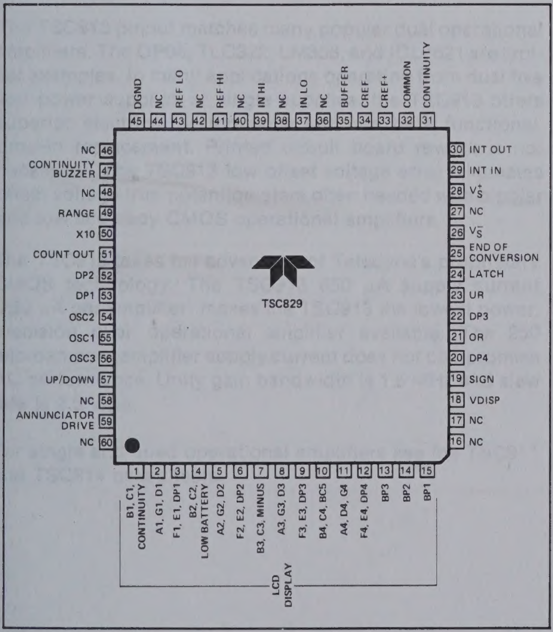
TSC829
4 1/2 Digit ADC with LCD Drive
• Continuity Audio Signal • 10 μV Resolution • 10 mW Power Dissipation

General Description

The CMOS TSC829 combines a precision 4 1/2 digit ADC, and triplex LCD display drive circuit in a single low power CMOS chip. The TSC829 offers several functional enhancements over the first generation ICL7129 converter. An audio frequency continuity buzzer signal is generated on-chip along with the continuity logic output signal. The TSC829 eliminates the external audio signal generator and piezoelectric driver needed in 7129 based systems. More compact and less costly systems result. The 60-pin flat package also allows the complicated dual function 7129 input/output control pins to be replaced by easy to use single function pins.

By using the UP/DOWN, SIGN, X10 and conversion count out logic signals the data can be transferred to a microprocessor.

Pin Configuration


DGND 45
NC 44
REF LO 43
NC 42
REF HI 41
NC 40
IN HI 39
NC 38
IN LO 37
NC 36
BUFFER 35
CREF- 34
CREF+ 33
COMMON 32
CONTINUITY 31
NC 46
CONTINUITY BUZZER 47
NC 48
RANGE 49
X10 50
COUNT OUT 51
DP2 52
DP1 53
OSC2 54
OSC1 55
OSC3 56
UP/DOWN 57
NC 58
ANNUNCIATOR DRIVE 59
NC 60
30 INT OUT
29 INT IN
28 V$_S^+$
27 NC
26 V$_S^-$
25 END OF CONVERSION
24 LATCH
23 UR
22 DP3
21 OR
20 DP4
19 SIGN
18 VDISP
17 NC
16 NC
TSC829
1 B1, C1, CONTINUITY
2 A1, G1, D1
3 F1, E1, DP1
4 B2, C2, LOW BATTERY
5 A2, G2, D2
6 F2, E2, DP2
7 B3, C3, MINUS
8 A3, G3, D3
9 F3, E3, DP3
10 B4, C4, BC5
11 A4, D4, G4
12 F4, E4, DP4
13 BP3
14 BP2
15 BP1
LCD DISPLAY

Features

- Triplex LCD Display Drive On-Chip
- Control Signals and Data Output for μ-Processor Interface
- Audio Frequency "Buzzer" Signal and Driver for Piezoelectric Continuity Transducer
- On-Chip Low Battery Detector and LCD Annunciator Driver
- On-Chip Continuity Detection and LCD Annunciator Driver
- Easy to Use Single Function DP4, OR, UR, DP3, LATCH and EOC Input/Output Control Pins
- 4 1/2 Digit Resolution
- 10 to 1 Digitally Controlled Full-Scale Range Selection
- Simple 1 V Reference for 200 mV or 2 V Full-Scale Range
- 10 μV Resolution on 200 mV Full-Scale Range

4 1/2 Digit Converter Comparison

FUNCTION	TSC829	GE/INTERSIL ICL7129
On-Chip Audio Frequency Continuity "Buzzer" Drive Signal	Yes	No
Simple, Easy to Use Decimal Point, Underrange, Overrange, Latch and End Of Conversion Input/Output Control Pins	Yes: Each Control Input/Output Function Has Separate Pin	No: Control Pins Are Multiplexed And Serve Dual Functions
Compact 60-Pin Surface Mount Flat Package	Yes	No
Access to Internal Data Count Registers for μ-Processor Interface	Yes	No

TELEDYNE SEMICONDUCTOR

Advance Product Information

TSC913

Dual Auto-Zeroed Operational Amplifier

- **15 μV Offset Voltage**
- **650 μA Supply Current**
- **No External Capacitors Required**

General Description

The TSC913 is the world's first complete monolithic dual auto-zeroed operational amplifier. The TSC913 sets a new standard for low power precision dual operational amplifiers. Chopper-stabilized or auto-zeroed amplifiers offer low offset voltage errors by periodically sampling offset error and storing correction voltages on capacitors. Previous single amplifier designs required two user supplied external 0.1 μF error storage correction capacitors — much too large for on-chip integration. The unique TSC913 architecture requires smaller capacitors making on-chip integration possible. Microvolt offset levels are achieved and **External Capacitors Are Not Required.**

The TSC913 system benefits are apparent when contrasted with a 7650 chopper amplifier circuit implementation. A single TSC913 replaces two 7650s and four capacitors. Five components and assembly steps are eliminated.

The TSC913 pinout matches many popular dual operational amplifiers. The OP04, TLC322, LM358, and ICL7621 are typical examples. In many applications operating from dual five volt power supplies or single supplies, the TSC913 offers superior electrical performance and can be a functional, drop-in replacement. Printed circuit board rework is not necessary. The TSC913 low offset voltage error eliminates offset voltage trim potentiometers often needed with bipolar and low accuracy CMOS operational amplifiers.

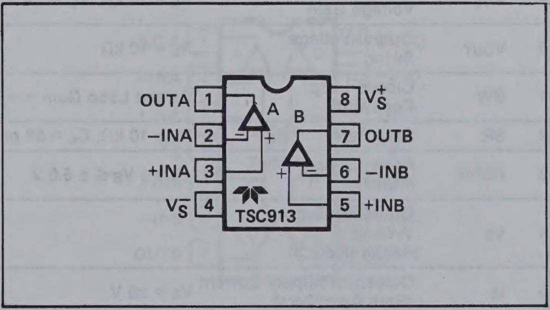
The TSC913 takes full advantage of Teledyne's proprietary CMOS technology. The TSC913 650 μA supply current (250 μA per amplifier) makes the TSC913 the lowest power, precision dual operational amplifier available. The 250 microampere amplifier supply current does not compromise AC performance. Unity gain bandwidth is 1.5 MHz and slew rate is 2.5 V/μs.

For single and quad operational amplifiers see the TSC911 and TSC914 data sheets.

Features

- First Monolithic Dual Auto-Zeroed Operational Amplifier
- Chopper Amplifier Performance Without External Capacitors
  - — 15 μV V_{OS} Maximum
  - — 0.15 μV/°C V_{OS} Drift Maximum
  - — Saves Cost/Assembly of Four "Chopper" Capacitors
- High DC Gain .... 120 dB
- Low Supply Current .... 650 μA
- Low Input Voltage Noise (0.1 to 10 Hz) .... 0.65 μV_{P-P}
- Wide Common-Mode Voltage Range .... V_S^- to V_S^+ -2 V
- High Common-Mode Rejection .... 116 dB
- Dual or Single Supply Operation .... ±3 V to ±8 V
+4.5 V to +16 V
- Excellent AC Operating Characteristics
  - — 2.5 V/μs Slew Rate
  - — 1.5 MHz Unity Gain Bandwidth
- Pin Compatible to LM358, OP14, MC1458, ICL7621, TL082, TLC322

Pin Configuration



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TSC913

Dual Auto-Zeroed Operational Amplifier

- **15 μV Offset Voltage**
- **650 μA Supply Current**
- **No External Capacitors Required**

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-)	18 Volts
Input Voltage	(V_S^+ + 0.3) to (V_S^- − 0.3) Volts
Storage Temp. Range	−55 °C to 150 °C
Lead Temperature (Soldering, 10 sec)	300 °C
Current into Any Pin	10 mA

Operating Temp. Range	
I Device	−25 °C to +85 °C
C Device	0 °C to +70 °C
Package Power Dissipation (T_A = 25 °C)	
CerDIP Package	500 mW
Plastic Package	375 mW

Electrical Characteristics: $V_S = \pm 5$, $T_A = 25°C$ unless otherwise indicated.

				TSC913A			TSC913B			
NO.	**SYMBOL**	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
1	V_{OS}	Input Offset Voltage	$T_A = 25°C$	—	5	15	—	15	30	μV
2	V_{OS}/T	Average Temperature Coefficient of Input Offset Voltage	$0°C \le T_A \le 70°C$ $-25°C \le T_A \le 85°C$	— —	0.05 0.05	0.15 0.15	— —	— —	0.25 0.25	μV/°C μV/°C
3	I_B	Average Input Bias Current	$T_A = 25°C$ $0°C \le T_A \le 70°C$ $-25°C \le T_A \le 85°C$	— — —	— — —	90 3 4	— — —	— — —	120 4 6	pA nA nA
4	I_{OS}	Average Input	Offset Current	—	5	20	—	10	40	pA
5	en	Input Voltage Noise	0.1 to 1.0 Hz, $R_S \le 100\ \Omega$	—	0.6	—	—	0.6	—	μV_{P-P}
6	en	Input Voltage Noise	0.1 to 10 Hz, $R_S \le 100\ \Omega$	—	11	—	—	11	—	μV_{P-P}
7	CMRR	Common-Mode Rejection Ratio	$V_S^- \le V_{CM} \le V_S^+ - 2.2$ V	110	116	—	100	110	—	dB
8	CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+ −2.0	V_S^-	—	V_S^+ −2.0	V
9	A_{OL}	Open-Loop Voltage Gain	$R_L = 10$ kΩ, $V_O = \pm 4$ V	115	120	—	110	120	—	dB
10	V_{OUT}	Output Voltage Swing	$R_L = 10$ kΩ	V_S^- + .3 V	—	V_S^+ −.9 V	V_S^- + .3 V	—	V_S^+ −.9 V	V
11	BW	Closed Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
12	SR	Slew Rate	$R_L = 10$ kΩ, $C_L = 50$ pf	—	2.5	—	—	2.5	—	V/μs
13	PSRR	Power Supply Rejection	$\pm 3.3 \le V_S \le \pm 5.5$ V	110	—	—	100	—	—	dB
14	V_S	Operating Supply Voltage Range (Note 3)		±3 V	—	±8 V	±3 V	—	±8 V	V
15	I_S	Quiescent Supply Current (Both Amplifiers)	$V_S = \pm 5$ V	—	0.65	0.85	—	—	1.1	mA

Notes:

1. Static Sensitive Device. Unused devices should be stored in conductive material.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.
3. Single Supply Operation: V_S^+ = +4.5 V to +16 V.
4. Advance product information.

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TELEDYNE SEMICONDUCTOR

TSC914
Quad Auto-Zeroed Operational Amplifier
• 15 μV Offset Voltage
• 1.5 mA Supply Current
• No External Capacitors Required

Advance Product Information

General Description

The TSC914 is the world's first complete monolithic quad auto-zeroed operational amplifier. The TSC914 sets a new standard for low power precision quad operational amplifiers. Chopper-stabilized or auto-zeroed amplifiers offer low offset voltage errors by periodically sampling offset error and storing correction voltages on capacitors. Previous single amplifier designs required two user supplied external 0.1 μF error storage correction capacitors — much too large for on-chip integration. The unique TSC914 architecture requires smaller capacitors making on-chip integration possible. Microvolt offset levels are achieved and **External Capacitors Are Not Required.**

The TSC914 system benefits are apparent when contrasted with a 7650 chopper amplifier circuit implementation. A single TSC914 replaces four 7650s and eight capacitors. Eleven components and assembly steps are eliminated.

The TSC914 pinout matches many popular quad operational amplifiers. The OP11, TLC274, LTC1014, LM348, and ICL7642/41 are typical examples. In many applications operating from dual five volt power supplies or single supplies, the TSC914 offers superior electrical performance and can be a functional, drop-in replacement. Printed circuit board rework is not necessary. The TSC914 low offset voltage error eliminates offset voltage trim potentiometers often needed with bipolar and low accuracy CMOS operational amplifiers.

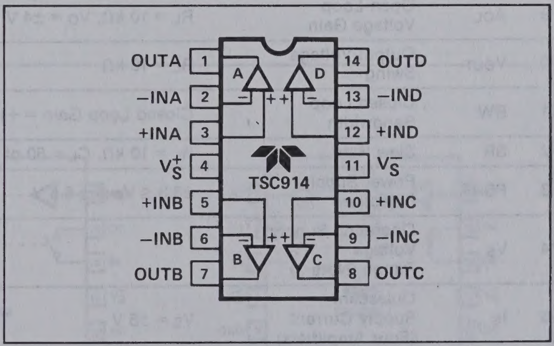
The TSC914 takes full advantage of Teledyne's proprietary CMOS technology. The TSC914 1.5 mA supply current (250 μA per amplifier) makes the TSC914 the lowest power, precision quad operational amplifier available. The 250 microampere amplifier supply current does not compromise AC performance. Unity gain bandwidth is 1.5 MHz and slew rate is 2.5 V/μs.

For single and dual operational amplifiers see the TSC911 and TSC913 data sheets.

Features

- First Monolithic Quad Auto-Zeroed Operational Amplifier
- Chopper Amplifier Performance Without External Capacitors
  - — 15 μV V_{OS}
  - — 0.15 μV/°C V_{OS} Drift
  - — Saves Cost/Assembly of Eight "Chopper" Capacitors
- High DC Gain .... 110 dB
- Low Supply Current .... 1.5 mA
- Wide Common-Mode Voltage Range .... V_S^- to V_S^+ −2 V
- High Common-Mode Rejection .... 110 dB
- Dual or Single Supply Operation .... ±3 V to ±8 V
+4.5 V to +16 V
- Excellent AC Operating Characteristics
  - — 2.5 V/μs Slew Rate
  - — 1.5 MHz Unity Gain Bandwidth
- Pin Compatible to LM348, TLC274, LM324, OP11, ICL7641/42

Pin Configuration



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Quad Auto-Zeroed Operational Amplifier

- 15 µV Offset Voltage
- 1.5 mA Supply Current
- No External Capacitors Required

TSC914

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-) .... 18 Volts
Input Voltage .... (V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range .... -55 °C to 150 °C
Lead Temperature (Soldering, 10 sec) .... 300 °C
Current into Any Pin .... 10 mA

Operating Temp. Range
I Device .... -25 °C to +85 °C
C Device .... 0 °C to +70 °C
Package Power Dissipation (T_A = 25 °C)
CerDIP Package .... 500 mW
Plastic Package .... 375 mW

Electrical Characteristics: V_S = ±5, T_A = 25°C unless otherwise indicated.

				TSC914A			TSC914B			
NO.	**SYMBOL**	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
1	V_{OS}	Input Offset Voltage	T_A = 25°C	—	5	15	—	15	30	µV
2	V_{OS}/T	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— —	0.05 0.05	0.15 0.15	— —	— —	0.25 0.25	µV/°C µV/°C
3	I_B	Average Input Bias Current	T_A = 25°C 0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— — —	— — —	90 3 4	— — —	— — —	120 4 6	pA nA nA
4	I_{OS}	Average Input	Offset Current	—	5	20	—	10	40	pA
5	e_n	Input Voltage Noise	0.1 to 1.0 Hz, R_S ≤ 100 Ω	—	0.6	—	—	0.6	—	$µV_{P-P}$
6	e_n	Input Voltage Noise	0.1 to 10 Hz, R_S ≤ 100 Ω	—	11	—	—	11	—	$µV_{P-P}$
7	CMRR	Common-Mode Rejection Ratio	V_S^- ≤ V_{CM} ≤ V_S^+ - 2.2 V	110	116	—	100	110		dB
8	CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+ -2.0	V_S^-	—	V_S^+ -2.0	V
9	A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_O = ±4 V	115	120	—	110	120	—	dB
10	V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^- + .3 V	—	V_S^+ -.9 V	V_S^- + .3 V	—	V_S^+ -.9 V	V
11	BW	Closed Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
12	SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pf	—	2.5	—	—	2.5	—	V/µs
13	PSRR	Power Supply Rejection	±3.3 ≤ V_S ≤ ± 5.5 V	110	—	—	100	—	—	dB
14	V_S	Operating Supply Voltage Range (Note 3)		±3 V	—	±8 V	±3 V	—	±8 V	V
15	I_S	Quiescent Supply Current (Four Amplifiers)	V_S = ±5 V	—	—	1.6	—	—	2.2	mA

Notes:
1. Static Sensitive Device. Unused devices should be stored in conductive material.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.
3. Single Supply Operation: V_S^+ = +4.5 V to +16 V.
4. Advance product information.

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TELEDYNE SEMICONDUCTOR

Advance Product Information

TSC4201/4202/4203
Low Cost CMOS Quad Analog Switches
• 300μA Supply Current
• 1 nA Leakage Current
• Single +5 V Supply Operation

General Description

The TSC4201, TSC4202 and TSC4203 are low leakage, low power CMOS quad SPST analog switches. Pin out matches the "201" analog switch configuration.

The TSC4201 and TSC4202 have opposite input logic polarity. The TSC4203, with two normally open and two normally closed switches, can be configured as a quad SPST, dual SPDT, DPDT, or dual DPST switch.

The family features single or dual power supply. Single +5 to +15 V or ±5 V operation is possible. Analog input voltage range equals the supply voltage. Power supply current is a low 300 μA. Leakage currents are a low 1 nA.

For devices with address data latches, see the TSC441, TSC442, and TSC443 product specifications.

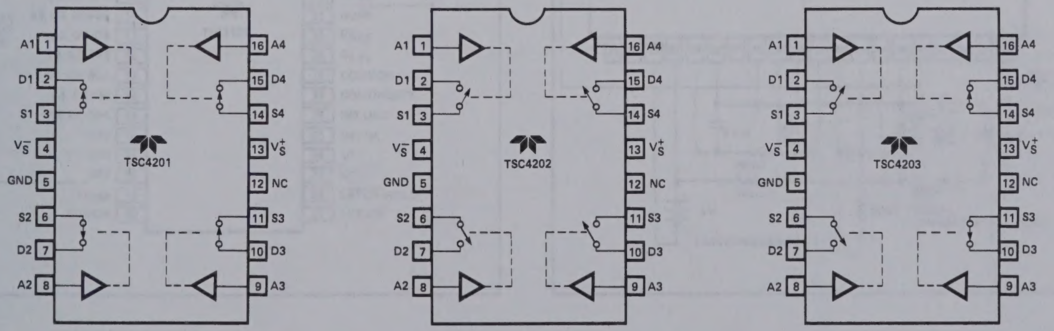
Features

- 300 μA Supply Current
- 120 Ω ON Resistance
- Low Input Leakage Current .... 1 nA
- Dual ±5 V or Single +5 to +15 V Supply Operation
- Analog Signal Range Equal to Supply Voltage
- TTL/CMOS Compatible Low Current Logic Input
- TSC4201: Pin Compatible to DG201
- TSC4202: Pin Compatible to DG202
- TSC4203: SPST, SPDT, DPST Configuration

Truth Table

A_N	TSC4201 Switch State	TSC4202 Switch State	TSC4203 Switch State
0	Closed	Open	SW1, SW2, Open SW3, SW4, Closed
1	Open	Closed	SW1, SW2, Closed SW3, SW4, Open

Pin Configuration



AN = 0, NC = No Internal Connection

Notes

TELEDYNE SEMICONDUCTOR

TSC7129
4 1/2 Digit ADC with Triplex LCD Display Drive

Advance Product Information

- **Single Chip**
- **10 μV Resolution**
- **Low Battery Detection**

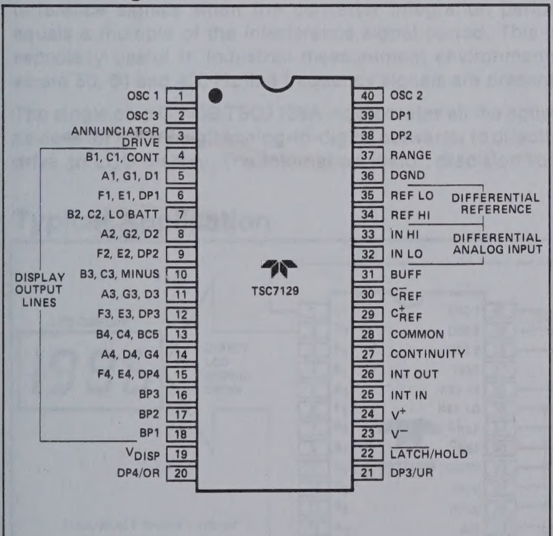
General Description

The TSC7129 4 1/2 digit single chip analog-to-digital converter directly drives multiplexed liquid crystal displays. External LCD drivers for decimal point, low battery, continuity, and polarity annunciators are not required. On-chip low battery detection, analog continuity adn 10 to 1 digital range change circuits eliminate external active components. Underrange and overrange outputs make autorange instruments possible.

Operating form conventional 9 V batteries or the compact VR22 9 V cell supply current is below 1 mA. With twelve external resistors/capacitors, 120 kHz crystal, TSC9491 bandgap reference, and LCD display a precision low cost 0.005% resolution instrument can be constructed.

For a compact surface mounted single chip 4 1/2 digit ADC see the TSC829 data sheet.

Pin Configuration

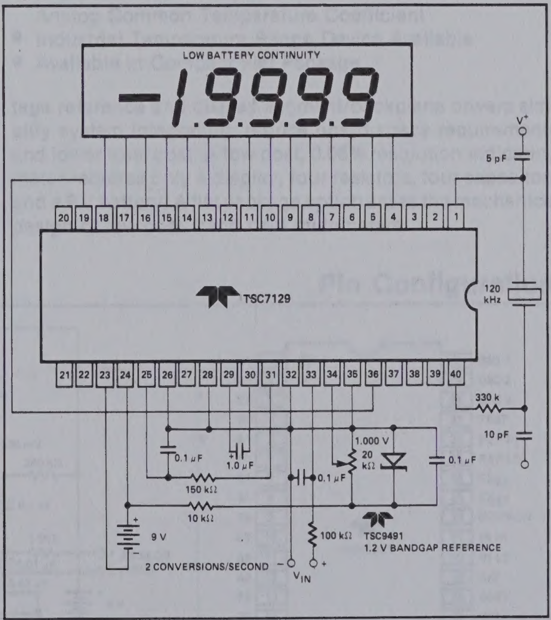


OSC 1 1
OSC 3 2
ANNUNCIATOR DRIVE 3
B1, C1, CONT 4
A1, G1, D1 5
F1, E1, DP1 6
B2, C2, LO BATT 7
A2, G2, D2 8
F2, E2, DP2 9
B3, C3, MINUS 10
A3, G3, D3 11
F3, E3, DP3 12
B4, C4, BC5 13
A4, D4, G4 14
F4, E4, DP4 15
BP3 16
BP2 17
BP1 18
V_DISP 19
DP4/OR 20
DISPLAY OUTPUT LINES
TSC7129
40 OSC 2
39 DP1
38 DP2
37 RANGE
36 DGND
35 REF LO
34 REF HI
DIFFERENTIAL REFERENCE
33 IN HI
32 IN LO
DIFFERENTIAL ANALOG INPUT
31 BUFF
30 C-REF
29 C+REF
28 COMMON
27 CONTINUITY
26 INT OUT
25 INT IN
24 V+
23 V−
22 LATCH/HOLD
21 DP3/UR

Features

- Single Chip 4 1/2 Digit ADC
- ± 19,999 Count Resolution
- Triplex LCD Display Drive
  - — Decimal Point, Low Battery Continuity and Polarity LCD Annunciators
- Low Battery Detection and LCD Annunciator
- Fast Analog Continuity Detection
- Differntial Reference and Signal Input
- 10 mW Power Dissipation
- Overrange/Underrange Outputs
- Digital Range Select
  - — 200 mV or 2 V Full-Scale
- Direct ICL7129 Replacement

Typical Configuration



LOW BATTERY CONTINUITY
-1.9.9.9.9
V+
5 pF
TSC7129
120 kHz
330 k
10 pF
0.1 µF
1.0 µF
150 kΩ
10 kΩ
0.1 µF
1.000 V
20 kΩ
0.1 µF
9 V
100 kΩ
TSC9491
1.2 V BANDGAP REFERENCE
2 CONVERSIONS/SECOND
V_IN

Notes

TELEDYNE SEMICONDUCTOR

Advance Product Information

TSC7136A

Low Power 3 1/2 Digit ADC with LCD Drive

- **Fast Overload Recovery**
- **Low Drift Internal Reference**
- **< 1 mW Power Dissipation**

General Description

The TSC7136A is a low power 3 1/2 Digit LCD display analog-to-digital converter. An improved internal zener reference voltage circuit reduces analog common temperature drift to 35 ppm/°C typically. This represents a 2 to 4 times improvement over similar 3 1/2 digit converters.

An integrator zero cycle eliminates overload recovery hangup. The auto-zero cycle guarantees a zero display reading for zero volt input.

The TSC7136A limits linearity error to less than 1 count on 200 mV or 2 V full-scale ranges. Rollover error (the difference in readings for equal magnitude but opposite polarity input signals) is below 1 count. High impedance differential inputs offer 1 pA leakage currents and a 10^{12} Ω input impedance. Ratiometric measurements for ohms or bridge transducer measurements are easy with the differential reference input. The low noise performance guarantees a "rock solid" reading.

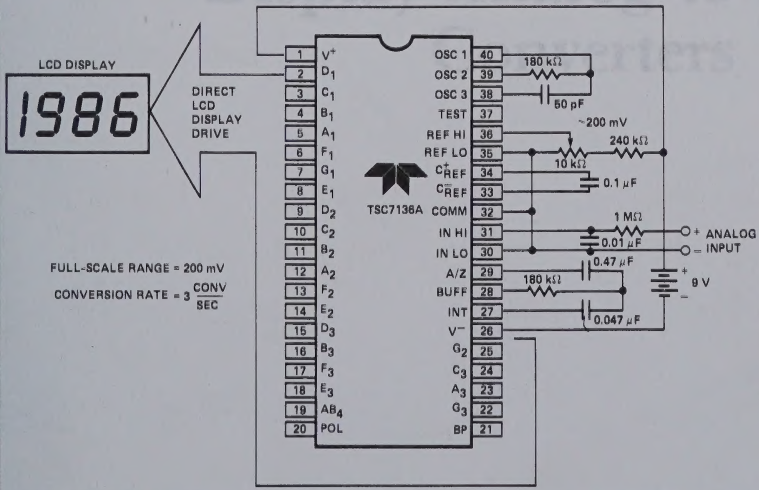
The TSC7136A dual slope conversion technique rejects interference signals when the converter integration period equals a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The single chip CMOS TSC7136A incorporates all the active devices for a 3 1/2 digit analog-to-digital converter to directly drive an LCD display. The internal oscillator, precision voltage reference and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, 0.05% resolution indicating meter requires only a display, four resistors, four capacitors and a 9 V battery. A flat package option eases the mechanical design of low cost, hand held multimeters.

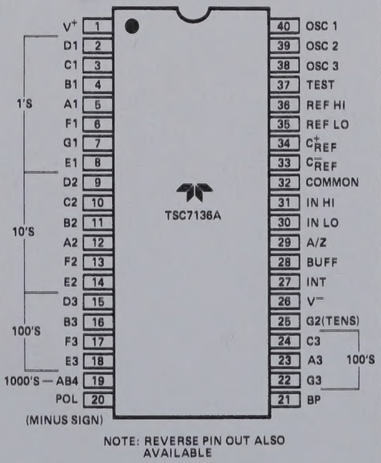
Features

- Fast Recovery from Overrange Input Signals
- Internal Reference With Low Temperature Drift .... 35 ppm/°C Typical
  75 ppm/°C Maximum
- Guaranteed Zero Reading With Zero Input
- Low Noise .... 15 μV_{p-p}
- High Resolution (0.05%) and Wide Dynamic Range (72 dB)
- Low Input Leakage Current .... 1 pA Typical
  10 pA Maximum
- Direct LCD Drive — No External Components
- Precision Null Detection With True Polarity at Zero
- High Impedance Differential Input
- Convenient 9 V Battery Operation With Low Power Dissipation .... 900 μW Maximum
- Internal Clock Circuit
- Improved Drop-In Replacement For ICL7136 with Low Analog Common Temperature Coefficient
- Industrial Temperature Range Device Available
- Available in Compact Flat Package

Typical Application


LCD DISPLAY
1986
DIRECT LCD DISPLAY DRIVE
FULL-SCALE RANGE = 200 mV
CONVERSION RATE = 3 CONV/SEC
TSC7136A
1 V+
2 D1
3 C1
4 B1
5 A1
6 F1
7 G1
8 E1
9 D2
10 C2
11 B2
12 A2
13 F2
14 E2
15 D3
16 B3
17 F3
18 E3
19 AB4
20 POL
40 OSC 1
39 OSC 2
38 OSC 3
37 TEST
36 REF HI
35 REF LO
34 C+REF
33 C−REF
32 COMM
31 IN HI
30 IN LO
29 A/Z
28 BUFF
27 INT
26 V−
25 G2
24 C3
23 A3
22 G3
21 BP
180 kΩ
50 pF
~200 mV
240 kΩ
10 kΩ
0.1 μF
1 MΩ
0.01 μF
+ ANALOG
− INPUT
0.47 μF
180 kΩ
9 V
0.047 μF

Pin Configuration


V+ 1
D1 2
C1 3
B1 4
A1 5
F1 6
G1 7
E1 8
D2 9
C2 10
B2 11
A2 12
F2 13
E2 14
D3 15
B3 16
F3 17
E3 18
1000'S — AB4 19
POL 20
(MINUS SIGN)
1'S
10'S
100'S
40 OSC 1
39 OSC 2
38 OSC 3
37 TEST
36 REF HI
35 REF LO
34 C+REF
33 C−REF
32 COMMON
31 IN HI
30 IN LO
29 A/Z
28 BUFF
27 INT
26 V−
25 G2(TENS)
24 C3
23 A3
22 G3
21 BP
100'S
TSC7136A
NOTE: REVERSE PIN OUT ALSO AVAILABLE

Notes

SECTION 7

Display Analog-to-Digital Converters

Section 7

Display A/D Converters 7-3

TSC500	Analog Processor for Microprocessor-Based A/D Converters	7-5
TSC805	3 1/2 Digit Auto-Ranging A/D Converter	7-7
TSC815	3 1/2 Digit Auto-Ranging A/D Converter with Display Hold	7-25
TSC826	A/D Converter with Bar-Graph Display Output	7-43
TSC7106A/7107A	3 1/2 Digit A/D Converter with Low Drift Reference	7-55
TSC7106/7107	3 1/2 Digit A/D Converter	7-73
TSC7116A/7117A	3 1/2 Digit A/D Converter with Low Drift Reference and Display Hold	7-85
TSC7116/7117	3 1/2 Digit A/D Converter with Display Hold	7-97
TSC7126A	Low Power 3 1/2 Digit A/D Converter with Low Drift Reference	7-109
TSC7126	Low Power 3 1/2 Digit A/D Converter	7-121
TSC7135	4 1/2 Digit Precision A/D Converter with BCD Output	7-133
TSC8750	3 1/2 Digit ADC with Parallel BCD Output	7-145
TSC14433A	Precision 3 1/2 Digit ADC with Multiplexed BCD Output	7-153
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TSC14433	3 1/2 Digit ADC with Multiplexed BCD Output	7-165

TELEDYNE SEMICONDUCTOR

See Section 8 For Full Specifications

TSC500
Analog Processor for Microprocessor-Based A/D Converters

General Description

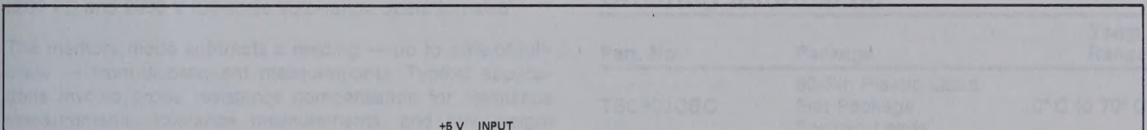
The TSC500 allows Microprocessor-Based A/D Converters for Display that offer many more features than an application-specific ADC can. See page 8-3 for complete details.

Applications

- The TSC500 Offers Flexibility!
- Under Software Control the User Selects:
  - — Speed
  - — Resolution
  - — Offset Correction
  - — Transfer Function (Output/Input)
- Leading to End Products Featuring:
  - — Auto-Ranging
  - — Auto-Tare (Scales)
  - — Transducer Linearization
  - — Complex Functions
  - — Intelligence

Features

- 4 Phase Dual Slope Converter Subsystem
  - — Auto-Zero Phase
  - — Signal Integrate Phase
  - — Reference Integrate Phase
  - — Integrator Zero Phase
  - — Fast Overload Recovery
- Excellent Linearity 0.005%
- Low Power .... 10 mW @ ±5 V Supplies
- High Input Sensitivity .... 100 µV
- Differential Analog Input
- Differential Reference Input for Ratiometric Measurement
- Low Input Current .... 15 pA Max.



+5 V
INPUT
+
−
−5 V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
TSC500
C_{REF}
V_{REF}
-12938
B_0 INTERRUPT
B_1
B_2
DISPLAY DRIVE
MICRO-COMPUTER
DATA ENTRY
1 2 3
4 5 6
7 8 9

TSC500/Microcomputer Display ADC

Notes

TELEDYNE SEMICONDUCTOR

TSC805
3 1/2 Digit Auto-Ranging Analog-to-Digital Converter
• Triplex LCD Drive
• Low Power CMOS

General Description

The TSC805 is a 3 1/2 digit integrating analog-to-digital converter with triplex LCD display drive and automatic ranging. Input voltage/ohm attenuators ranging from 1 to 1/10,000 are automatically selected. Five full-scale ranges are provided. The CMOS TSC805 contains all the logic and analog switches needed to manufacture an auto-ranging instrument for ohms and voltage measurements. User selected 20 mA and 200 mA current ranges are available. Full-scale range and decimal point LCD annunciators are automatically set in auto-range operation. Auto-range operation is available during ohms (high and low power ohms) and voltage (AC & DC) measurements. Auto-ranging eliminates expensive range switches in hand-held DMM designs and makes compact meters easier and less costly to design. The auto-range feature may be bypassed allowing decimal point selection and input attenuator selection control through a single line input. Expensive rotary switches are not required.

During manual mode operation resolution is extended to 3000 counts full-scale. The extended range operation is indicated by a flashing 1 MSD. The extended resolution is available during 2000 kΩ and 2000 V full-scale auto-range operation also.

The memory mode subtracts a reading — up to ±5% of full-scale — from subsequent measurements. Typical applications involve probe resistance compensation for resistance measurements, tolerance measurements, and tare weight measurement.

The TSC805 includes and AC to DC converter for AC measurements. Only external diodes/resistors/capacitors are required.

A complete LCD annunciator set describes the TSC805 meter function and measurement range during ohms, voltage and current operation. AC measurements are indicated as well as auto-range operation. A low battery detection circuit also sets the low battery display annunciator. The triplex LCD display drive levels may be set and temperature compensation applied via the V_{DISP} pin.

The "low ohms" measurement option allows in circuit resistance measurements by preventing semiconductor junctions from being forward biased.

A continuity buzzer output is activated with inputs less than 1% of full-scale. An overrange input signal also enables the buzzer, except during resistance measurements, and flashes the MSD display. Featuring single 9 V battery operation, 10 mW power consumption, a precision internal voltage reference (75 ppm/° C max. TC) and a compact surface mounted 60-pin quad flat package, the TSC805 is ideal for portable instruments.

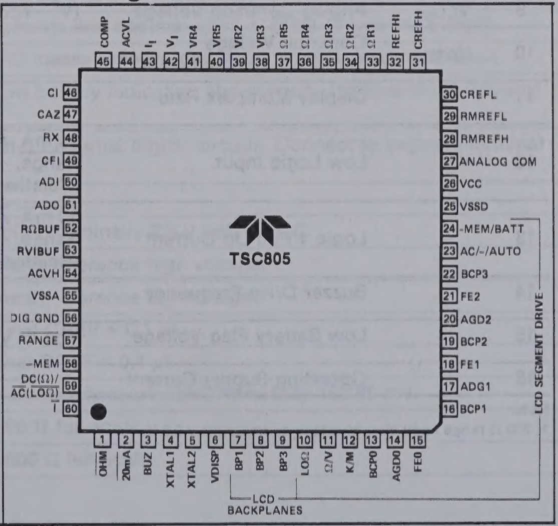
Features

- Auto-Range Operation for AC & DC Voltage and Resistance Measurements
  - — Two User Selected AC/DC Current Ranges 20 & 200 mA
- 22 Operating Ranges
  - — 9 DC/AC Voltage
  - — 4 AC/DC Current
  - — 9 Resistance and Low Power Ohms
- Low Cost Switches Control Operation
- 3 1/2 Digit Resolution in Auto-Range Mode 1/2000
  - — Extended Resolution in Manual Mode 1/3000
- Memory Mode for Relative Measurements ... ±5% F.S.
- Internal AC to DC Conversion Op Amp
- Triplex LCD Drive for Decimal Points, Digits and Annunciators
- Continuity Detection and Piezoelectric Transducer Driver
- Compact Surface Mounted 60-Pin Quad Flat Package
- Low Drift Internal Reference .... 75 ppm/° C
- 9 V Battery Operation
- Low Battery Detection and LCD Annunciator
- Low Power CMOS .... 10 mW

Ordering Information

Part. No.	Package	Temp. Range
TSC805CBQ	60-Pin Plastic Quad Flat Package Formed Leads	0° C to 70° C
TSC805CSQ	60-Pin Plastic Quad Flat Package Straight Leads	0° C to 70° C

Pin Configuration


COMP 45
ACVL 44
I_I 43
V_I 42
VR4 41
VR5 40
VR2 39
VR3 38
ΩR5 37
ΩR4 36
ΩR3 35
ΩR2 34
ΩR1 33
REFHI 32
CREFH 31
CI 46
CAZ 47
RX 48
CFI 49
ADI 50
ADO 51
RΩBUF 52
RVIBUF 53
ACVH 54
VSSA 55
DIG GND 56
$\overline{\text{RANGE}}$ 57
–MEM 58
DC(Ω)/ $\overline{\text{AC}}$($\overline{\text{LOΩ}}$) 59
$\overline{\text{I}}$ 60
30 CREFL
29 RMREFL
28 RMREFH
27 ANALOG COM
26 VCC
25 VSSD
24 –MEM/BATT
23 AC/–/AUTO
22 BCP3
21 FE2
20 AGD2
19 BCP2
18 FE1
17 ADG1
16 BCP1
TSC805
1 $\overline{\text{OHM}}$
2 $\overline{\text{20mA}}$
3 BUZ
4 XTAL1
5 XTAL2
6 VDISP
7 BP1
8 BP2
9 BP3
10 LOΩ
11 Ω/V
12 K/M
13 BCP0
14 AGD0
15 FE0
LCD BACKPLANES
LCD SEGMENT DRIVE

©1984

Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) .... 15 V
Analog Input Voltage .... V^+ to V^-
Reference Input Voltage .... V^+ to V^-
Voltage at Pin 43 .... GND ±0.7 V
Power Dissipation
Plastic Package .... 800 mW
Operating Temperature
"C" Devices .... 0°C to +70°C

Storage Temperature .... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) .... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

Electrical Characteristics: V_S = 9 V, T_A = 25°C, Figure 1 Test Circuit

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC805 MIN	TSC805 TYP	TSC805 MAX	UNIT
1		Zero Input Reading	200 mV Range w/o 10 MΩ Input Resistor	-0000	0000	+0000	Digital Reading
			200 mV Range w/10 MΩ Input	-0001	—	+0001	
			20 mA and 200 mA Range	-0000	0000	+0000	
2	RE	Rollover Error	200 mV Range w/o 10 MΩ Input Resistor	—	—	±1	Count
			200 mV Range w/10 MΩ Input	—	—	±3	
			20 mA and 200 mA Range	—	—	±1	
3	NL	Linearity Error	Best Case Straight Line	—	—	±1	Count
4	I_{IN}	Input Leakage Current		—	—	10	pA
5	E_N	Input Noise	BW = 0.1 to 10 Hz	—	20	—	μV_{p-p}
6		AC Frequency Response	±1% Error	—	40 to 500	—	Hz
			±5% Error	—	40 to 2000	—	
7		Open Circuit Voltage for OHM Measurements	Excludes 200 Ω Range	—	570	660	mV
8		Open Circuit Voltage for LO OHM Measurement	Excludes 200 Ω Range	—	285	350	mV
9	V_{COM}	Analog Common Voltage	(V^+ -V_{COM})	2.5	2.6	3.3	V
10	V_{CTC}	Common Voltage Temperature Coefficient		—	—	50	ppm/°C
11		Display Multiplex Rate		—	100	—	Hz
12	V_{IL}	Low Logic Input	$\overline{20\text{ mA}}$, $\overline{AC}$, $\overline{I}$, $\overline{\text{Low }\Omega}$, Range, -MEM, $\overline{\text{OHMs}}$ (Relative to DIG GND Pin 56)	—	—	1	V
13		Logic 1 Pull Up Current	$\overline{20\text{ mA}}$, $\overline{AC}$, $\overline{I}$, $\overline{\text{Low }\Omega}$, Range, -MEM, $\overline{\text{OHMs}}$ (Relative to DIG GND Pin 56)	—	25	—	μA
14		Buzzer Drive Frequency		—	4	—	kHz
15		Low Battery Flag Voltage	V_{CC} to V_{SSA}	6.3	6.6	7.0	V
16		Operating Supply Current		—	0.8	1.5	mA

Note:
1. 200 Ω range open circuit voltage approximately 2.8 V.

Pin Description and Function Table 1:

PIN NO. (Quad Flat Package)	SYMBOL	DESCRIPTION
1	$\overline{\text{OHM}}$	Logic Input. "0" (Digital Ground) for resistance measurement.
2	$\overline{\text{20 mA}}$	Logic Input. "0" (Digital Ground) for 20 mA full-scale current measurement.
3	BUZ	Audio frequency, 4 kHz, output for continuity indication during resistance measurement. A non-continuous 4 kHz signal is output to indicate an input overrange during voltage or current measurements.
4	XTAL1	32.768 kHz Crystal Connection.
5	XTAL2	32.768 kHz Crystal Connection.
6	VDISP	Sets peak LCD drive signal: VP = VCC-VDISP. VDISP may also be used to compensate for temperature variation of LCD crystal threshold voltage.
7	BP1	LCD Backplane #1.
8	BP2	LCD Backplane #2.
9	BP3	LCD Backplane #3.
10	Low Ω/A	LCD Annunciator segment drive for low ohms resistance measurement and current measurement.
11	Ω/V	LCD Annunciator segment drive for resistance measurement and voltage measurement.
12	K/m	LCD Annunciator segment drive for k ("kilo-ohms") and m ("milli-amps" and "milli-volts").
13	BCP0 (Ones digit).	LCD segment drive for "b," "c" segments and decimal point of least significant digit (LSD).
14	AGD0	LCD segment drive for "a," "g," "d" segments of LSD.
15	FE0	LCD segment drive for "f" and "e" segments of LSD.
16	BCP1	LCD segment drive for "b," "c" segments and decimal point of 2nd LSD.
17	AGD1	LCD segment drive for "a," "g," "d" segments of 2nd LSD (Ten's digit).
18	FE1	LCD segment drive for "f," and "e" segments of 2nd LSD.
19	BCP2	LCD segment drive for "b," "c," and decimal point of 3rd LSD. (Hundreds digit).
20	AGD2	LCD segment drive for "a," "g," "d" segments of 3rd LSD.
21	FE2	LCD segment drive for "b" and "c" segments of 3rd LSD.
22	BCP3	LCD segment drive for "b," "c" segments and decimal point of MSD (Thousand's digit).
23	AC/-/AUTO	LCD annunciator drive signal for AC measurements, polarity, and auto-range operation.
24	-MEM/BATT mode.	LCD annunciator drive signal for low battery indication and memory (relative measurement)
25	VSSD	Negative battery supply connection for internal digital circuits. Connect to negative terminal of battery.
26	VCC	Positive battery supply connection.
27	COM	Analog circuit ground reference point. Nominally 2.6 V below VCC.
28	RMREFH	Ratiometric (Resistance measurement) reference high voltage.
29	RMREFL	Ratiometric (Resistance measurement) reference low voltage.
30	CREFL	Reference capacitor negative terminal CREF = 0.1 μf.
31	CREFH	Reference capacitor positive terminal CREF = 0.1 μf.
32	REFHI	Reference voltage for voltage and current measurement. Nominally 163.85 mV.
33	ΩR1	Standard resistor connection for 200 Ω full-scale.
34	ΩR2	Standard resistor connection for 2000 Ω full-scale.

Pin Description and Function Cont.

PIN NO. (Quad Flat Package)	SYMBOL	DESCRIPTION
35	ΩR3	Standard resistor connection for 20 kΩ full-scale range.
36	ΩR4	Standard resistor connection for 200 kΩ full-scale range.
37	ΩR5	Standard resistor connection for 2000 kΩ full-scale range.
38	VR3	Voltage measurement ÷ 100 attenuator.
39	VR2	Voltage measurement ÷ 10 attenuator.
40	VR5	Voltage measurement ÷ 10,000 attenuator.
41	VR4	Voltage measurement ÷ 1000 attenuator.
42	V_I	Unknown voltage input ÷ 1 attenuator.
43	I_I	Unknown current input.
44	ACVL	Low output of AC to DC converter.
45	COMP	Comparator output.
46	CI	Integrator capacitor connection. Nominally 0.1 μf. (Low dielectric absorption. Polypropylene dielectric suggested).
47	CAZ	Auto-zero capacitor connection. Nominally 0.1 μf.
48	Rx	Unknown resistance input.
49	CFI	Input filter connection.
50	ADI	Negative input of internal AC to DC operational amplifier.
51	ADO	Output of internal AC to DC operational amplifier.
52	RΩBUF	Active buffer output for resistance measurement. Integration resistor connection. Integrator resistor nominally 220 kΩ.
53	RVIBUF	Active buffer output for voltage and current measurement. Integration resistor connection. Integration resistor nominally 150 kΩ.
54	ACVH	Positive output of AC to DC converter.
55	VSSA	Negative supply connection for analog circuits. Connect to negative terminal of 9 V battery.
56	DIG GND	Internal logic digital ground. The logic "0" level. Nominally 4.7 V below VCC.
57	$\overline{\text{RANGE}}$	Input to set manual operation and change ranges.
58	$\overline{\text{MEM}}$	Input to enter memory measurement mode for relative measurements. The two LSD's are stored and subtracted from future measurements.
59	DC/$\overline{\text{AC}}$, Ω/LOW Ω	Input that selects AC or DC option during voltage/current measurements. For resistance measurements, the ohms or low power (voltage) ohms option can be selected.
60	$\overline{\text{I}}$	Input to select current measurement. Set to logic "0" (Digital ground) for current measurement.

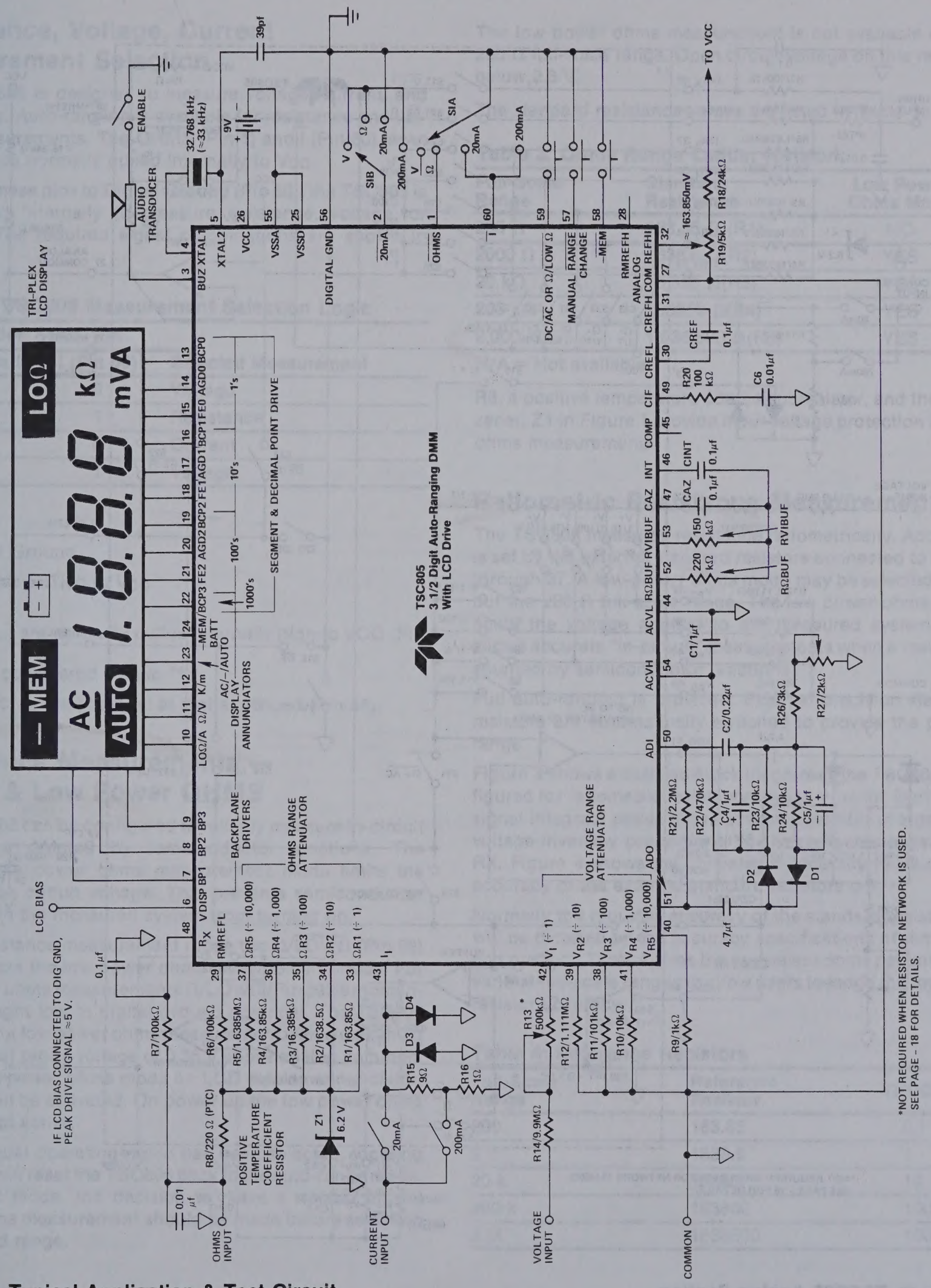
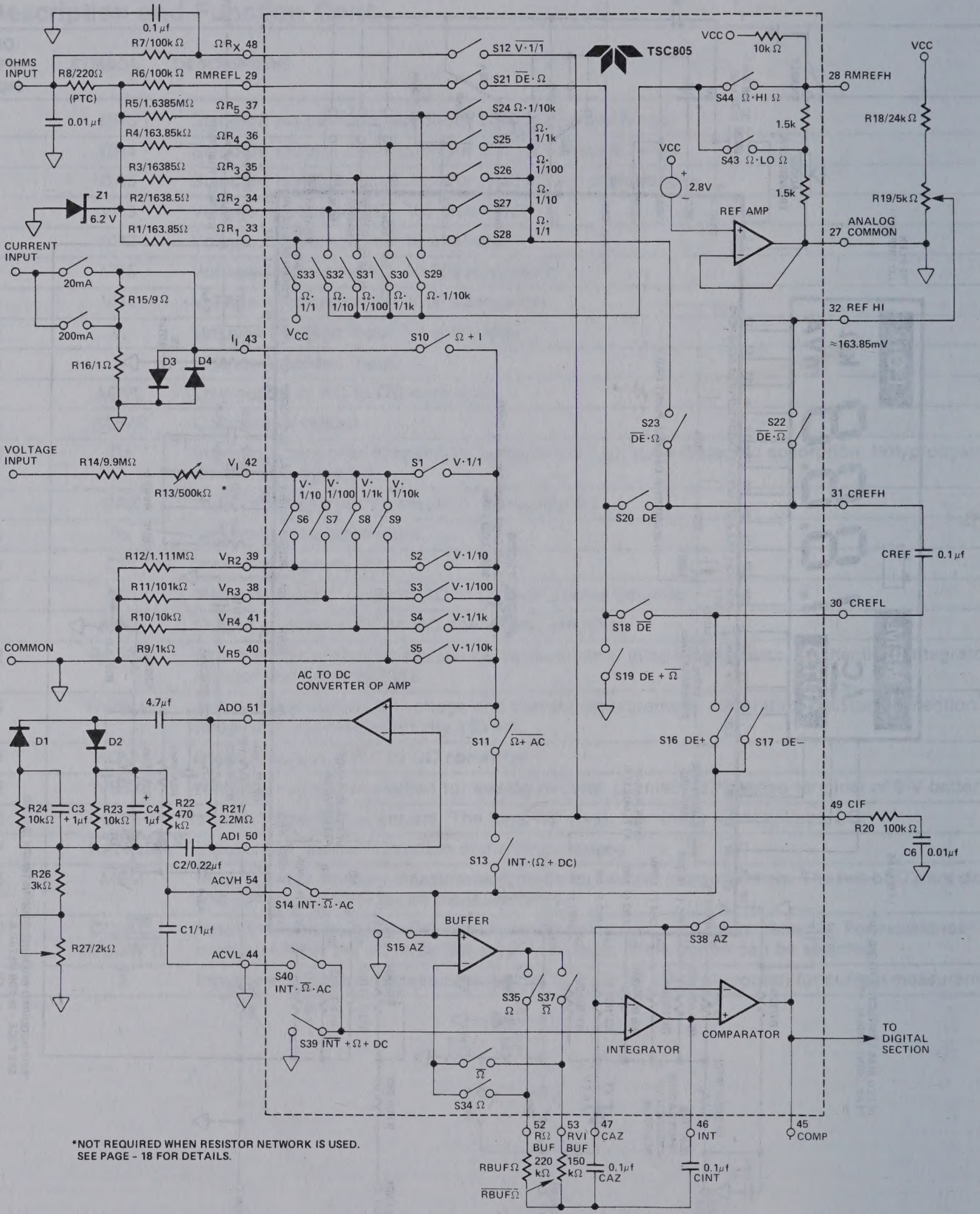

TSC805
3 1/2 Digit Auto-Ranging DMM
With LCD Drive
TRI-PLEX LCD DISPLAY
– MEM
AC
AUTO
LOΩ
kΩ
mVA
1.8.8.8
AUDIO TRANSDUCER
ENABLE
32.768 kHz (≈33 kHz)
39pf
9V
SIB
SIA
V
Ω
20mA
200mA
BUZ XTAL1
XTAL2
VCC
VSSA
VSSD
DIGITAL GND
20mA
OHMS
DC/AC OR Ω/LOW Ω
MANUAL RANGE CHANGE
–MEM
RMREFH
ANALOG CREFH COM REFHI
CREFL
CIF
COMP
INT
CAZ
RVIBUF
RΩBUF
ACVL
ACVH
ADI
ADO
RX RMREFL
ΩR5 (÷ 10,000)
ΩR4 (÷ 1,000)
Ω R3 (÷ 100)
ΩR2 (÷ 10)
ΩR1 (÷ 1)
II
VI (÷ 1)
VR2 (÷ 10)
VR3 (÷ 100)
VR4 (÷ 1,000)
VR5 (÷ 10,000)
VDISP BP1 BP2 BP3
BACKPLANE DRIVERS
LOΩ/A Ω/V K/m AC/–/AUTO –MEM/BCP3 BATT
DISPLAY ANNUNCIATORS
FE2 AGD2 BCP2 FE1 AGD1 BCP1 FE0 AGD0 BCP0
1000's 100's 10's 1's
SEGMENT & DECIMAL POINT DRIVE
OHMS RANGE ATTENUATOR
VOLTAGE RANGE ATTENUATOR
LCD BIAS
IF LCD BIAS CONNECTED TO DIG GND, PEAK DRIVE SIGNAL ≈5 V.
0.1μf
R7/100kΩ
R6/100kΩ
R5/1.6385MΩ
R4/163.85kΩ
R3/16.385kΩ
R2/1638.5Ω
R1/163.85Ω
R8/220 Ω (PTC)
POSITIVE TEMPERATURE COEFFICIENT RESISTOR
Z1 6.2 V
D3
D4
R15 9Ω
R16 1Ω
R13* 500kΩ
R12/1.111MΩ
R11/101kΩ
R10/10kΩ
R14/9.9MΩ
R9/1kΩ
0.01 μf
OHMS INPUT
CURRENT INPUT
VOLTAGE INPUT
COMMON
20mA
200mA
4.7μf
R21/2.2MΩ
R22/470kΩ
C4/1μf
R23/10kΩ
R24/10kΩ
C5/1μf
D1
D2
C2/0.22μf
R26/3kΩ
R27/2kΩ
C1/1μf
220 kΩ
150 kΩ
CAZ 0.1μf
CINT 0.1μf
R20 100 kΩ
C6 0.01μf
CREF 0.1μf
R19/5kΩ
R18/24kΩ
≈ 163.850mV
TO VCC
*NOT REQUIRED WHEN RESISTOR NETWORK IS USED. SEE PAGE - 18 FOR DETAILS.

Figure 1: Typical Application & Test Circuit


0.1 μf
R7/100k Ω
ΩR$_X$ 48
OHMS INPUT
R8/220Ω
(PTC)
R6/100k Ω
RMREFL 29
0.01 μf
R5/1.6385MΩ
ΩR$_5$ 37
R4/163.85kΩ
ΩR$_4$ 36
R3/16385Ω
ΩR$_3$ 35
Z1
6.2 V
R2/1638.5Ω
ΩR$_2$ 34
R1/163.85Ω
ΩR$_1$ 33
S12 V·1/1
S21 DE·Ω
S24 Ω·1/10k
S25
Ω·1/1k
S26
Ω·1/100
S27
Ω·1/10
S28
Ω·1/1
TSC805
VCC
10k Ω
S44 Ω·HI Ω
28 RMREFH
1.5k
S43 Ω·LO Ω
1.5k
2.8V
REF AMP
VCC
R18/24k Ω
R19/5k Ω
ANALOG
27 COMMON
CURRENT INPUT
20mA
R15/9 Ω
200mA
S33 S32 S31 S30 S29
Ω·1/1
Ω·1/10
Ω·1/100
Ω·1/1k
Ω·1/10k
V$_{CC}$
32 REF HI
≈163.85mV
R16/1Ω
D3
D4
I$_I$ 43
S10
Ω + I
S23
DE·Ω
S22
DE·Ω
VOLTAGE INPUT
R14/9.9MΩ
R13/500kΩ
V$_I$ 42
S1
V·1/1
V·1/10
V·1/100
V·1/1k
V·1/10k
S6 S7 S8 S9
S20 DE
31 CREFH
CREF
0.1 μf
R12/1.111MΩ
V$_{R2}$ 39
S2 V·1/10
R11/101kΩ
V$_{R3}$ 38
S3 V·1/100
R10/10kΩ
V$_{R4}$ 41
S4 V·1/1k
30 CREFL
S18 DE
COMMON
R9/1kΩ
V$_{R5}$ 40
S5 V·1/10k
S19 DE + Ω
AC TO DC
CONVERTER OP AMP
4.7μf
ADO 51
D1
D2
S11
Ω + AC
S16 DE+
S17 DE−
R24 10kΩ
C3 1μf
R23 10kΩ
C4 1μf
R22 470 kΩ
R21/2.2MΩ
ADI 50
49 CIF
R20 100k Ω
C6 0.01μf
R26 3kΩ
C2/0.22μf
S13
INT·(Ω + DC)
ACVH 54
S14 INT·Ω·AC
C1/1μf
BUFFER
S38 AZ
S15 AZ
R27/2kΩ
ACVL 44
S40 INT·Ω·AC
S35 Ω
S37 Ω
S39 INT + Ω + DC
INTEGRATOR
COMPARATOR
TO DIGITAL SECTION
Ω
S34 Ω
52 RΩ BUF
53 RVI BUF
47 CAZ
46 INT
45 COMP
RBUFΩ
220 kΩ
150 kΩ
0.1μf CAZ
0.1μf CINT
RBUFΩ

*NOT REQUIRED WHEN RESISTOR NETWORK IS USED. SEE PAGE - 18 FOR DETAILS.

Figure 2: TSC805 Analog Section

Resistance, Voltage, Current Measurement Selection

The TSC805 is designed to measure voltage, current, and resistance. Auto-ranging is available for resistance and voltage measurements. The $\overline{\text{OHMS}}$ (Pin 1) and $\overline{\text{I}}$ (Pin 60) input controls are normally pulled internally to V_{CC}.

By tying these pins to Digital Ground (Pin 56), the TSC805 is configured internally to measure resistance, voltage, or current. The required signal combinations are shown in Table 2.

Table 2: TSC805 Measurement Selection Logic

Function Select Pin		
$\overline{\text{OHM}}$ (Pin 1)	$\overline{\text{I}}$ (Pin 60)	Selected Measurement
0	0	Voltage
0	1	Resistance
1	0	Current
1	1	Voltage

0 = Digital Ground

1 = Floating or Tied to Vcc

Notes:

1. $\overline{\text{OHM}}$ & $\overline{\text{I}}$ are normally pulled internally high to VCC (Pin 26).
   This is considered a logic "1."
2. Logic "0" is the potential at digital ground (Pin 56).

Resistance Measurements — OHMS & Low Power OHMS

The TSC805 can be configured to reliably measure in-circuit resistances shunted by semiconductor junctions. The TSC805 low power ohms measurement mode limits the probe open circuit voltage. This prevents semiconductor junctions in the measured system from turning on.

In the resistance measurement mode the Ω/$\overline{\text{LOW}\Omega}$ (Pin 59) input selects the low power ohms measurement mode. For low power ohms measurements Ω/$\overline{\text{LOW}\Omega}$ (Pin 59) is momentarily brought low to digital ground potential. The TSC805 sets up for a low power ohms measurement with a maximum open circuit probe voltage of 0.35 V above analog common. In the low power ohms mode an LCD display annunciator, LOW Ω, will be activated. On power up the low power ohms mode is not active.

If the manual operating mode has been selected, toggling Ω/$\overline{\text{LOW}\Omega}$ will reset the TSC805 back to the auto-range mode. In manual mode, the decision to make a normal or low power ohms measurement should be made before selecting the desired range.

The low power ohms measurement is not available on the 200 Ω full-scale range. Open circuit voltage on this range is below 2.8 V.

The standard resistance values are listed in Table 3.

Table 3: Ohms Range Ladder Network

Full-Scale Range	Standard Resistance	Low Power Ohms Mode
200 Ω	163.85 Ω (R1)	NO
2000 Ω	1638.5 Ω(R2)	YES
20 kΩ	16,358 Ω(R3)	YES
200 kΩ	163850 Ω(R4)	YES
2,000 kΩ	1,638,500 Ω(R5)	YES

N/A = Not available.

R8, a positive temperature coefficient resistor, and the 6.2 V zener, Z1 in Figure 1 provide input voltage protection during ohms measurements.

Ratiometric Resistance Measurements

The TSC805 measures resistance ratiometrically. Accuracy is set by the external standard resistors connected to Pin 33 through 37. A low-power ohms mode may be selected on all but the 200 Ω full-scale range. The low power ohms mode limits the voltage applied to the measured system. This allows accurate "in-circuit" measurements when a resistor is shunted by semiconductor junctions.

Full auto-ranging is provided. External precision standard resistors are automatically switched to provide the proper range.

Figure 3 shows a detailed block diagram of the TSC805 configured for ratiometric resistance measurements. During the signal integrate phase the reference capacitor charges to a voltage inversely proportional to the measured resistance-RX. Figure 4 shows the conversion accuracy relies on the accuracy of the external standard resistors only.

Normally the required accuracy of the standard resistances will be dictated by the accuracy specifications of the users end product. Table 4 gives the equivalent ohms per count for various full-scale ranges to allow users to judge the required resistor accuracy.

Table 4: Reference Resistors

Full-Scale Range	Reference Resistor	Ω/COUNT
200	163.85	0.1
2 k	1638.5	1
20 k	16385	10
200 k	163850	100
2 M	1638500	1000

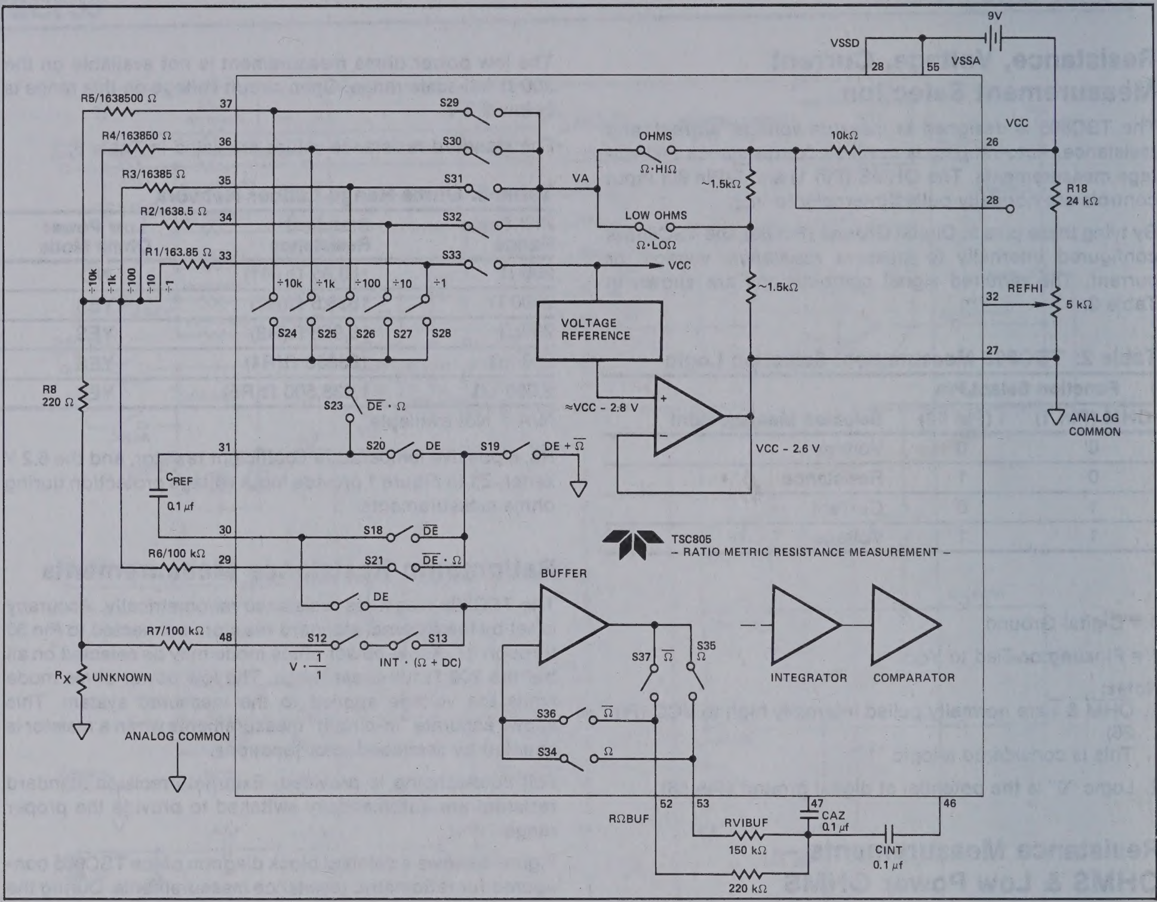

9V
VSSD
28
55
VSSA
R5/1638500 Ω
37
S29
R4/163850 Ω
36
S30
OHMS
Ω·HIΩ
10kΩ
VCC
26
R3/16385 Ω
35
S31
VA
~1.5kΩ
R18
24 kΩ
28
R2/1638.5 Ω
34
S32
LOW OHMS
Ω·LOΩ
R1/163.85 Ω
33
S33
VCC
÷10k
÷1k
÷100
÷10
÷1
÷10k
÷1k
÷100
÷10
÷1
~1.5kΩ
REFHI
32
5 kΩ
S24
S25
S26
S27
S28
VOLTAGE REFERENCE
27
R8
220 Ω
S23
DE · Ω
≈VCC - 2.8 V
ANALOG COMMON
31
S20
DE
S19
DE + Ω
VCC - 2.6 V
CREF
0.1 µf
30
S18
DE
TSC805
– RATIO METRIC RESISTANCE MEASUREMENT –
R6/100 kΩ
29
S21
DE · Ω
BUFFER
DE
R7/100 kΩ
48
S12
S13
V · 1/1
INT · (Ω + DC)
S37
Ω
S35
Ω
INTEGRATOR
COMPARATOR
RX
UNKNOWN
S36
Ω
ANALOG COMMON
S34
Ω
52
53
47
46
RΩBUF
RVIBUF
CAZ
0.1 µf
150 kΩ
CINT
0.1 µf
220 kΩ

Figure 3: Ratiometric Resistance Measurement Functional Diagram

Voltage Measurement

Resistive dividers are automatically changed to provide in range readings for 200 mV to 2000 V full-scale readings (Figure 2). The input resistance is set by external resistors R14/R13. The divider leg resistors are R9-R12. The divider leg resistors give a 200 mV signal at VI (Pin 42) for full-scale voltages from 200 mV to 2000 V.

For applications which do not require a 10 MΩ input impedance the divider network impedances may be lowered. This will reduce voltage offset errors induced by switch leakage currents.

Current Measurement

The TSC805 measures current only under manual range operation. The two user selectable full-scale ranges are: 20 mA and 200 mA. Select the current measurement mode by holding the $\overline{I}$ input (Pin 60) low at digital ground potential. The OHM input (Pin 1) is left floating or tied to the positive supply.

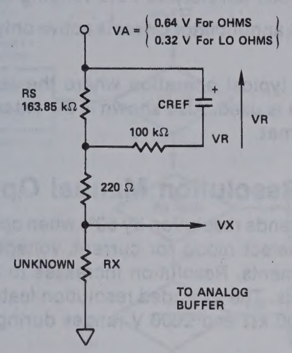
Two ranges are possible. The 20 mA full-scale range is selected by connecting the $\overline{20\text{ mA}}$ input (Pin 2) to digital ground. If left floating the 200 mA full-scale range is selected.

External current to voltage conversion resistors are used at the I_I input (Pin 43). For 20 mA measurements a 10 Ω resistor is used. the 200 mA range needs a 1 Ω resistor. Full-scale is 200 mV.

PC board trace resistance between analog common and R16 (See Figure 1) must be minimized. In the 200 mA range, for example, a 0.05 Ω trace resistance will cause a 5% current to voltage conversion error at I_I (Pin 43).

The extended resolution measurement option operates during current measurements.

To minimize rollover error the potential difference between analog common (Pin 27) and system common must be minimized.


VA = 0.64 V For OHMS
0.32 V For LO OHMS
RS
163.85 kΩ
CREF
+
100 kΩ
VR
VR
220 Ω
VX
UNKNOWN
RX
TO ANALOG
BUFFER

Example: 200 kΩ Full-Scale Measurement

(a) $$VR = \frac{163.85\ \text{k}\Omega}{163.85 + 220 + RX} \times 0.64$$

(b) $$VX = \frac{RX}{163.85\ \text{k}\Omega + 220\ \Omega + RX} \times 0.64$$

(c) "Ramp Up Voltage" = "Ramp Down Voltage"

$$\therefore \frac{VX}{R_I C_I} \times T_I = \frac{VR}{R_I C_I} T_{DE}$$

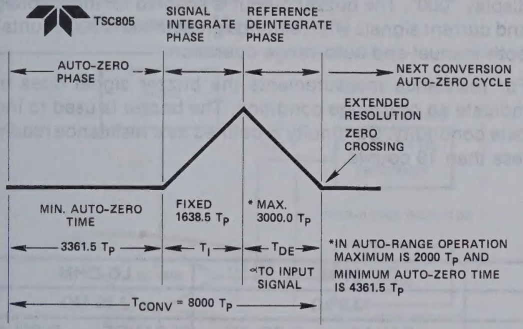
Where:

R_I = Integrating Resistor, T_I = Integrate Time
C_I = Integrating Capacitor, T_{DE} = Deintegrate Time

(d) $$RX = 163.85 \left(\frac{T_{DE}}{T_I} \right)$$

Independent of R_I, C_I or Internal Voltage Reference

Figure 4: Resistance Measurement Accuracy Set by External Standard Resistor


TSC805
SIGNAL
INTEGRATE
PHASE
REFERENCE
DEINTEGRATE
PHASE
AUTO-ZERO
PHASE
NEXT CONVERSION
AUTO-ZERO CYCLE
EXTENDED
RESOLUTION
ZERO
CROSSING
MIN. AUTO-ZERO
TIME
FIXED
1638.5 T_P
* MAX.
3000.0 T_P
3361.5 T_P
T_I
T_DE
∝TO INPUT
SIGNAL
*IN AUTO-RANGE OPERATION
MAXIMUM IS 2000 T_P AND
MINIMUM AUTO-ZERO TIME
IS 4361.5 T_P
T_CONV = 8000 T_P

External Crystal = 32.768 kHz
Internal Clock Period = T_P = 2/32.768 = 61.04 μs
Total Conversion Time = T_{CONV} = 8000 (T_P)
= 488.3 ms ≈ 2 CONV/SEC
Integration Time = T_I = 1638.5 (T_P) = 100.0 ms
Maximum Reference Deintegrate Time
= T_{DE} = 3000 (T_P) = 183.1 ms (Manual, Extended Resolution)
= 2000 (T_P) = 122.1 ms (Auto-Range)
Minimum Auto-Zero Time
= (8000–3000–1638.5) (T_P) = 205.1 ms (Manual, Extended Resolution)
= (8000–2000–1638.5) (T_P) = 266.2 ms (Auto-Range)

Figure 5: Basic TSC805 Conversion Timing

Measurement Options
AC to DC Measurements

In voltage and current measurements the TSC805 can be configured for AC measurements. An on chip operational amplifier and external rectifier components perform the AC to DC conversion.

When power is first applied the TSC805 enters the DC measurement mode. For AC measurements (current or voltage), $\overline{\text{AC}}$/DC (Pin 59) is momentarily brought low to digital ground potential; the TSC805 sets-up for AC measurements and the AC liquid crystal display annunciator activates. Toggling $\overline{\text{AC}}$/DC low again will return the TSC805 to DC operation.

If the manual operating mode has been selected toggling AC/DC will reset the TSC805 back to the auto-range mode. In manual mode operation AC or DC operation should be selected first and then the desired range selected.

The minimum AC voltage full-scale voltage range is 2 V. The DC full-scale minimum voltage is 200 mV.

AC current measurements are available on the 20 mA and 200 mA full-scale current range.

Conversion Timing

The TSC805 analog-to-digital converter uses the conventional dual slope integrating conversion technique with an added phase that automatically eliminates zero offset errors. The TSC805 gives a zero reading with a zero volt input.

The TSC805 is designed to operate with a 32.768 kHz crystal. The 32 kHz crystal is low cost and readily available; it serves as a time base oscillator crystal in many digital clocks. (See External Crystal Sources.)

The external clock is divided by two. The internal clock frequency is 16.348 kHz giving a clock period of 61.04 μs. The total conversion — auto-zero phase, signal integrate and reference deintegrate — requires 8000 clock periods or 488.3 ms. There are approximately two complete conversions per second.

The integration time is fixed at 1638.5 clock periods or 100 ms. This gives rejection of 50/60 Hz AC line noise.

The maximum reference deintegrate time, representing a full-scale analog input, is 3000 clock periods or 183.1 ms during manual extended resolution operation. The 3000 counts are available in manual mode, extended resolution operation only. In auto-ranging mode the maximum deintegrate time is 2000 clock periods. The 1000 clock periods are added to the auto-zero phase. An auto-ranging or manual conversion takes 8000 clock periods. After a zero crossing is detected in the reference deintegrate mode, the auto-zero phase is entered.

Figure 5 shows the basic TSC805 timing relationships.

Manual Range Selection

The TSC805 voltage and resistance auto-ranging feature can be disabled by momentarily bringing $\overline{\text{RANGE}}$ (Pin 57) to digital ground potential (Pin 56). When the change from auto-to-manual ranging occurs the first manual range selected is the last range in the auto-ranging mode.

The TSC805 power-up circuit selects auto-range operation initially. Once the manual range option is entered, range changes are made my momentarily grounding the RANGE control input. The TSC805 remains in the manual range mode until the measurement function (voltage or resistance) or measurement option (AC/DC, Ω/LO Ω) changes. This causes the TSC805 to return to auto-ranging operation.

The "Auto" LCD annunciator driver is active only in the auto-range mode.

Table 5 shows typical operation where the manual range selection option is used. Also shown is the extended resolution display format.

Extended Resolution Manual Operation

The TSC805 extends resolution by 50% when operated in the manual range select mode for current, voltage, and resistance measurements. Resolution increases to 3000 counts from 2000 counts. The extended resolution feature operates only on the 2000 kΩ and 2000 V ranges during auto-range operation.

In the extended resolution operating mode readings above 1999 are displayed with a blinking "1" most significant digit. The blinking "1" should be interpreted as the digit 2. The three least significant digits display data normally.

An input overrange condition causes the most significant digit to blink and sets the three least significant digits to display "000". The buzzer output is enabled for input voltage and current signals with readings greater than 2000 counts in both manual and auto-range operation.

For resistance measurements the buzzer signal does not indicate an overrange condition. The buzzer is used to indicate continuity. Continuity is defined as a resistance reading less than 19 counts.

Table 5: Manual Range Operation

INPUT		DC VOLTS		AC VOLTS		OHM		LO OHM	
		23.5 V		18.2 V		18.2 kΩ		2.35 MΩ	
		RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY
POWER-ON		200 mV	"1"00.0 mV	2 V	"1".000 V	200 Ω	"1"00.0 Ω	2 kΩ	"1".000 kΩ
AUTO-RANGE OPERATION		2 V	"1".000 V	20 V	18.20 V	2 kΩ	"1".000 kΩ	10 kΩ	"1"0.00 kΩ
		20 V	"1"0.00 V			20 kΩ	18.20 kΩ	200 kΩ	"1"00.0 kΩ
		200 V	23.5 V					2000 kΩ	"1"350 kΩ
# of $\overline{\text{RANGE}}$ CHANGES ‾|_|‾	‾|_|‾	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY
MANUAL OPERATION	1	200 V	23.5 V	20 V	18.20 V	20 kΩ	18.20 kΩ	2000 kΩ	"1"350 kΩ
	2	200 mV	"1"00.0 mV	2 V	"1".000 V	200 Ω	"1"00.0 Ω	2 kΩ	"1".000 kΩ
	3	2 V	1.000 V	20 V	18.20 V	2 kΩ	"1".000 kΩ	20 kΩ	"1"0.00 kΩ
	4	20 V	"1"3.50 V	200 V	18.2 V	20 kΩ	18.20 kΩ	200 kΩ	"1"00.0 kΩ
	5	200 V	23.5 V	600 V	19 V	200 kΩ	18.2 kΩ	2000 kΩ	"1"350 kΩ
	6	1000 V	24 V	2 V	"1".000 V	2000 kΩ	19 kΩ	2 kΩ	"1".000 kΩ
	7	200 mV	"1"00.0 mV	20 V	18.20 V	200 Ω	"1"'00.0 Ω	20 kΩ	"1"0.00 kΩ
	8	2 V	"1".000 V	200 V	18.2 V	2 kΩ	"1".000 kΩ	200 kΩ	"1"00.0 kΩ

Notes:

1. A flashing MSD is shown as a "1". A flashing MSD indicates the TSC805 is over-ranged if all other digits are zero.
2. The first manual range selected is the last range in the auto-ranging mode.
3. A flashing MSD with a non-zero display indicates the TSC805 has entered the extended resolution operating mode. An additional 1000 counts of resolution is available. This extended operation is available only in manual operation for voltage, resistance and current measurements.
4. ‾|_|‾ = momentary ground connection.

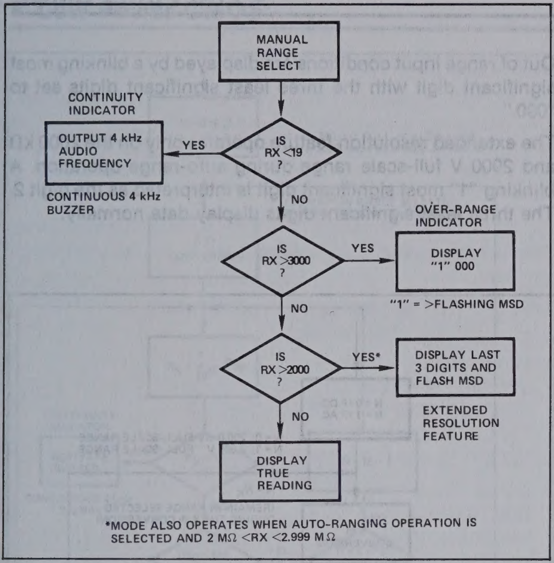

MANUAL RANGE SELECT
CONTINUITY INDICATOR
OUTPUT 4 kHz AUDIO FREQUENCY
YES
IS RX <19 ?
CONTINUOUS 4 kHz BUZZER
NO
OVER-RANGE INDICATOR
IS RX >3000 ?
YES
DISPLAY "1" 000
"1" = >FLASHING MSD
NO
IS RX >2000 ?
YES*
DISPLAY LAST 3 DIGITS AND FLASH MSD
NO
EXTENDED RESOLUTION FEATURE
DISPLAY TRUE READING
*MODE ALSO OPERATES WHEN AUTO-RANGING OPERATION IS SELECTED AND 2 MΩ <RX <2.999 MΩ

Figure 6: Manual Range Selection; Resistance Measurement

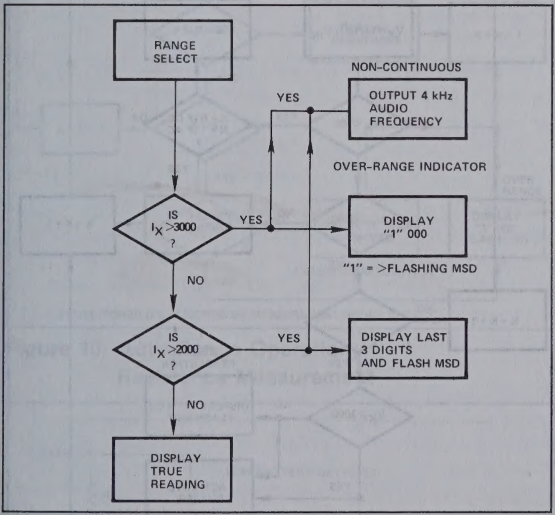

RANGE SELECT
NON-CONTINUOUS
YES
OUTPUT 4 kHz AUDIO FREQUENCY
OVER-RANGE INDICATOR
IS IX >3000 ?
YES
DISPLAY "1" 000
"1" = >FLASHING MSD
NO
IS IX >2000 ?
YES
DISPLAY LAST 3 DIGITS AND FLASH MSD
NO
DISPLAY TRUE READING

Figure 7: Manual Range Selection; Current Measurement

-MEM Operating Mode

Bringing $\overline{MEM}$ (Pin 58) momentarily low configures the TSC805 "-MEM" operating mode. The -MEM LCD Annunciator becomes active. In this operating mode subsequent measurements are made relative to the last two digits (≤99) displayed at the time MEM is low. This represents 5% of full-scale. The last two significant digits are stored and subtracted from all the following input conversions.

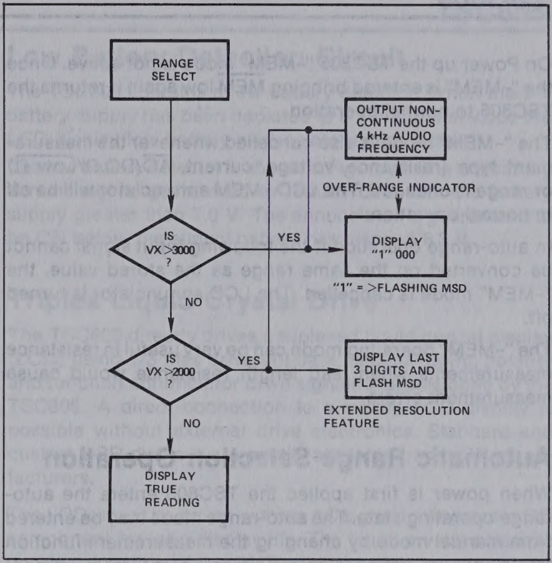

RANGE SELECT
OUTPUT NON-CONTINUOUS 4 kHz AUDIO FREQUENCY
OVER-RANGE INDICATOR
IS VX >3000 ?
YES
DISPLAY "1" 000
"1" = >FLASHING MSD
NO
IS VX >2000 ?
YES
DISPLAY LAST 3 DIGITS AND FLASH MSD
EXTENDED RESOLUTION FEATURE
NO
DISPLAY TRUE READING

Figure 8: Manual Range Selection; Voltage Measurement

A few examples clarify operation:

Example 1: In Auto-Ranging

Ri (N) = 18.21 kΩ (20 kΩ Range) = > Display 18.21 kΩ
$\overline{MEM}$ ‾|_|‾ = > Store 0.21 kΩ

Ri (N+1) = 19.87 kΩ (20 kΩ Range)
= > Display 19.87 - 0.21 = 19.66 kΩ

Ri (N+2) = 22.65 kΩ (200 kΩ Range)
= > Display 22.7 kΩ & $\overline{MEM}$ Disappears

Example 2: In Fixed Range , 200.0 Ω Full-Scale

Ri (N) = 18.2 Ω = > Display 18.2 Ω
$\overline{MEM}$ ‾|_|‾ = > Store 8.2 Ω
Ri (N+1) = 36.7 Ω
= > Display 36.7 - 8.2 = 28.5 Ω

Ri (N+2) = 5.8 Ω
= > Display 5.8 - 8.2 = –2.4 Ω*

* Will display minus resistance if following input is less than offset stored at fixed range

Example 3: In Fixed Range 20.00 V Full-Scale

Vi (N) = 0.51 V = > Display 0.51 V
$\overline{MEM}$ ‾|_|‾ = > Store 0.51 V

Vi (N+1) = 3.68 V
= > Display 3.68 - 0.51 = 3.17 V

Vi (N+2) = 0.23 V
= > Display 0.23 - 0.51 = –0.28 V

Vi (N+3) = –5.21 V
= > Display -5.21 - 0.51 = –5.72 V

On Power up the TSC805 "-MEM" mode is not active. Once the "-MEM" is entered bringing $\overline{\text{MEM}}$ low again it returns the TSC805 to normal operation.

The "-MEM" mode is also cancelled whenever the measurement type (resistance, voltage, current, $\overline{\text{AC}}$/DC,Ω/$\overline{\text{Low Ω}}$) or range is changed. The LCD -MEM annunciator will be off in normal operation.

In auto-range operation if the following input signal cannot be converted on the same range as the stored value, the "-MEM" mode is cancelled. The LCD annunciator is turned off.

The "-MEM" operating mode can be very useful in resistance measurements when lead length resistance would cause measurement errors.

Automatic Range Selection Operation

When power is first applied the TSC805 enters the auto-range operating state. The auto-range mode may be entered from manual mode by changing the measurement function (resistance or voltage) or by changing the measurement option ($\overline{\text{AC}}$/DC, Ω/$\overline{\text{LOΩ}}$).

The automatic voltage range selection begins on the most sensitive scale first: 200 mV for DC or 2.000 V for AC measurements. The voltage range selection flow chart is given in Figure 9.

Internal input protection diodes to VCC (Pin 26) and VSSA (Pin 55) clamp the input voltage. The external 10 MΩ input resistance (See Figure 1, R14 and R13) limits current safely in an overrange condition.

The voltage range selection is designed to maximize resolution. For input signals less than 9% of full-scale (count reading <180) the next most sensitive range is selected.

An overrange voltage input condition is flagged whenever the internal count exceeds 2000 by activating the buzzer output (Pin 3). This 4 kHz signal can directly drive a piezo electric acoustic transducer. An out of range input signal causes the 4 kHz signal to be on for 122 ms, off for 122 ms, on for 122 ms, and off for 610 ms (See Figure 15).

During voltage auto-range operation the extended resolution feature operates on the 2000 V range only (See extended resolution operating mode discussion).

The resistance automatic range selection procedure is shown in Figure 10. The 200 Ω range is the first range selected unless the TSC805 low ohms resistance measurement option is selected. In low ohms operation the first full-scale range tried is 2 kΩ.

The resistance range selected maximizes sensitivity. If the conversion results in a reading less than 180 the next most sensitive full-scale range is tried.

If the conversion is less than 19 in auto-range operation a continuous 4 kHz signal is output at BUZ (Pin 3). An overrange input does not activate the buzzer.

Out of range input conditions are displayed by a blinking most significant digit with the three least significant digits set to "000."

The extended resolution feature operates only on the 2000 kΩ and 2000 V full-scale range during auto-range operation. A blinking "1" most significant digit is interpreted as the digit 2. The three least significant digits display data normally.

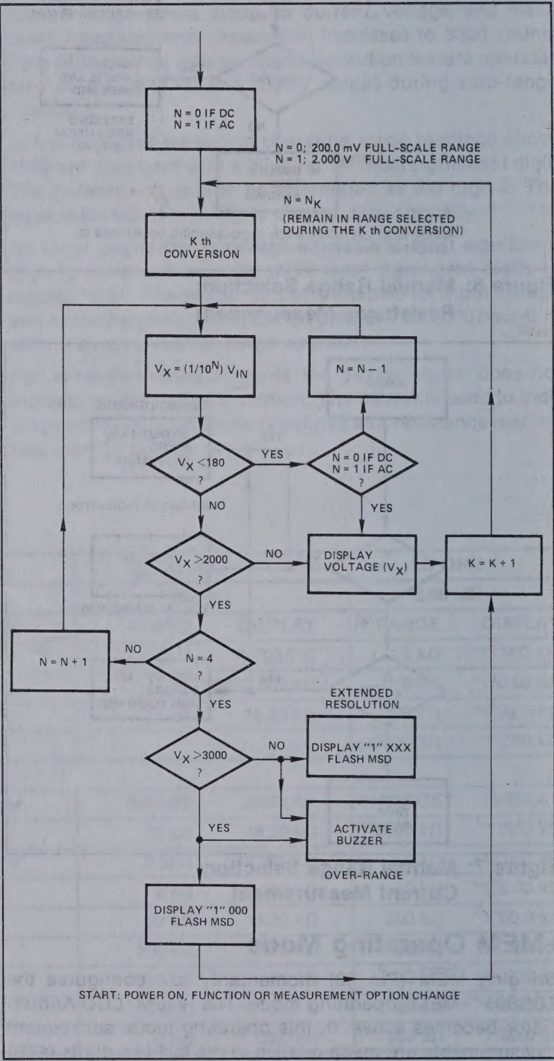

N = 0 IF DC
N = 1 IF AC
N = 0; 200.0 mV FULL-SCALE RANGE
N = 1; 2.000 V FULL-SCALE RANGE
N = N_K
(REMAIN IN RANGE SELECTED DURING THE K th CONVERSION)
K th CONVERSION
V_X = (1/10^N) V_IN
N = N − 1
V_X <180 ?
YES
NO
N = 0 IF DC
N = 1 IF AC
?
YES
V_X >2000 ?
NO
DISPLAY VOLTAGE (V_X)
K = K + 1
YES
N = N + 1
NO
N = 4 ?
YES
EXTENDED RESOLUTION
V_X >3000 ?
NO
DISPLAY "1" XXX FLASH MSD
YES
ACTIVATE BUZZER
OVER-RANGE
DISPLAY "1" 000 FLASH MSD
START: POWER ON, FUNCTION OR MEASUREMENT OPTION CHANGE

Figure 9: Auto-Range Operation; Voltage Measurement

3 1/2 Digit Auto-Ranging Analog-to-Digital Converter
- **Triplex LCD Drive**
- **Low Power CMOS**

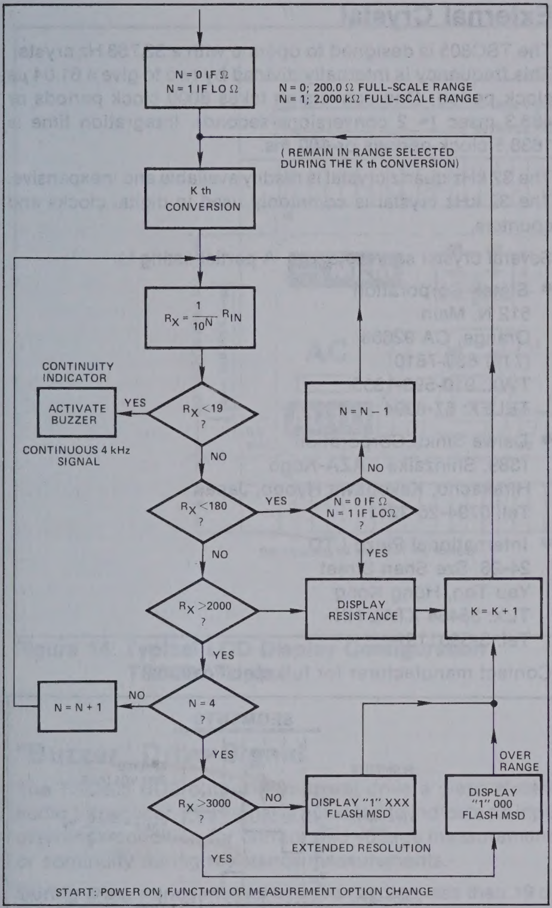

N = 0 IF Ω
N = 1 IF LO Ω
N = 0; 200.0 Ω FULL-SCALE RANGE
N = 1; 2.000 kΩ FULL-SCALE RANGE
(REMAIN IN RANGE SELECTED DURING THE K th CONVERSION)
K th CONVERSION
$R_X = \frac{1}{10^N} R_{IN}$
CONTINUITY INDICATOR
ACTIVATE BUZZER
YES
R_X <19 ?
CONTINUOUS 4 kHz SIGNAL
N = N − 1
NO
NO
R_X <180 ?
YES
N = 0 IF Ω N = 1 IF LOΩ ?
NO
YES
R_X >2000 ?
DISPLAY RESISTANCE
K = K + 1
YES
NO
N = N + 1
N = 4 ?
YES
OVER RANGE
R_X >3000 ?
NO
DISPLAY "1" XXX FLASH MSD
DISPLAY "1" 000 FLASH MSD
EXTENDED RESOLUTION
YES
START: POWER ON, FUNCTION OR MEASUREMENT OPTION CHANGE

Figure 10: Auto-Range Operation; Resistance Measurement

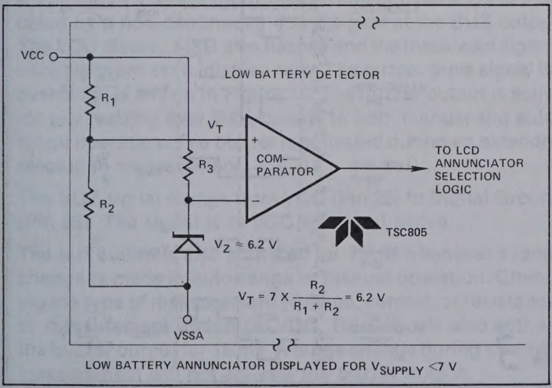

VCC
LOW BATTERY DETECTOR
R_1
V_T
+
R_3
COM-PARATOR
−
TO LCD ANNUNCIATOR SELECTION LOGIC
R_2
TSC805
$V_Z \approx 6.2$ V
$V_T = 7 \times \frac{R_2}{R_1 + R_2} = 6.2$ V
VSSA
LOW BATTERY ANNUNCIATOR DISPLAYED FOR V_{SUPPLY} <7 V

Figure 11: Low Battery Detector

Low Battery Detection Circuit

The TSC805 contains a low battery detector. When the 9 V battery supply has been depleted to a 7 V nominal value the LCD display low battery annunciator is activated.

The low battery detector is shown in Figure 11. The low battery annunciator is guaranteed to remain OFF with the battery supply greater than 7.0 V. The annunciator is guaranteed to be ON before the supply battery has reached 6.3 V.

Triplex Liquid Crystal Drive

The TSC805 directly drives a triplexed liquid crystal display (LCD) using 1/3 bias drive. All data, decimal point, polarity and function annunciator drive signals are developed by the TSC805. A direct connection to a triplex LCD display is possible without external drive electronics. Standard and custom LCD displays are readily available from LCD manufacturers.

The LCDs must be driven with an AC signal having a zero DC component for long display life. The liquid crystal polarization is a function of the RMS voltage appearing across the backplane and segment driver. The peak drive signal applied to the LCD is: VCC-VDISP.

If VDISP, for example, is set at a potential 3 V below VCC the peak drive signal is:

$$V_p = VCC - VDISP = 3\ V$$

An "OFF" LCD segment has an RMS voltage of Vp/3 across it or 1 volt. An "ON" segment has a 0.63 Vp signal across it or 1.92 V for VCC–VDISP = 3 V.

Since the VDISP pin is available the user may adjust the "ON" and "OFF" LCD levels for various manufacturer's displays by changing Vp. Liquid crystal threshold voltage moves down with temperature.

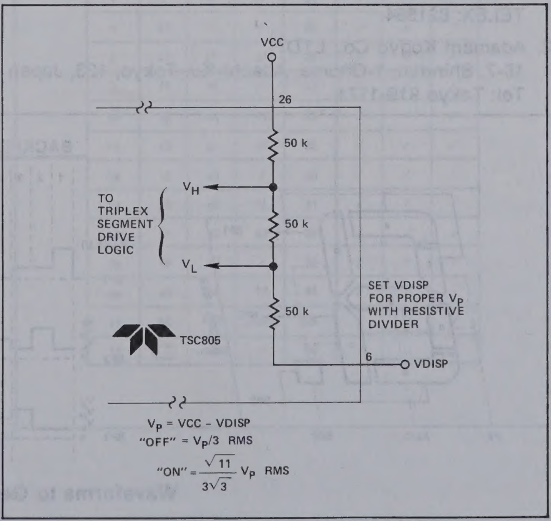

VCC
26
50 k
V_H
TO TRIPLEX SEGMENT DRIVE LOGIC
50 k
V_L
50 k
SET VDISP FOR PROPER V_P WITH RESISTIVE DIVIDER
TSC805
6
VDISP
V_P = VCC − VDISP
"OFF" = $V_P/3$ RMS
"ON" = $\frac{\sqrt{11}}{3\sqrt{3}} V_P$ RMS

Figure 12: 1/3 Bias LCD Drive

"OFF" segments may become visible at high LCD operating temperatures. A voltage with a -5 to -20 mV/° C temperature coefficient can be applied to VDISP to accommodate the liquid crystal temperature operating characteristics if necessary.

The TSC805 internally generates two intermediate LCD drive potentials (V_H & V_L) from a resistive divider (Figure 12) between VCC (Pin 26) and VDISP (Pin 6). The ladder impedance is approximately 150 kΩ. This drive method is commonly known as 1/3 bias. With V_{DISP} connected to digital ground $V_P \approx 5.0$ V.

The intermediate levels are needed so that drive signals giving RMS "ON" and "OFF" levels can be generated. Figure 13 shows a typical drive signal and the resulting wave forms for "ON" and "OFF" RMS voltage levels across a selected LCD element.

LCD Displays

Although most users will design their own custom LCD display, several manufacturers offer standard displays for the TSC805. Figure 14 shows a typical display available from Varitronix.

1. Varitronix Ltd.
   9/F Liven House, 61-63, King Yip Street
   Kwun Tjong, Hong Kong
   Tel: 3-410286
   TELEX: 36643 VTRAX HX

Part No.: VIM 309-1 Pin Connector
VIM 309-2 Elastomer Connector

USA OFFICE:
VL Electronics Inc.
2775 Glendower Ave.
Los Angeles, CA 90027
Tel. (213) 661-8883
TELEX: 821554

2. Adamant Kogyo Co., LTD.
   16-7, Shinden, 1-Chome, Adachi-Ku, Tokyo, 123, Japan
   Tel: Tokyo 919-1171

External Crystal

The TSC805 is designed to operate with a 32,768 Hz crystal. This frequency is internally divided by two to give a 61.04 μs clock period. One conversion takes 8000 clock periods or 488.3 msec (≈ 2 conversions/second). Integration time is 1638.5 clock periods or 100 ms.

The 32 kHz quartz crystal is readily available and inexpensive. The 32 kHz crystal is commonly used in digital clocks and counters.

Several crystal sources exists. A partial listing is:

- Statek Corporation
  512 N. Main
  Orange, CA 92668
  (714) 639-7810
  TWX: 910-593-1355
  TELEX: 67-8394

- Daiwa Sinku Corporation
  1389, Shinzaike - AZA-Kono
  Hirakacho, Kakogawa Hyogo, Japan
  Tel: 0794-26-3211

- International Piezo LTD
  24-26, Sze Shan Street
  Yau Ton, Hong Kong
  TLX: 35454 XTAL HX
  Tel: 3-3501151

Contact manufacturer for full specifications.

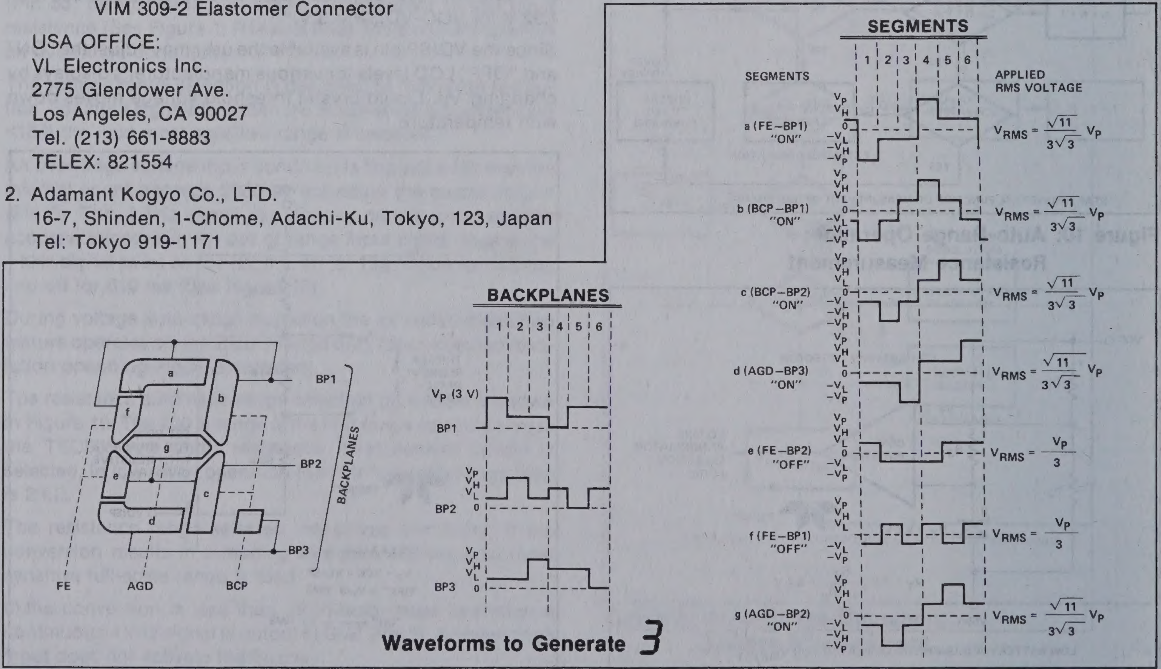

SEGMENTS
1 2 3 4 5 6
SEGMENTS
APPLIED RMS VOLTAGE
a (FE–BP1) "ON"
b (BCP–BP1) "ON"
c (BCP–BP2) "ON"
d (AGD–BP3) "ON"
e (FE–BP2) "OFF"
f (FE–BP1) "OFF"
g (AGD–BP2) "ON"
V_P V_H V_L 0 $-V_L$ $-V_H$ $-V_P$
$V_{RMS} = \frac{\sqrt{11}}{3\sqrt{3}} V_P$
$V_{RMS} = \frac{V_P}{3}$
BACKPLANES
1 2 3 4 5 6
V_P (3 V)
BP1
BP2
BP3
a
b
c
d
e
f
g
BP1
BP2
BP3
BACKPLANES
FE
AGD
BCP
Waveforms to Generate 3

Figure 13: Triplex LCD Drive Waveforms

3 1/2 Digit Auto-Ranging Analog-to-Digital Converter

- **Triplex LCD Drive**
- **Low Power CMOS**

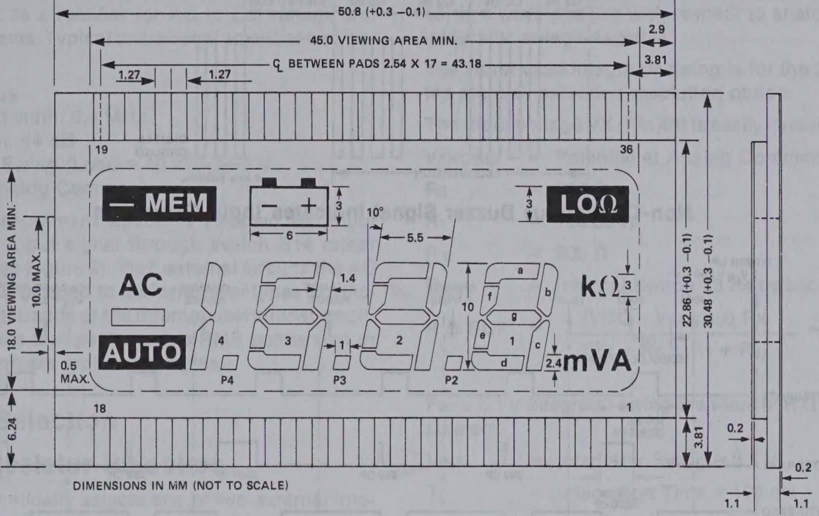

50.8 (+0.3 –0.1)
45.0 VIEWING AREA MIN.
℄ BETWEEN PADS 2.54 X 17 = 43.18
1.27
1.27
2.9
3.81
19
36
18
1
— MEM
LOΩ
AC
AUTO
kΩ
mVA
3
6
10°
5.5
1.4
10
3
1
2.4
0.5 MAX.
a
b
c
d
e
f
g
1
2
3
4
P4
P3
P2
18.0 VIEWING AREA MIN.
10.0 MAX.
6.24
22.86 (+0.3 –0.1)
30.48 (+0.3 –0.1)
3.81
0.2
0.2
1.1
1.1
DIMENSIONS IN MM (NOT TO SCALE)

Figure 14: Typical LCD Display Configuration TSC805 Triplex

PAD	BP1	BP2	BP3	PAD	COM1	COM2	COM3
1	BP1	/	/	19	/	/	/
2	/	BP2	/	20	/	/	/
3	/	/	BP3	21	/	/	/
4	/	LOΩ	A	22	/	/	/
5	/	Ω	V	23	/	/	/
6	/	k	m	24	/	/	/
7	b1	c1	/	25	/	/	/
8	a1	g1	d1	26	/	/	/
9	f1	e1	/	27	/	/	/
10	b2	c2	P2	28	/	/	/
11	a2	g2	d2	29	/	/	/
12	f2	e2	/	30	/	/	/
13	b3	c3	P3	31	/	/	/
14	a3	g3	d3	32	/	/	/
15	f3	e3	/	33	/	/	/
16	b4	c4	P4	34	/	/	/
17	AC	▭	AUTO	35	/	/	/
18	🔋	–MEM	/	36	/	/	/

"Buzzer" Drive Signal

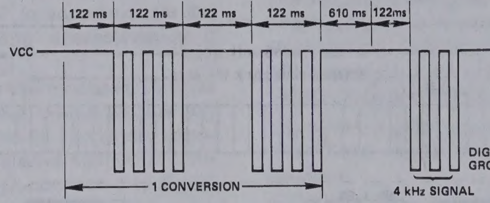
The TSC805 BUZ output (Pin 3) will drive a piezo electric audio transducer. The signal is activated to indicate an input overrange condition for current and voltage measurements or continuity during resistance measurements.

During a resistance measurement a reading less than 19 on any full-scale range causes a continuous 4 kHz signal to be output. This is used as a continuity indication.

A voltage or current input measurement overrange is indicated by a non-continuous 4 kHz signal at the BUZ output. The LCD display MSD also flashes and the three least significant digits are set to display zero. The buzzer drive signal for overrange is shown in Figure 15. The buzzer output is active for any reading over 2000 counts in both manual and auto-range operation. The buzzer is activated during an extended resolution measurement.

The BUZ signal swings from VCC (Pin 26) to Digital Ground (Pin 56). The signal is at VCC when not active.

The buz output is also activated for 15 ms whenever a range change is made in auto-range or manual operation. Changing the type of measurement (voltage, current, or resistance) or measurement option ($\overline{\text{AC}}$/DC, Ω/$\overline{\text{LO}\Omega}$) will also activate the buzzer output for 15 ms. A range change during a current measurement will not activate the buzzer output.


122 ms
122 ms
122 ms
122 ms
610 ms
122ms
VCC
DIGITAL GROUND
1 CONVERSION
4 kHz SIGNAL

Non-Continuous Buzzer Signal Indicates Input Overrange

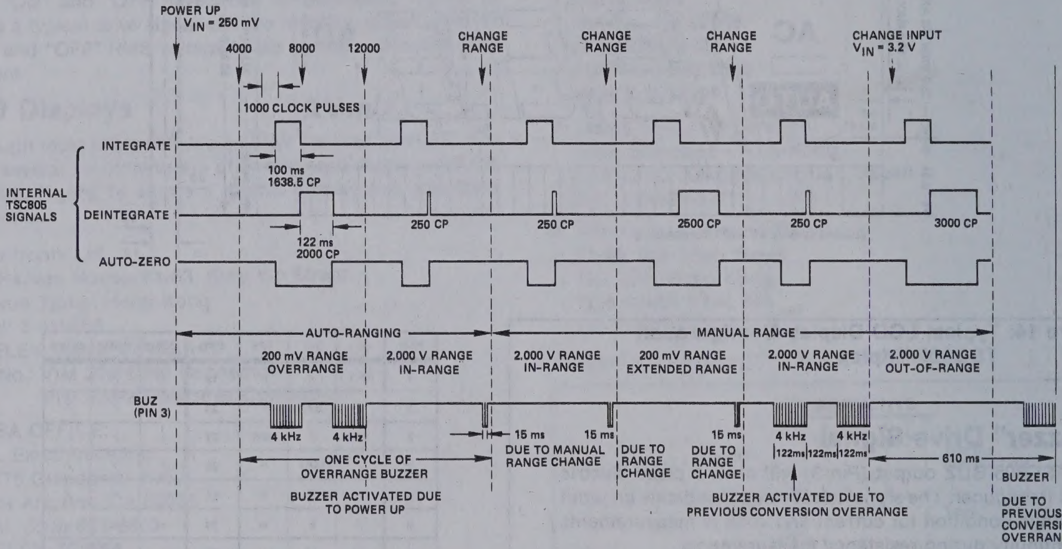

POWER UP
V_IN = 250 mV
4000
8000
12000
CHANGE RANGE
CHANGE RANGE
CHANGE RANGE
CHANGE INPUT V_IN = 3.2 V
1000 CLOCK PULSES
INTEGRATE
100 ms
1638.5 CP
INTERNAL TSC805 SIGNALS
DEINTEGRATE
250 CP
250 CP
2500 CP
250 CP
3000 CP
122 ms
2000 CP
AUTO-ZERO
AUTO-RANGING
MANUAL RANGE
200 mV RANGE OVERRANGE
2.000 V RANGE IN-RANGE
2.000 V RANGE IN-RANGE
200 mV RANGE EXTENDED RANGE
2.000 V RANGE IN-RANGE
2.000 V RANGE OUT-OF-RANGE
BUZ (PIN 3)
4 kHz
4 kHz
15 ms
15 ms
15 ms
4 kHz
4 kHz
122ms
122ms
122ms
610 ms
ONE CYCLE OF OVERRANGE BUZZER
DUE TO MANUAL RANGE CHANGE
DUE TO RANGE CHANGE
DUE TO RANGE CHANGE
BUZZER
BUZZER ACTIVATED DUE TO POWER UP
BUZZER ACTIVATED DUE TO PREVIOUS CONVERSION OVERRANGE
DUE TO PREVIOUS CONVERSION OVERRANGE

Figure 15: TSC805 Timing Waveform for Buzzer Output

Vendors for piezo electric audio transducers are:

1. Gulton Industries
   Piezo Products Division
   212 Durham Avenue
   Metuchen, New Jersey 08840
   (201) 548-2800
   Typical P/N's: 102-95NS, 101-FB-00
2. Taiyo Yuden (USA) Inc.
   Arlington Center
   714 West Algonquin Road
   Arlington Hts., Ill. 60005
   Typical P/N's: CB27BB, CB20BB, CB355BB

Display Decimal Point Selection

The TSC805 provides a decimal point LCD drive signal. The decimal point position is a function of the selected full-scale range as shown in Table 6.

Table 6: Decimal Point Selection

	1 •	9 •	9 • 9
Full-Scale Range	**DP3**	**DP2**	**DP1**
2000 V, 2000 kΩ	OFF	OFF	OFF
200.0 V, 200.0 kΩ	OFF	OFF	ON
20.00 V, 20.00 kΩ	OFF	ON	OFF
2.000 V, 2.000 kΩ	ON	OFF	OFF
200.0 mV, 200.0 Ω	OFF	OFF	ON
20.00 mA	OFF	ON	OFF
200.0 mA	OFF	OFF	ON

AC to DC Converter Operational Amplifier

The TSC805 contains an on chip operational amplifier that may be connected as a rectifier for AC to DC voltage and current measurements. Typical operational amplifier characteristics are:

- Slew Rate: 1 V/µs
- Unity Gain Bandwidth: 0.4 MHz
- Open Loop Gain: 44 dB
- Output Voltage Swing (Load = 10 kΩ) ±1.5 V (Reference to Analog Common)

When the AC measurement option is selected the input buffer receives an input signal through switch S14 rather than switch S11 (See Figure 2). With external circuits the AC operating mode can be used to perform other types of functions within the constraints of the internal operational amplifier. External circuits that perform true RMS conversion or a peak hold function are typical examples.

Component Selection

Integration Resistor Selection

The TSC805 automatically selects one of two external integration resistors. RVIBUF (Pin 53) is selected for voltage and current measurement. RΩBUF (Pin 52) is selected for resistance measurements.

RVIBUF Selection (PIN 53)

In auto-range operation the TSC805 operates with a 200 mV maximum full-scale potential at VI (Pin 42). Resistive dividers at VR2 (Pin 39), VR3 (Pin 38), VR4 (Pin 41) and VR5 (Pin 40) are automatically switched to maintain the 200 mV full-scale potential.

In manual mode the extended operating mode is activated giving a 300 mV full-scale potential at VI (Pin 42).

The integrator output swing should be maximized but saturations must be avoided. The integrator will swing within 0.45 V of VCC (Pin 26) and 0.5 V of VSSA (Pin 55) without saturating. A ±2 V swing is suggested. The value of RVIBUF is easily calculated assuming a worst case extended resolution input signal:

V_{INT} = Integrator Swing = ±2 V
T_I = Integration Time = 100 ms
C_I = Integration Capacitor = 0.1 µf
V_{MAX} = Maximum Input at V_I = 300 mV

$$\text{RVIBUF} = \frac{V_{MAX}(T_I)}{V_{INT}\,(C_I)} \approx 150\ \text{k}\Omega$$

RΩBUF Selection (Pin 52)

In ratiometric resistance measurements the signal at Rx (Pin 48) is always positive with respect to analog common. The integrator swings negative.

The worst case integrator swing is for the 200 Ω range with the manual, extended resolution option.

The input voltage VX (Pin 48) is easily calculated (Figure 16).

V_{ANCOM} = Potential at Analog Common ≈ 2.7 V
R_8 = 220 Ω
R_1 = 163.85 Ω
R_X = 300 Ω
R_S = Internal Switch 33 Resistance ≈ 600 Ω

$$\text{R}\,\Omega\,\text{BUF} = \frac{(V_{CC} - V_{ANCOM})\,R_X}{(R_X + R_S + R_1 + R_8)} = 0.63\ \text{V}$$

For a 3.1 V integrator swing the value of R Ω BUF is easily calculated:

V_{INT} = Integrator Swing = 3.1 V
T_I = Integration Time = 100 ms
C_I = Integration Cap. = 0.1 µf
R_X Max = 300 Ω
V_X Max = 700 mV

$$\text{R}\,\Omega\,\text{BUF} = \frac{(V_X\ \text{MAX})\,(T_I)}{C_I\,(V_{INT})} \approx 220\ \text{k}\Omega$$

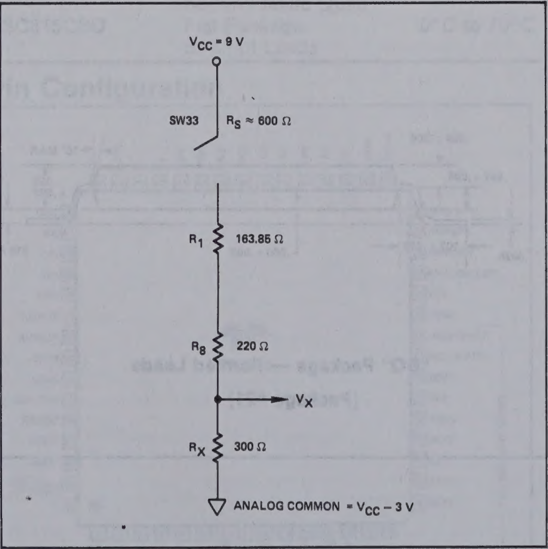


Figure 16: RΩBUF Calculation (200 Ω Manual Operation)

With a low battery voltage of 6.6 V analog common will be approximately 3.6 V above the negative supply terminal. With the integrator swinging down from analog common toward the negative supply a 3.1 V swing will set the integrator output to 0.5 V above the negative supply.

CINT, CAZ and CREF Capacitors

The integration capacitor, CINT, must have low dielectric absorption. A 0.1 uf polypropylene capacitor is suggested. The auto-zero capacitor, CAZ, and reference capacitor, CREF, should be selected for low leakage and dielectric absorption. Polystyrene capacitors are good choices.

Reference Voltage Adjustment

The TSC805 contains a low temperature drift internal voltage reference. The analog common potential (Pin 27) is established by this reference. Maximum drift is a low 75 ppm/° C. Analog common is designed to be approximately 2.6 V below VCC (Pin 26). A resistive divider (R18/R19, Figure 1) sets the TSC805 reference input voltage (REFHI, Pin 32) to approximately 163.85 mV.

With an input voltage near full-scale on the 200 mV range, R19 is adjusted for the proper reading.

Flat Package Socket

Sockets suitable for prototype work are available. A USA source is:

Nepenthe Distribution
2471 East Bayshore
Suite 520
Palo Alto, CA 94303
(415) 856-9332
TWX: 910-373-2060

(a) "BQ" Socket Part No.: IC51-064-042 BQ
(b) "SQ" Socket Part No.: IC51-064-042 SQ

Resistive Ladder Networks

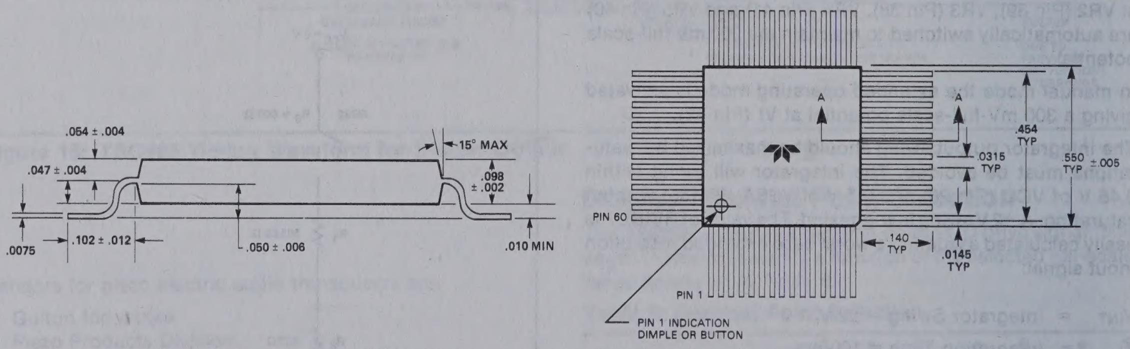
Resistor attenuator networks for voltage and resistance measurement are available from:

Caddock Electronics
1717 Chicago Avenue
Riverside, CA 92507
TEL: (714) 788-1700
TWX: 910-332-6108

Attenuator Accuracy	Attenuator Type	Caddock Part Number
0.1%	Voltage	1776-C441
0.25%	Voltage	1776-C44
0.25%	Resistance	T 1794-204-1

Package Outline

60-Pin Plastic Flat Package



"BQ" Package — Formed Leads
(Package #21)

"SQ" Package — Unformed Leads
(Package #22)

TELEDYNE SEMICONDUCTOR

TSC815
3 1/2 Digit Auto-Ranging Analog-to-Digital Converter
• Triplex LCD Drive
• Display Hold Function

General Description

The TSC815 is a 3 1/2 digit integrating analog-to-digital converter with triplex LCD display drive and automatic ranging. A display hold function is on-chip. Input voltage/ohm attenuators ranging from 1 to 1/10,000 are automatically selected. Five full-scale ranges are provided. The CMOS TSC815 contains all the logic and analog switches needed to manufacture an auto-ranging instrument for ohms and voltage measurements. User selected 20 mA and 200 mA current ranges are available. Full-scale range and decimal point LCD annunciators are automatically set in auto-range operation. Auto-range operation is available during ohms (high and low power ohms) and voltage (AC & DC) measurements. Auto-ranging eliminates expensive range switches in hand-held DMM designs and makes compact meters easier and less costly to design. The auto-range feature may be bypassed allowing decimal point selection and input attenuator selection control through a single line input. Expensive rotary switches are not required.

During manual mode operation resolution is extended to 3000 counts full-scale. The extended range operation is indicated by a flashing 1 MSD. The extended resolution is available during 2000 kΩ and 2000 V full-scale auto-range operation also.

The memory mode subtracts a reading — up to ±5% of full-scale — from subsequent measurements. Typical applications involve probe resistance compensation for resistance measurements, tolerance measurements, and tare weight measurement.

The TSC815 includes and AC to DC converter for AC measurements. Only external diodes/resistors/capacitors are required.

A complete LCD annunciator set describes the TSC815 meter function and measurement range during ohms, voltage and current operation. AC measurements are indicated as well as auto-range operation. A low battery detection circuit also sets the low battery display annunciator. The triplex LCD display drive levels may be set and temperature compensation applied via the V_{DISP} pin. With $\overline{HOLD}$ low the display is not updated. A HOLD MODE LCD annunciator is activated.

The "low ohms" measurement option allows in circuit resistance measurements by preventing semiconductor junctions from being forward biased.

A continuity buzzer output is activated with inputs less than 1% of full-scale. An overrange input signal also enables the buzzer, except during resistance measurements, and flashes the MSD display. Featuring single 9 V battery operation, 10 mW power consumption, a precision internal voltage reference (75 ppm/°C max. TC) and a compact surface mounted 60-pin quad flat package, the TSC815 is ideal for portable instruments.

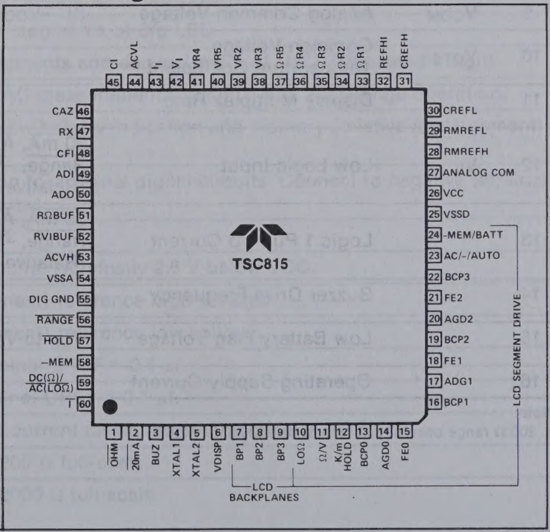
Features

- Auto-Range Operation for AC & DC Voltage and Resistance Measurements
  - — Two User Selected AC/DC Current Ranges 20 & 200 mA
- 22 Operating Ranges
  - — 9 DC/AC Voltage
  - — 4 AC/DC Current
  - — 9 Resistance and Low Power Ohms
- Display HOLD Function
- 3 1/2 Digit Resolution in Auto-Range Mode 1/2000
  - — Extended Resolution in Manual Mode 1/3000
- Memory Mode for Relative Measurements ... ±5% F.S.
- Internal AC to DC Conversion Op Amp
- Triplex LCD Drive for Decimal Points, Digits and Annunciators
- Continuity Detection and Piezoelectric Transducer Driver
- Compact Surface Mounted 60-Pin Quad Flat Package
- Low Drift Internal Reference .... 75 ppm/°C
- 9 V Battery Operation .... 10 mW
- Low Battery Detection and LCD Annunciator

Ordering Information

Part. No.	Package	Temp. Range
TSC815CBQ	60-Pin Plastic Quad Flat Package Formed Leads	0°C to 70°C
TSC815CSQ	60-Pin Plastic Quad Flat Package Straight Leads	0°C to 70°C

Pin Configuration


CI
ACVL
I_I
V_I
VR4
VR5
VR2
VR3
ΩR5
ΩR4
ΩR3
ΩR2
ΩR1
REFHI
CREFH
45
44
43
42
41
40
39
38
37
36
35
34
33
32
31
CAZ 46
RX 47
CFI 48
ADI 49
ADO 50
RΩBUF 51
RVIBUF 52
ACVH 53
VSSA 54
DIG GND 55
$\overline{RANGE}$ 56
$\overline{HOLD}$ 57
−MEM 58
DC(Ω)/$\overline{AC(LOΩ)}$ 59
T 60
30 CREFL
29 RMREFL
28 RMREFH
27 ANALOG COM
26 VCC
25 VSSD
24 −MEM/BATT
23 AC/−/AUTO
22 BCP3
21 FE2
20 AGD2
19 BCP2
18 FE1
17 ADG1
16 BCP1
LCD SEGMENT DRIVE
TSC815
1 OHM
2 20mA
3 BUZ
4 XTAL1
5 XTAL2
6 VDISP
7 BP1
8 BP2
9 BP3
10 LOΩ
11 Ω/V
12 K/m HOLD
13 BCP0
14 AGD0
15 FE0
LCD BACKPLANES

©1985

3 1/2 Digit Auto-Ranging Analog-to-Digital Converter
• Triplex LCD Drive
• Display Hold Function

TSC815

Absolute Maximum Ratings

Supply Voltage (V^+ to V^-)	15 V
Analog Input Voltage	V^+ to V^-
Reference Input Voltage	V^+ to V^-
Voltage at Pin 43	GND ±0.7 V
Power Dissipation	
Plastic Package	800 mW
Operating Temperature	
"C" Devices	0°C to +70°C
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering, 60 sec.)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

Electrical Characteristics: V_S = 9 V, T_A = 25°C, Figure 1 Test Circuit

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC815 MIN	TYP	MAX	UNIT
1		Zero Input Reading	200 mV Range w/o 10 MΩ Input Resistor	-0000	0000	+0000	Digital Reading
			200 mV Range w/10 MΩ Input	-0001	—	+0001	
			20 mA and 200 mA Range	-0000	0000	+0000	
2	RE	Rollover Error	200 mV Range w/o 10 MΩ Input Resistor	—	—	±1	Count
			200 mV Range w/10 MΩ Input	—	—	±3	
			20 mA and 200 mA Range	—	—	±1	
3	NL	Linearity Error	Best Case Straight Line	—	—	±1	Count
4	I_{IN}	Input Leakage Current		—	—	10	pA
5	E_N	Input Noise	BW = 0.1 to 10 Hz	—	20	—	μV_{p-p}
6		AC Frequency Response	±1% Error	—	40 to 500	—	Hz
			±5% Error	—	40 to 2000	—	
7		Open Circuit Voltage for OHM Measurements	Excludes 200 Ω Range	—	570	660	mV
8		Open Circuit Voltage for LO OHM Measurement	Excludes 200 Ω Range	—	285	350	mV
9	V_{COM}	Analog Common Voltage	(V^+ $-V_{COM}$)	2.5	2.6	3.3	V
10	V_{CTC}	Common Voltage Temperature Coefficient		—	—	50	ppm/°C
11		Display Multiplex Rate		—	100	—	Hz
12	V_{IL}	Low Logic Input	$\overline{\text{20 mA}}$, $\overline{\text{AC}}$, $\overline{\text{I}}$, $\overline{\text{Low }\Omega}$, $\overline{\text{HOLD}}$ Range, -MEM, $\overline{\text{OHM}_\text{S}}$ (Relative to DIG GND Pin 56)	—	—	1	V
13		Logic 1 Pull Up Current	$\overline{\text{20 mA}}$, $\overline{\text{AC}}$, $\overline{\text{I}}$, $\overline{\text{Low }\Omega}$, $\overline{\text{HOLD}}$ Range, -MEM, $\overline{\text{OHM}_\text{S}}$ (Relative to DIG GND Pin 56)	—	25	—	μA
14		Buzzer Drive Frequency		—	4	—	kHz
15		Low Battery Flag Voltage	V_{CC} to V_{SSA}	6.3	6.6	7.0	V
16		Operating Supply Current		—	0.8	1.5	mA

Note:
1. 200 Ω range open circuit voltage approximately 2.8 V.

Pin Description and Function Table 1:

PIN NO. (Quad Flat Package)	SYMBOL	DESCRIPTION
1	$\overline{\text{OHM}}$	Logic Input. "0" (Digital Ground) for resistance measurement.
2	$\overline{\text{20 mA}}$	Logic Input. "0" (Digital Ground) for 20 mA full-scale current measurement.
3	BUZ	Audio frequency, 4 kHz, output for continuity indication during resistance measurement. A non-continuous 4 kHz signal is output to indicate an input overrange during voltage or current measurements.
4	XTAL1	32.768 kHz Crystal Connection.
5	XTAL2	32.768 kHz Crystal Connection.
6	VDISP	Sets peak LCD drive signal: VP = VCC-VDISP. VDISP may also be used to compensate for temperature variation of LCD crystal threshold voltage.
7	BP1	LCD Backplane #1.
8	BP2	LCD Backplane #2.
9	BP3	LCD Backplane #3.
10	Low Ω/A	LCD Annunciator segment drive for low ohms resistance measurement and current measurement.
11	Ω/V	LCD Annunciator segment drive for resistance measurement and voltage measurement.
12	K/m/HOLD	LCD Annunciator segment drive for k ("kilo-ohms"), m ("milli-amps" and "milli-volts") and HOLD mode.
13	BCP0	LCD segment drive for "b," "c" segments and decimal point of least significant digit (LSD). (Ones digit).
14	AGD0	LCD segment drive for "a," "g," "d" segments of LSD.
15	FE0	LCD segment drive for "f" and "e" segments of LSD.
16	BCP1	LCD segment drive for "b," "c" segments and decimal point of 2nd LSD.
17	AGD1	LCD segment drive for "a," "g," "d" segments of 2nd LSD (Ten's digit).
18	FE1	LCD segment drive for "f," and "e" segments of 2nd LSD.
19	BCP2	LCD segment drive for "b," "c," and decimal point of 3rd LSD. (Hundreds digit).
20	AGD2	LCD segment drive for "a," "g," "d" segments of 3rd LSD.
21	FE2	LCD segment drive for "b" and "c" segments of 3rd LSD.
22	BCP3	LCD segment drive for "b," "c" segments and decimal point of MSD (Thousand's digit).
23	AC/-/AUTO	LCD annunciator drive signal for AC measurements, polarity, and auto-range operation.
24	-MEM/BATT	LCD annunciator drive signal for low battery indication and memory (relative measurement) mode.
25	VSSD	Negative battery supply connection for internal digital circuits. Connect to negative terminal of battery.
26	VCC	Positive battery supply connection.
27	COM	Analog circuit ground reference point. Nominally 2.6 V below VCC.
28	RMREFH	Ratiometric (Resistance measurement) reference high voltage.
29	RMREFL	Ratiometric (Resistance measurement) reference low voltage.
30	CREFL	Reference capacitor negative terminal CREF = 0.1 μf.
31	CREFH	Reference capacitor positive terminal CREF = 0.1 μf.
32	REFHI	Reference voltage for voltage and current measurement. Nominally 163.85 mV.
33	ΩR1	Standard resistor connection for 200 Ω full-scale.
34	ΩR2	Standard resistor connection for 2000 Ω full-scale.

Pin Description and Function Table 1:

PIN NO. (Quad Flat Package)	SYMBOL	DESCRIPTION
35	ΩR3	Standard resistor connection for 20 kΩ full-scale range.
36	ΩR4	Standard resistor connection for 200 kΩ full-scale range.
37	ΩR5	Standard resistor connection for 2000 kΩ full-scale range.
38	VR3	Voltage measurement ÷ 100 attenuator.
39	VR2	Voltage measurement ÷ 10 attenuator.
40	VR5	Voltage measurement ÷ 10,000 attenuator.
41	VR4	Voltage measurement ÷ 1000 attenuator.
42	V_I	Unknown voltage input ÷ 1 attenuator.
43	I_I	Unknown current input.
44	ACVL	Low output of AC to DC converter.
45	CI	Integrator capacitor connection. Nominally 0.1 μf. (Low dielectric absorption. Polypropylene dielectric suggested).
46	CAZ	Auto-zero capacitor connection. Nominally 0.1 μf.
47	Rx	Unknown resistance input.
48	CFI	Input filter connection.
49	ADI	Negative input of internal AC to DC operational amplifier.
50	ADO	Output of internal AC to DC operational amplifier.
51	RΩBUF	Active buffer output for resistance measurement. Integration resistor connection. Integrator resistor nominally 220 kΩ.
52	RVIBUF	Active buffer output for voltage and current measurement. Integration resistor connection. Integration resistor nominally 150 kΩ.
53	ACVH	Positive output of AC to DC converter.
54	VSSA	Negative supply connection for analog circuits. Connect to negative terminal of 9 V battery.
55	DIG GND	Internal logic digital ground. The logic "0" level. Nominally 4.7 V below VCC.
56	$\overline{\text{RANGE}}$	Input to set manual operation and change ranges.
57	$\overline{\text{HOLD}}$	Input to hold display. connect to DIG GND.
58	$\overline{\text{MEM}}$	Input to enter memory measurement mode for relative measurements. The two LSD's are stored and subtracted from future measurements.
59	DC/$\overline{\text{AC}}$, $\Omega/\overline{\text{LOW }\Omega}$	Input that selects AC or DC option during voltage/current measurements. For resistance measurements, the ohms or low power (voltage) ohms option can be selected.
60	$\overline{\text{I}}$	Input to select current measurement. Set to logic "0" (Digital ground) for current measurement.

3 1/2 Digit Auto-Ranging Analog-to-Digital Converter

- **Triplex LCD Drive**
- **Display Hold Function**

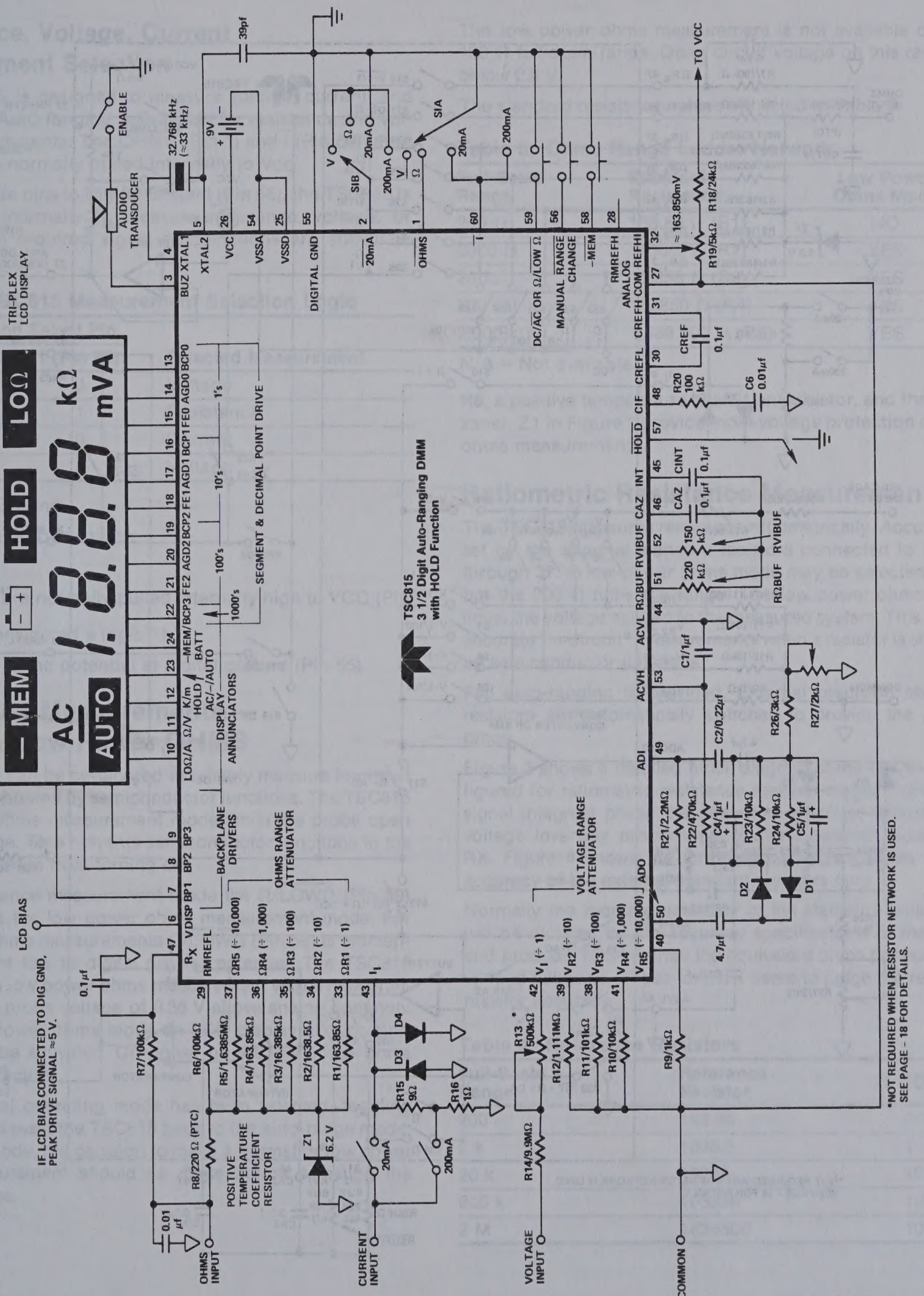
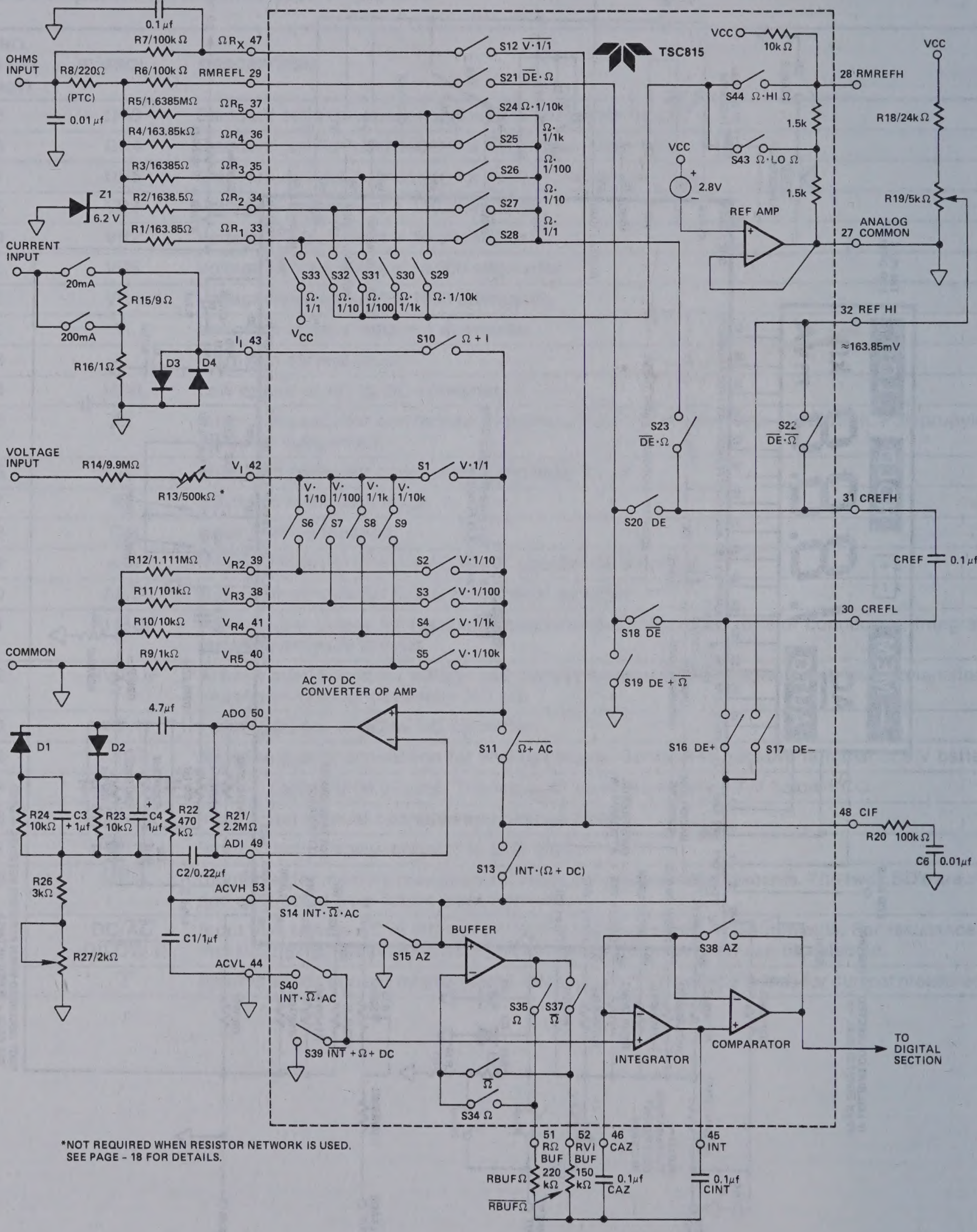

TRI-PLEX LCD DISPLAY
–MEM
AC
AUTO
HOLD
LOΩ
kΩ
mVA
1.8.8.8
AUDIO TRANSDUCER
ENABLE
32.768 kHz (≈33 kHz)
39pf
9V
SIB
SIA
V
Ω
20mA
200mA
TSC815 3 1/2 Digit Auto-Ranging DMM with HOLD Function
BUZ XTAL1
XTAL2
VCC
VSSA
VSSD
DIGITAL GND
20mA
OHMS
DC/AC OR Ω/LOW Ω
MANUAL RANGE CHANGE
–MEM
RMREFH
ANALOG COM
REFHI
CREFH
CREFL
CIF
HOLD
INT
CAZ
RVIBUF
RΩBUF
ACVL
ACVH
ADI
ADO
≈163.850mV
TO VCC
R18/24kΩ
R19/5kΩ
CREF 0.1µf
R20 100 kΩ
C6 0.01µf
CINT 0.1µf
CAZ 0.1µf
150 kΩ
220 kΩ
C1/1µf
C2/0.22µf
R26/3kΩ
R27/2kΩ
R21/2.2MΩ
R22/470kΩ
C4/1µf
R23/10kΩ
R24/10kΩ
C5/1µf
D1
D2
4.7µf
VOLTAGE RANGE ATTENUATOR
V_1 (÷ 1)
V_{R2} (÷ 10)
V_{R3} (÷ 100)
V_{R4} (÷ 1,000)
V_{R5} (÷ 10,000)
R13* 500kΩ
R12/1.111MΩ
R11/101kΩ
R10/10kΩ
R9/1kΩ
R14/9.9MΩ
VOLTAGE INPUT
COMMON
*NOT REQUIRED WHEN RESISTOR NETWORK IS USED. SEE PAGE - 18 FOR DETAILS.
LOΩ/A Ω/V K/m HOLD AC/–/AUTO BATT –MEM/BCP3 FE2 AGD2 BCP2 FE1 AGD1 BCP1 FE0 AGD0 BCP0
DISPLAY ANNUNCIATORS
1000's
100's
10's
1's
SEGMENT & DECIMAL POINT DRIVE
BACKPLANE DRIVERS
VDISP BP1 BP2 BP3
OHMS RANGE ATTENUATOR
R_X
RMREFL
ΩR5 (÷ 10,000)
ΩR4 (÷ 1,000)
ΩR3 (÷ 100)
ΩR2 (÷ 10)
ΩR1 (÷ 1)
I_I
LCD BIAS
IF LCD BIAS CONNECTED TO DIG GND, PEAK DRIVE SIGNAL ≈5 V.
0.1µf
R7/100kΩ
R6/100kΩ
R5/1.6385MΩ
R4/163.85kΩ
R3/16.385kΩ
R2/1638.5Ω
R1/163.85Ω
D3
D4
R15 9Ω
R16 1Ω
Z1 6.2 V
20mA
200mA
R8/220 Ω (PTC)
POSITIVE TEMPERATURE COEFFICIENT RESISTOR
0.01 µf
OHMS INPUT
CURRENT INPUT

Figure 1: Typical Application & Test Circuit


0.1µf
R7/100k Ω
ΩRX 47
OHMS INPUT
R8/220Ω
(PTC)
R6/100k Ω
RMREFL 29
0.01µf
R5/1.6385MΩ
ΩR5 37
R4/163.85kΩ
ΩR4 36
R3/16385Ω
ΩR3 35
Z1
6.2 V
R2/1638.5Ω
ΩR2 34
R1/163.85Ω
ΩR1 33
CURRENT INPUT
20mA
R15/9Ω
200mA
R16/1Ω
D3
D4
I1 43
VOLTAGE INPUT
R14/9.9MΩ
R13/500kΩ *
VI 42
R12/1.111MΩ
VR2 39
R11/101kΩ
VR3 38
R10/10kΩ
VR4 41
COMMON
R9/1kΩ
VR5 40
4.7µf
ADO 50
D1
D2
R24 10kΩ
C3 1µf
R23 10kΩ
C4 1µf
R22 470 kΩ
R21/ 2.2MΩ
ADI 49
C2/0.22µf
R26 3kΩ
ACVH 53
C1/1µf
R27/2kΩ
ACVL 44
S12 V̅·1/1
S21 D̅E̅·Ω
S24 Ω·1/10k
S25
Ω· 1/1k
S26
Ω· 1/100
S27
Ω· 1/10
S28
Ω· 1/1
S33
S32
S31
S30
S29
Ω· 1/1
Ω· 1/10
Ω· 1/100
Ω· 1/1k
Ω· 1/10k
VCC
S10
Ω + I
S1
V·1/1
V· 1/10
V· 1/100
V· 1/1k
V· 1/10k
S6
S7
S8
S9
S2
V·1/10
S3
V·1/100
S4
V·1/1k
S5
V·1/10k
AC TO DC CONVERTER OP AMP
S11
Ω̅+ AC
S13
INT·(Ω + DC)
S14 INT·Ω̅·AC
S15 AZ
BUFFER
S40 INT·Ω̅·AC
S39 I̅N̅T̅ +Ω+ DC
S35 Ω
S37 Ω̅
Ω̅
S34 Ω
S38 AZ
INTEGRATOR
COMPARATOR
TO DIGITAL SECTION
51 RΩ BUF
52 RVI BUF
46 CAZ
45 INT
RBUFΩ
220 kΩ
150 kΩ
0.1µf CAZ
0.1µf CINT
R̅B̅U̅F̅Ω̅
TSC815
VCC
10k Ω
S44 Ω·HI Ω
1.5k
S43 Ω·LO Ω
VCC
2.8V
1.5k
REF AMP
28 RMREFH
VCC
R18/24k Ω
R19/5k Ω
ANALOG 27 COMMON
32 REF HI
≈163.85mV
S23 D̅E̅·Ω
S22 D̅E̅·Ω̅
S20 DE
31 CREFH
CREF 0.1µf
S18 D̅E̅
30 CREFL
S19 DE + Ω̅
S16 DE+
S17 DE–
48 CIF
R20 100k Ω
C6 0.01µf

*NOT REQUIRED WHEN RESISTOR NETWORK IS USED. SEE PAGE - 18 FOR DETAILS.

Figure 2: TSC815 Analog Section

Resistance, Voltage, Current Measurement Selection

The TSC815 is designed to measure voltage, current, and resistance. Auto-ranging is available for resistance and voltage measurements. The $\overline{\text{OHMS}}$ (Pin 1) and $\overline{\text{I}}$ (Pin 60) input controls are normally pulled internally to V_{CC}.

By tying these pins to Digital Ground (Pin 56), the TSC815 is configured internally to measure resistance, voltage, or current. The required signal combinations are shown in Table 2.

Table 2: TSC815 Measurement Selection Logic

Function Select Pin		
OHM (Pin 1)	**I (Pin 60)**	**Selected Measurement**
0	0	Voltage
0	1	Resistance
1	0	Current
1	1	Voltage

0 = Digital Ground

1 = Floating or Tied to V_{CC}

Notes:

1. $\overline{\text{OHM}}$ & $\overline{\text{I}}$ are normally pulled internally high to VCC (Pin 26).
   This is considered a logic "1."
2. Logic "0" is the potential at digital ground (Pin 55).

Resistance Measurements — OHMS & Low Power OHMS

The TSC815 can be configured to reliably measure in-circuit resistances shunted by semiconductor junctions. The TSC815 low power ohms measurement mode limits the probe open circuit voltage. This prevents semiconductor junctions in the measured system from turning on.

In the resistance measurement mode the $\Omega/\overline{\text{LOW}\Omega}$ (Pin 59) input selects the low power ohms measurement mode. For low power ohms measurements $\Omega/\overline{\text{LOW}\Omega}$ (Pin 59) is momentarily brought low to digital ground potential. The TSC815 sets up for a low power ohms measurement with a maximum open circuit probe voltage of 0.35 V above analog common. In the low power ohms mode an LCD display annunciator, LOWΩ, will be activated. On power up the low power ohms mode is not active.

If the manual operating mode has been selected, toggling $\Omega/\overline{\text{LOW}\Omega}$ will reset the TSC815 back to the auto-range mode. In manual mode, the decision to make a normal or low power ohms measurement should be made before selecting the desired range.

The low power ohms measurement is not available on the 100 Ω full-scale range. Open circuit voltage on this range is below 2.8 V.

The standard resistance values are listed in Table 3.

Table 3: Ohms Range Ladder Network

Full-Scale Range	Standard Resistance	Low Power Ohms Mode
200 Ω	163.85 Ω (R1)	NO
2000 Ω	1638.5 Ω (R2)	YES
20 kΩ	16,358 Ω (R3)	YES
200 kΩ	163850 Ω (R4)	YES
2,000 kΩ	1,638,500 Ω (R5)	YES

N/A = Not available.

R8, a positive temperature coefficient resistor, and the 6.2 V zener, Z1 in Figure 1 provide input voltage protection during ohms measurements.

Ratiometric Resistance Measurements

The TSC815 measures resistance ratiometrically. Accuracy is set by the external standard resistors connected to Pin 33 through 37. A low-power ohms mode may be selected on all but the 200 Ω full-scale range. The low power ohms mode limits the voltage applied to the measured system. This allows accurate "in-circuit" measurements when a resistor is shunted by semiconductor junctions.

Full auto-ranging is provided. External precision standard resistors are automatically switched to provide the proper range.

Figure 3 shows a detailed block diagram of the TSC815 configured for ratiometric resistance measurements. During the signal integrate phase the reference capacitor charges to a voltage inversely proportional to the measured resistance-RX. Figure 4 shows the conversion accuracy relies on the accuracy of the external standard resistors only.

Normally the required accuracy of the standard resistances will be dictated by the accuracy specifications of the users end product. Table 4 gives the equivalent ohms per count for various full-scale ranges to allow users to judge the required resistor accuracy.

Table 4: Reference Resistors

Full-Scale Range	Reference Resistor	Ω/COUNT
200	163.85	0.1
2 k	1638.5	1
20 k	16385	10
200 k	163850	100
2 M	1638500	1000

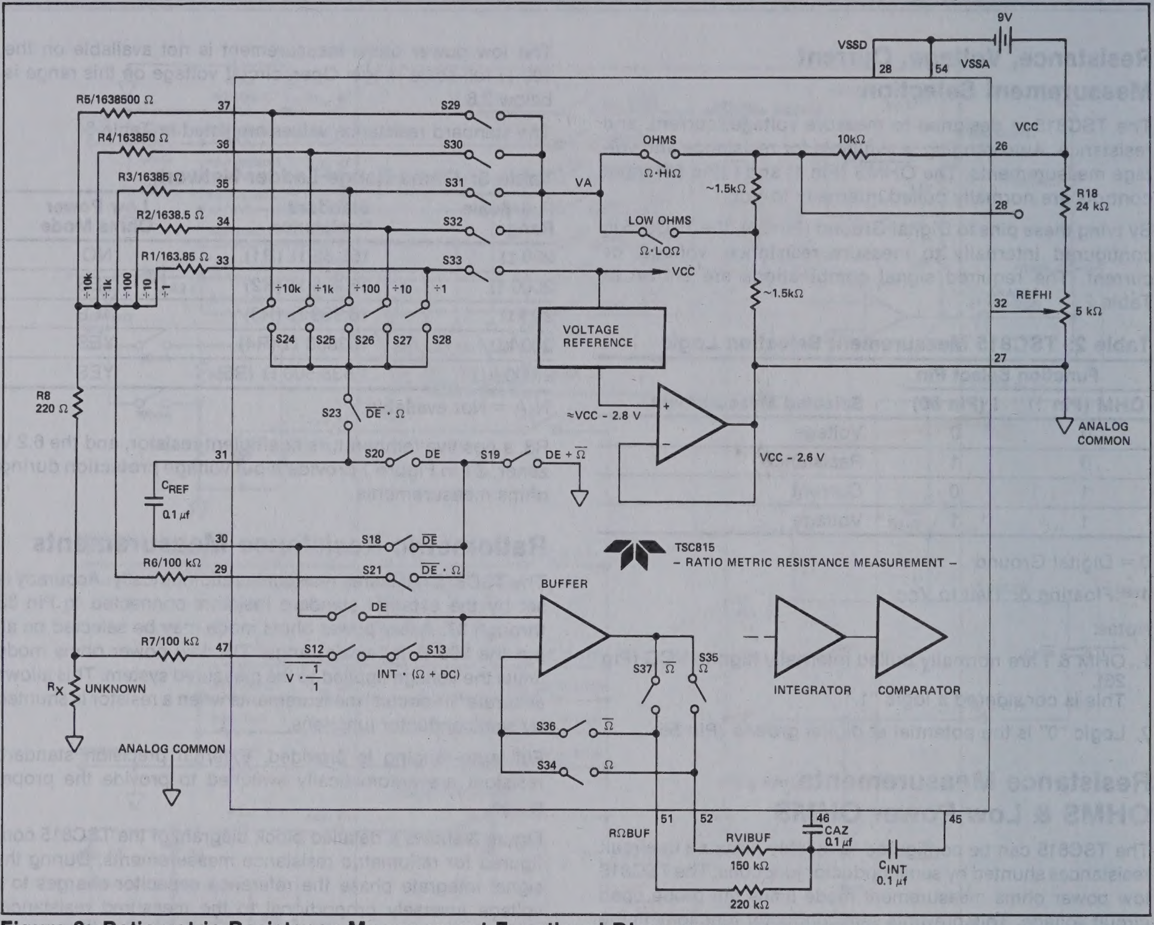

R5/1638500 Ω
37
R4/163850 Ω
36
R3/16385 Ω
35
R2/1638.5 Ω
34
R1/163.85 Ω
33
÷10k
÷1k
÷100
÷10
÷1
S29
S30
S31
S32
S33
VA
S24
S25
S26
S27
S28
VOLTAGE REFERENCE
R8
220 Ω
S23
DE · Ω
31
S20
DE
S19
DE + Ω
C_REF
0.1 µf
30
S18
DE
R6/100 kΩ
29
S21
DE · Ω
BUFFER
DE
R7/100 kΩ
47
S12
S13
V · 1/1
INT · (Ω + DC)
R_X UNKNOWN
ANALOG COMMON
VSSD
28
54
VSSA
9V
VCC
OHMS
Ω·HIΩ
10kΩ
26
~1.5kΩ
R18
24 kΩ
28
LOW OHMS
Ω·LOΩ
VCC
~1.5kΩ
REFHI
32
5 kΩ
27
≈VCC - 2.8 V
VCC - 2.6 V
ANALOG COMMON
TSC815
– RATIO METRIC RESISTANCE MEASUREMENT –
INTEGRATOR
COMPARATOR
S37
Ω
S35
Ω
S36
Ω
S34
Ω
51
52
46
CAZ
0.1 µf
45
RΩBUF
RVIBUF
150 kΩ
220 kΩ
C_INT
0.1 µf

Figure 3: Ratiometric Resistance Measurement Functional Diagram

Voltage Measurement

Resistive dividers are automatically changed to provide in range readings for 200 mV to 2000 V full-scale readings (Figure 2). The input resistance is set by external resistors R14/R13. The divider leg resistors are R9-R12. The divider leg resistors give a 200 mV signal VI (Pin 42) for full-scale voltages from 200 mV to 2000 V.

For applications which do not require a 10 mΩ input impedance the divider network impedances may be lowered. This will reduce voltage offset errors induced by switch leakage currents.

Current Measurement

The TSC815 measures current only under manual range operation. The two user selectable full-scale ranges are: 20 mA and 200 mA. Select the current measurement mode by holding the I input (Pin 60) low at digital ground potential. The OHM input (Pin 1) is left floating or tied to the positive supply.

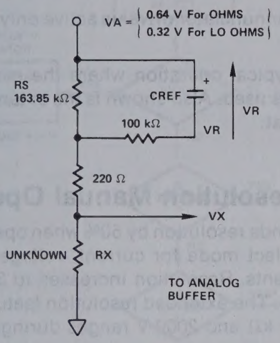
Two ranges are possible. The 20 mA full-scale range is selected by connecting the 20 mA input (Pin 2) to digital ground. If left floating the 200 mA full-scale range is selected.

External current to voltage conversion resistors are used at the I_I input (Pin 43). For 20 mA measurements a 10 Ω resistor is used. the 200 mA range needs a 1 Ω resistor. Full-scale is 200 mV.

PC board trace resistance between analog common and R16 (See Figure 1) must be minimized. In the 200 mA range, for example, a 0.05 trace resistance will cause a 5% current to voltage conversion error at I_I (Pin 43).

The extended resolution measurement option operates during current measurements.

To minimize rollover error the potential difference between analog common (Pin 27) and system common must be minimized.


VA = 0.64 V For OHMS
0.32 V For LO OHMS
RS
163.85 kΩ
CREF
+
VR
100 kΩ
VR
220 Ω
VX
UNKNOWN
RX
TO ANALOG
BUFFER

Example: 200 kΩ Full-Scale Measurement

(a) $VR = \frac{163.85\ k\Omega}{163.85 + 220 + RX} \times 0.64$

(b) $VX = \frac{RX}{\begin{array}{c}163.85\ k\Omega + 220\ \Omega + RX \\ + RX\end{array}} \times 0.64$

(c) "Ramp Up Voltage" = "Ramp Down Voltage"

$$\therefore \frac{VX}{R_I C_I} \times T_I = \frac{VR}{R_I C_I} T_{DE}$$

Where:

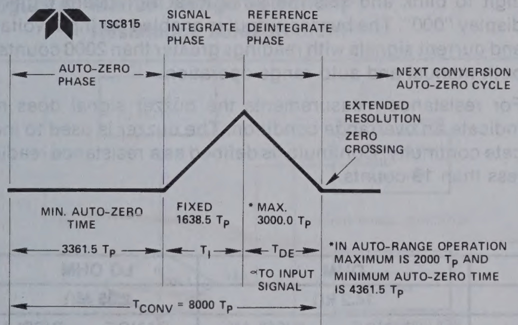
R_I = Integrating Resistor, T_I = Integrate Time

C_I = Integrating Capacitor, T_{DE} = Deintegrate Time

(d) $RX = 163.85 \left(\frac{T_{DE}}{T_I} \right)$

Independent of R_I, C_I or Internal Voltage Reference

Figure 4: Resistance Measurement Accuracy Set by External Standard Resistor


TSC815
SIGNAL INTEGRATE PHASE
REFERENCE DEINTEGRATE PHASE
AUTO-ZERO PHASE
NEXT CONVERSION AUTO-ZERO CYCLE
EXTENDED RESOLUTION
ZERO CROSSING
MIN. AUTO-ZERO TIME
FIXED 1638.5 T_P
* MAX. 3000.0 T_P
3361.5 T_P
T_I
T_{DE}
∝TO INPUT SIGNAL
*IN AUTO-RANGE OPERATION MAXIMUM IS 2000 T_P AND MINIMUM AUTO-ZERO TIME IS 4361.5 T_P
T_{CONV} = 8000 T_P

External Crystal = 32.768 kHz

Internal Clock Period = T_P = 2/32.768 = 61.04 μs

Total Conversion Time = T_{CONV} = 8000 (T_P)

= 488.3 ms ≈ 2 CONV/SEC

Integration Time = T_I = 1638.5 (T_P) = 100.0 ms

Maximum Reference Deintegrate Time

= T_{DE} = 3000 (T_P) = 183.1 ms (Manual, Extended Resolution)

= 2000 (T_P) = 122.1 ms (Auto-Range)

Minimum Auto-Zero Time

= (8000-3000-1638.5) (T_P) = 205.1 ms (Manual, Extended Resolution)

= (8000-2000-1638.5) (T_P) = 266.2 ms (Auto-Range)

Figure 5: Basic TSC815 Conversion Timing

Measurement Options

AC to DC Measurements

In voltage and current measurements the TSC815 can be configured for AC measurements. An on chip operational amplifier and external rectifier components perform the AC to DC conversion.

When power is first applied the TSC815 enters the DC measurement mode. For AC measurements (current or voltage), $\overline{AC}$/DC (Pin 59) is momentarily brought low to digital ground potential; the TSC815 sets-up for AC measurements and the AC liquid crystal display annunciator activates. Toggling $\overline{AC}$/DC low again will return the TSC815 to DC operation.

If the manual operating mode has been selected toggling $\overline{AC}$/DC will reset the TSC815 back to the auto-range mode. In manual mode operation AC or DC operation should be selected first and then the desired range selected.

The minimum AC voltage full-scale voltage range is 2V. The DC full-scale minimum voltage is 200 mV.

AC current measurements are available on the 20 mA and 100 mA full-scale current range.

Conversion Timing

The TSC815 analog-to-digital converter uses the conventional dual slope integrating conversion teghnique with an added phase that automatically eliminates zero offset errors. The TSC815 gives a zero reading with a zero volt input.

The TSC815 is designed to operate with a 32.768 kHz crystal. The 32 kHz crystal is low cost and readily available; it serves as a time base oscillator crystal in many digital clocks. (See External Crystal Sources).

The external clock is divided by two. The internal clock frequency is 16.348 kHz giving a clock period of 61.04 μs. The total conversion — auto-zero phase, signal integrate and reference deintegrate — requires 8000 clock periods or 488.3 ms. There are approximately two complete conversions per second.

The integration time is fixed at 1638.5 clock periods or 100 ms. This gives rejection of 50/60 Hz AC line noise.

The maximum reference deintegrate time, representing a full-scale analog input, is 3000 clock periods or 183.1 ms during manual extended resolution operation. The 3000 counts are available in manual mode, extended resolution operation only. In auto-ranging mode the maximum deintegrate time is 2000 clock periods. The 1000 clock periods are added to the auto-zero phase. An auto-ranging or manual conversion takes 8000 clock periods. After a zero crossing is detected in the reference deintegrate mode, the auto-zero phase is entered.

Figure 5 shows the basic TSC815 timing relationships.

Manual Range Selection

The TSC815 voltage and resistance auto-ranging feature can be disabled by momentarily bringing $\overline{\text{RANGE}}$ (Pin 56) to digital ground potential (Pin 55). When the change from auto-to-manual ranging occurs the first manual range selected is the last range in the auto-ranging mode.

The TSC815 power-up circuit selects auto-range operation initially. Once the manual range option is entered, range changes are made my momentarily grounding the RANGE control input. The TSC815 remains in the manual range mode until the measurement function (voltage or resistance) or measurement option (AC/DC, Ω/LO Ω) changes. This causes the TSC815 to return to auto-ranging operation.

The "Auto" LCD annunciator driver is active only in the auto-range mode.

Table 5 shows typical operation where the manual range selection option is used. Also shown is the extended resolution display format.

Extended Resolution Manual Operation

The TSC815 extends resolution by 50% when operated in the manual range select mode for current, voltage, and resistance measurements. Resolution increases to 3000 counts from 2000 counts. The extended resolution feature operates only on the 2000 kΩ and 2000 V ranges during auto-range operation.

In the extended resolution operating mode readings above 1999 are displayed with a blinking "1" most significant digit. The blinking "1" should be interpreted as the digit 2. The three least significant digits display data normally.

An input overrange condition causes the most significant digit to blink and sets the three least significant digits to display "000". The buzzer output is enabled for input voltage and current signals with readings greater than 2000 counts in both manual and auto-range operation.

For resistance measurements the buzzer signal does not indicate an overrange condition. The buzzer is used to indicate continuity. Continuity is defined as a resistance reading less than 19 counts.

Table 5: Manual Range Operation

INPUT		**DC VOLTS**		**AC VOLTS**		**OHM**		**LO OHM**	
		23.5 V		**18.2 V**		**18.2 kΩ**		**2.35 MΩ**	
		RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY
POWER-ON		200 mV	"1"00.0 mV	2 V	"1".000 V	200 Ω	"1"00.0 Ω	2 kΩ	"1".000 kΩ
AUTO-RANGE OPERATION		2 V	"1".000 V	20 V	18.20 V	2 kΩ	"1".000 kΩ	10 kΩ	"1"0.00 kΩ
		20 V	"1"0.00 V			20 kΩ	18.20 kΩ	200 kΩ	"1"00.0 kΩ
		200 V	23.5 V					2000 kΩ	"1"350 kΩ
	# of RANGE CHANGES ⎺⎽⎺								
	⎺⎽⎺	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY
MANUAL OPERATION	1	200 V	23.5 V	20 V	18.20 V	20 kΩ	18.20 kΩ	2000 kΩ	"1"350 kΩ
	2	200 mV	"1"00.0 mV	2 V	"1".000 V	200 Ω	"1"00.0 Ω	2 kΩ	"1".000 kΩ
	3	2 V	1.000 V	20 V	18.20 V	2 kΩ	"1".000 kΩ	20 kΩ	"1"0.00 kΩ
	4	20 V	"1"3.50 V	200 V	18.2 V	20 kΩ	18.20 kΩ	200 kΩ	"1"00.0 kΩ
	5	200 V	23.5 V	600 V	19 V	200 kΩ	18.2 kΩ	2000 kΩ	"1"350 kΩ
	6	1000 V	24 V	2 V	"1".000 V	2000 kΩ	19 kΩ	2 kΩ	"1".000 kΩ
	7	200 mV	"1"00.0 mV	20 V	18.20 V	200 Ω	"1'"00.0 Ω	20 kΩ	"1"0.00 kΩ
	8	2 V	"1".000 V	200 V	18.2 V	2 kΩ	"1".000 kΩ	200 kΩ	"1"00.0 kΩ

Notes:
1. A flashing MSD is shown as a "1". A flashing MSD indicates the TSC815 is over-ranged if all other digits are zero.
2. The first manual range selected is the last range in the auto-ranging mode.
3. A flashing MSD with a non-zero display indicates the TSC815 has entered the extended resolution operating mode. An additional 1000 counts of resolution is available. This extended operation is available only in manual operation for voltage, resistance and current measurements.
4. ⎺⎽⎺ = momentary ground connection.

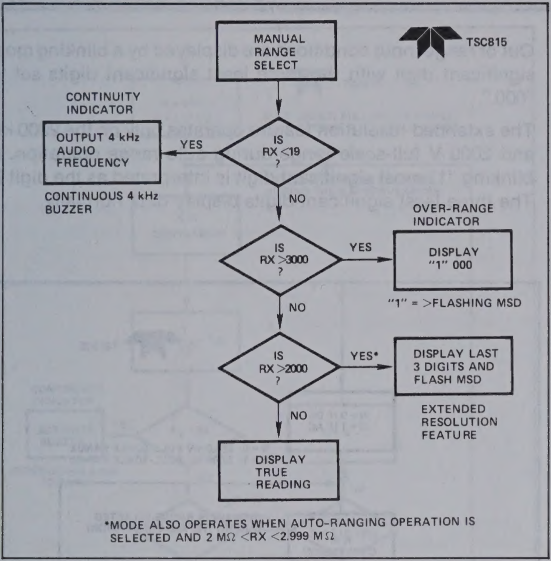

TSC815
MANUAL RANGE SELECT
CONTINUITY INDICATOR
OUTPUT 4 kHz AUDIO FREQUENCY
CONTINUOUS 4 kHz BUZZER
YES
IS RX <19 ?
NO
OVER-RANGE INDICATOR
IS RX >3000 ?
YES
DISPLAY "1" 000
"1" = >FLASHING MSD
NO
IS RX >2000 ?
YES*
DISPLAY LAST 3 DIGITS AND FLASH MSD
EXTENDED RESOLUTION FEATURE
NO
DISPLAY TRUE READING
*MODE ALSO OPERATES WHEN AUTO-RANGING OPERATION IS SELECTED AND 2 MΩ <RX <2.999 MΩ

Figure 6: Manual Range Selection; Resistance Measurement

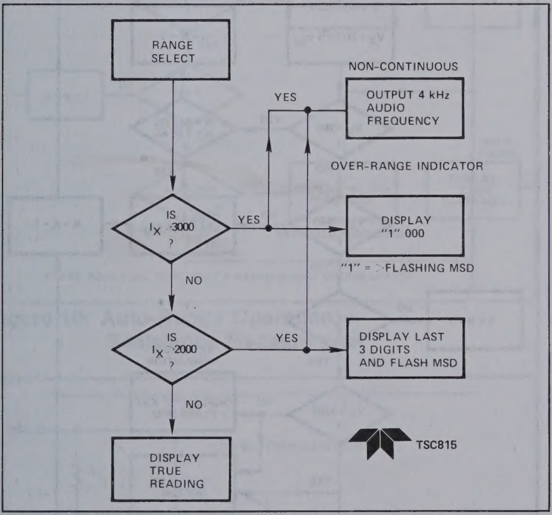

RANGE SELECT
NON-CONTINUOUS
YES
OUTPUT 4 kHz AUDIO FREQUENCY
OVER-RANGE INDICATOR
IS Ix >3000 ?
YES
DISPLAY "1" 000
"1" = >FLASHING MSD
NO
IS Ix >2000 ?
YES
DISPLAY LAST 3 DIGITS AND FLASH MSD
NO
DISPLAY TRUE READING
TSC815

Figure 7: Manual Range Selection; Current Measurement

-MEM Operating Mode

Bringing $\overline{\text{MEM}}$ (Pin 58) momentarily low configures the TSC815 "-MEM" operating mode. The -MEM LCD Annunciator becomes active. In this operating mode subsequent measurements are made relative to the last two digits (≤99) displayed at the time MEM is low. This represents 5% of full-scale. The last two significant digits are stored and subtracted from all the following input conversions.

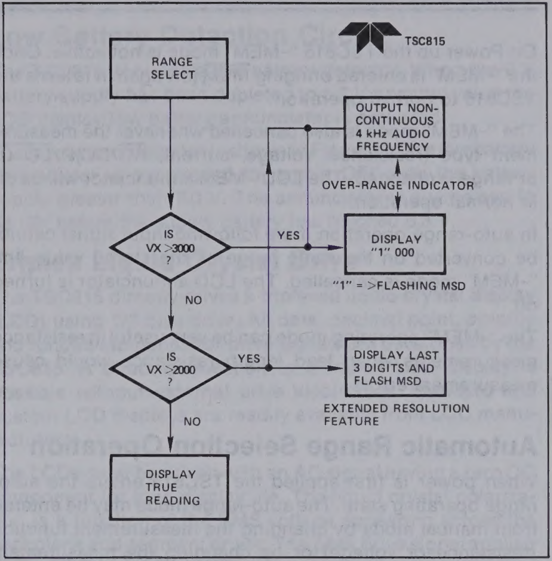

TSC815
RANGE SELECT
OUTPUT NON-CONTINUOUS 4 kHz AUDIO FREQUENCY
OVER-RANGE INDICATOR
IS VX >3000 ?
YES
DISPLAY "1" 000
"1" = >FLASHING MSD
NO
IS VX >2000 ?
YES
DISPLAY LAST 3 DIGITS AND FLASH MSD
EXTENDED RESOLUTION FEATURE
NO
DISPLAY TRUE READING

Figure 8: Manual Range Selection; Voltage Measurement

A few examples clarify operation:

Example 1: In Auto-Ranging

Ri (N) = 18.21 kΩ (20 kΩ Range) = > Display 18.21 kΩ
$\overline{\text{MEM}}$ ‾⊔‾ = > Store 0.21 kΩ

Ri (N+1) = 19.87 kΩ (20 kΩ Range)
= > Display 19.87 - 0.21 = 19.66 kΩ

Ri (N+2) = 22.65 kΩ (200 kΩ Range)
= > Display 22.7 kΩ & $\overline{\text{MEM}}$ Disappears

Example 2: In Fixed Range 200.0 Ω Full-Scale

Ri (N) = 18.2 Ω = > Display 18.2 Ω
$\overline{\text{MEM}}$ ‾⊔‾ = > Store 8.2 Ω

Ri (N+1) = 36.7 Ω
= > Display 36.7 - 8.2 = 28.5 Ω

Ri (N+2) = 5.8 Ω
= > Display 5.8 - 8.2 = -2.4 Ω*

* Will display minus resistance if following input is less than offset stored at fixed range

Example 3: In Fixed Range 20.00 V Full-Scale

Vi (N) = 0.51 V = > Display 0.51 V
$\overline{\text{MEM}}$ ‾⊔‾ = > Store 0.51 V

Vi (N+1) = 3.68 V
= > Display 3.68 - 0.51 = 3.17 V

Vi (N+2) = 0.23 V
= > Display 0.23 - 0.51 = -0.28 V

Vi (N+3) = -5.21 V
= > Display -5.21 - 0.51 = -5.72 V

On Power up the TSC815 "-MEM" mode is not active. Once the "-MEM" is entered bringing $\overline{\text{MEM}}$ low again it returns the TSC815 to normal operation.

The "-MEM" mode is also cancelled whenever the measurement type (resistance, voltage, current, $\overline{\text{AC}}$/DC,Ω/$\overline{\text{LO Ω}}$) or range is changed. The LCD -MEM annunciator will be off in normal operation.

In auto-range operation if the following input signal cannot be converted on the same range as the stored value, the "-MEM" mode is cancelled. The LCD annunciator is turned off.

The "-MEM" operating mode can be very useful in resistance measurements when lead length resistance would cause measurement errors.

Automatic Range Selection Operation

When power is first applied the TSC815 enters the auto-range operating state. The auto-range mode may be entered from manual mode by changing the measurement function (resistance or voltage) or by changing the measurement option ($\overline{\text{AC}}$/DC, Ω/$\overline{\text{LOΩ}}$).

The automatic voltage range selection begins on the most sensitive scale first: 200 mV for DC or 2.000 V for AC measurements. The voltage range selection flow chart is given in Figure 9.

Internal input protection diodes to VCC (Pin 26) and VSSA (Pin 54) clamp the input voltage. The external 10 MΩ input resistance (See Figure 1, R14 and R13) limits current safely in an overrange condition.

The voltage range selection is designed to maximize resolution. For input signals less than 9% of full-scale (count reading <180) the next most sensitive range is selected.

An overrange voltage input condition is flagged whenever the internal count exceeds 2000 by activating the buzzer output (Pin 3). This 4 kHz signal can directly drive a piezo electric acoustic transducer. An out of range input signal causes the 4 kHz signal to be on for 122 ms, off for 122 ms, on for 122 ms, and off for 610 ms (See Figure 15).

During voltage auto-range operation the extended resolution feature operates on the 2000 V range only (See extended resolution operating mode discussion).

The resistance automatic range selection procedure is shown in Figure 10. The 200 Ω range is the first range selected unless the TSC815 low ohms resistance measurement option is selected. In low ohms operation the first full-scale range tried is 2 kΩ.

The resistance range selected maximizes sensitivity. If the conversion results in a reading less than 180 the next most sensitive full-scale range is tried.

If the conversion is less than 19 in auto-range operation a continuous 4 kHz signal is output at BUZ (Pin 3). An overrange input does not activate the buzzer.

Out of range input conditions are displayed by a blinking most significant digit with the three least significant digits set to "000."

The extended resolution feature operates only on the 2000 kΩ and 2000 V full-scale range during auto-range operation. A blinking "1" most significant digit is interpreted as the digit 2. The three least significant digits display data normally.

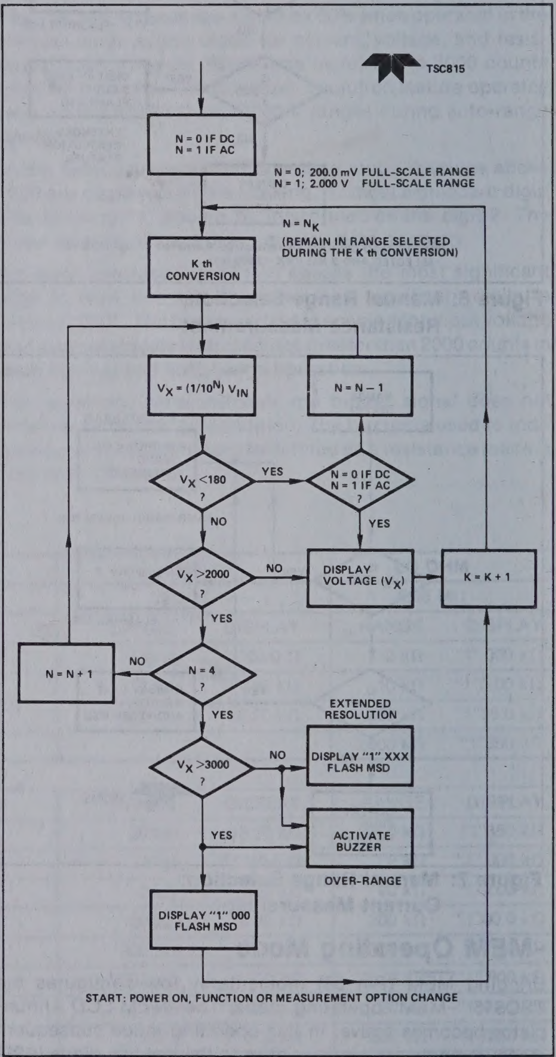

TSC815
N = 0 IF DC
N = 1 IF AC
N = 0; 200.0 mV FULL-SCALE RANGE
N = 1; 2.000 V FULL-SCALE RANGE
N = N_K
(REMAIN IN RANGE SELECTED DURING THE K th CONVERSION)
K th CONVERSION
V_X = (1/10^N) V_IN
N = N − 1
V_X <180 ?
YES
N = 0 IF DC
N = 1 IF AC ?
NO
YES
V_X >2000 ?
NO
DISPLAY VOLTAGE (V_X)
K = K + 1
YES
N = N + 1
NO
N = 4 ?
YES
EXTENDED RESOLUTION
V_X >3000 ?
NO
DISPLAY "1" XXX FLASH MSD
YES
ACTIVATE BUZZER
OVER-RANGE
DISPLAY "1" 000 FLASH MSD
START: POWER ON, FUNCTION OR MEASUREMENT OPTION CHANGE

Figure 9: Auto-Range Operation; Voltage Measurement

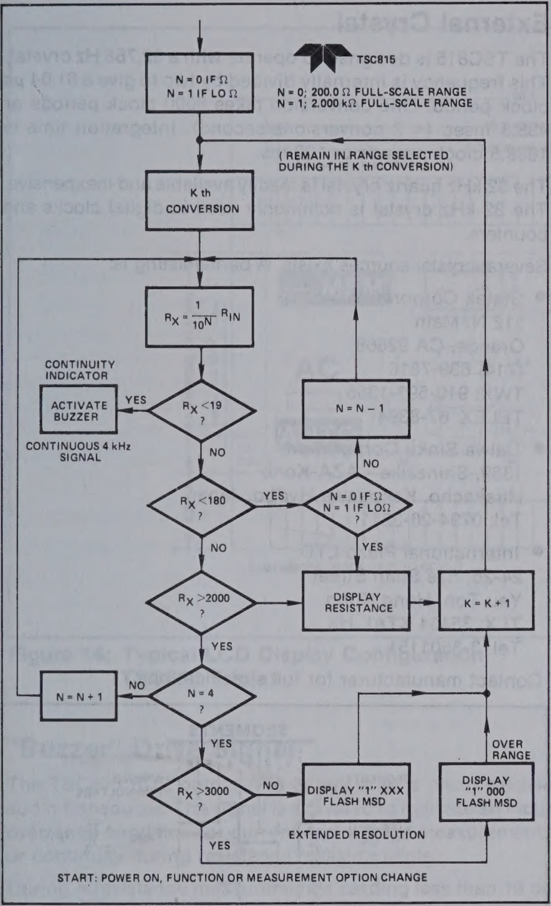

TSC815
N = 0 IF Ω
N = 1 IF LO Ω
N = 0; 200.0 Ω FULL-SCALE RANGE
N = 1; 2.000 kΩ FULL-SCALE RANGE
(REMAIN IN RANGE SELECTED DURING THE K th CONVERSION)
K th CONVERSION
$R_X = \frac{1}{10^N} R_{IN}$
CONTINUITY INDICATOR
ACTIVATE BUZZER
YES
$R_X < 19$?
CONTINUOUS 4 kHz SIGNAL
NO
N = N − 1
NO
$R_X < 180$?
YES
N = 0 IF Ω
N = 1 IF LO Ω ?
NO
YES
$R_X > 2000$?
DISPLAY RESISTANCE
K = K + 1
YES
N = N + 1
NO
N = 4 ?
YES
OVER RANGE
$R_X > 3000$?
NO
DISPLAY "1" XXX FLASH MSD
DISPLAY "1" 000 FLASH MSD
YES
EXTENDED RESOLUTION
START: POWER ON, FUNCTION OR MEASUREMENT OPTION CHANGE

Figure 10: Auto-Range Operation; Resistance Measurement

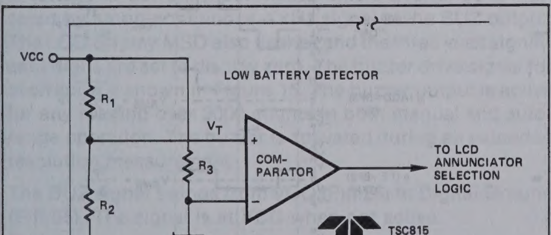

VCC
R_1
LOW BATTERY DETECTOR
V_T
+
COM-PARATOR
−
R_3
TO LCD ANNUNCIATOR SELECTION LOGIC
R_2
TSC815
$V_Z \approx 6.2$ V
$V_T = 7 \times \frac{R_2}{R_1 + R_2} = 6.2$ V
VSSA
LOW BATTERY ANNUNCIATOR DISPLAYED FOR $V_{SUPPLY} < 7$ V

Figure 11: Low Battery Detector

Low Battery Detection Circuit

The TSC815 contains a low battery detector. When the 9 V battery supply has been depleted to a 7 V nominal value the LCD display low battery annunciator is activated.

The low battery detector is shown in Figure 11. The low battery annunciator is guaranteed to remain OFF with the battery supply greater than 7.0 V. The annunciator is guaranteed to be ON before the supply battery has reached 6.3 V.

Triplex Liquid Crystal Drive

The TSC815 directly drives a triplexed liquid crystal display (LCD) using 1/3 bias drive. All data, decimal point, polarity and function annunciator drive signals are developed by the TSC815. A direct connection to a triplex LCD display is possible without external drive electronics. Standard and custom LCD displays are readily available from LCD manufacturers.

The LCDs must be driven with an AC signal having a zero DC component for long display life. The liquid crystal polarization is a function of the RMS voltage appearing across the backplane and segment driver. The peak drive signal applied to the LCD is: VCC-VDISP.

If VDISP, for example, is set at a potential 3 V below VCC the peak drive signal is:

$$Vp = VCC - VDISP = 3\ V$$

An "OFF" LCD segment has an RMS voltage of Vp/3 across it or 1 volt. An "ON" segment has a 0.63 Vp signal across it or 1.92 V for VCC–VDISP = 3 V.

Since the VDISP pin is available the user may adjust the "ON" and "OFF" LCD levels for various manufacturer's displays by changing Vp. Liquid crystal threshold voltage moves down with temperature.

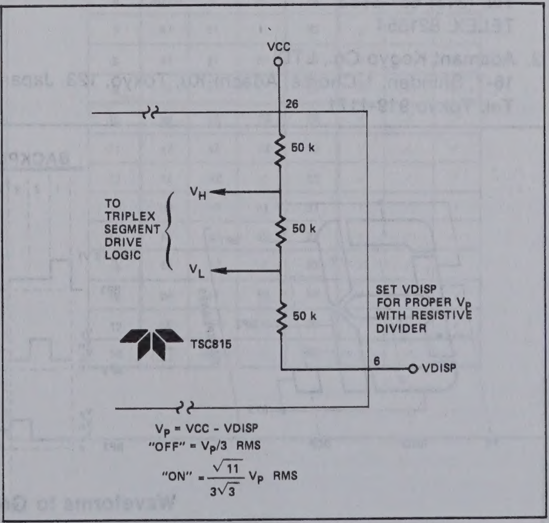

VCC
26
50 k
V_H
TO TRIPLEX SEGMENT DRIVE LOGIC
50 k
V_L
SET VDISP FOR PROPER V_P WITH RESISTIVE DIVIDER
50 k
TSC815
6
VDISP
V_P = VCC - VDISP
"OFF" = $V_P/3$ RMS
"ON" = $\frac{\sqrt{11}}{3\sqrt{3}} V_P$ RMS

Figure 12: 1/3 Bias LCD Drive

"OFF" segments may become visible at high LCD operating temperatures. A voltage with a -5 to -20 mV/° C temperature coefficient can be applied to VDISP to accommodate the liquid crystal temperature operating characteristics if necessary.

The TSC815 internally generates two intermediate LCD drive potentials (V_H & V_L) from a resistive divider (Figure 12) between VCC (Pin 26) and VDISP (Pin 6). The ladder impedance is approximately 150 kΩ. This drive method is commonly known as 1/3 bias. With V_{DISP} connected to digital ground $V_P \approx 5.0$ V.

The intermediate levels are needed so that drive signals giving RMS "ON" and "OFF" levels can be generated. Figure 13 shows a typical drive signal and the resulting wave forms for "ON" and "OFF" RMS voltage levels across a selected LCD element.

LCD Displays

Although most users will design their own custom LCD display, several manufacturers offer standard displays for the TSC815. Figure 14 shows a typical display available from Varitronix.

1. Varitronix Ltd.
   9/F Liven House, 61-63, King Yip Street
   Kwun Tjong, Hong Kong
   Tel: 3-410286
   TELEX: 36643 VTRAX HX

Part No.: VIM 310-1 Pin Connector
VIM 310-2 Elastomer Connector

USA OFFICE:
VL Electronics Inc.
2775 Glendower Ave.
Los Angeles, CA 90027
Tel. (213) 661-8883
TELEX: 821554

2. Adamant Kogyo Co., LTD.
   16-7, Shinden, 1-Chome, Adachi-Ku, Tokyo, 123, Japan
   Tel: Tokyo 919-1171

External Crystal

The TSC815 is designed to operate with a 32,768 Hz crystal. This frequency is internally divided by two to give a 61.04 μs clock period. One conversion takes 8000 clock periods or 488.3 msec (≈ 2 conversions/second). Integration time is 1638.5 clock periods or 100 ms.

The 32 kHz quartz crystal is readily available and inexpensive. The 32 kHz crystal is commonly used in digital clocks and counters.

Several crystal sources exists. A partial listing is:

- Statek Corporation
  512 N. Main
  Orange, CA 92668
  (714) 639-7810
  TWX: 910-593-1355
  TELEX: 67-8394
- Daiwa Sinku Corporation
  1389, Shinzaike - AZA-Kono
  Hirakacho, Kakogawa Hyogo, Japan
  Tel: 0794-26-3211
- International Piezo LTD
  24-26, Sze Shan Street
  Yau Ton, Hong Kong
  TLX: 35454 XTAL HX
  Tel: 3-3501151

Contact manufacturer for full specifications.

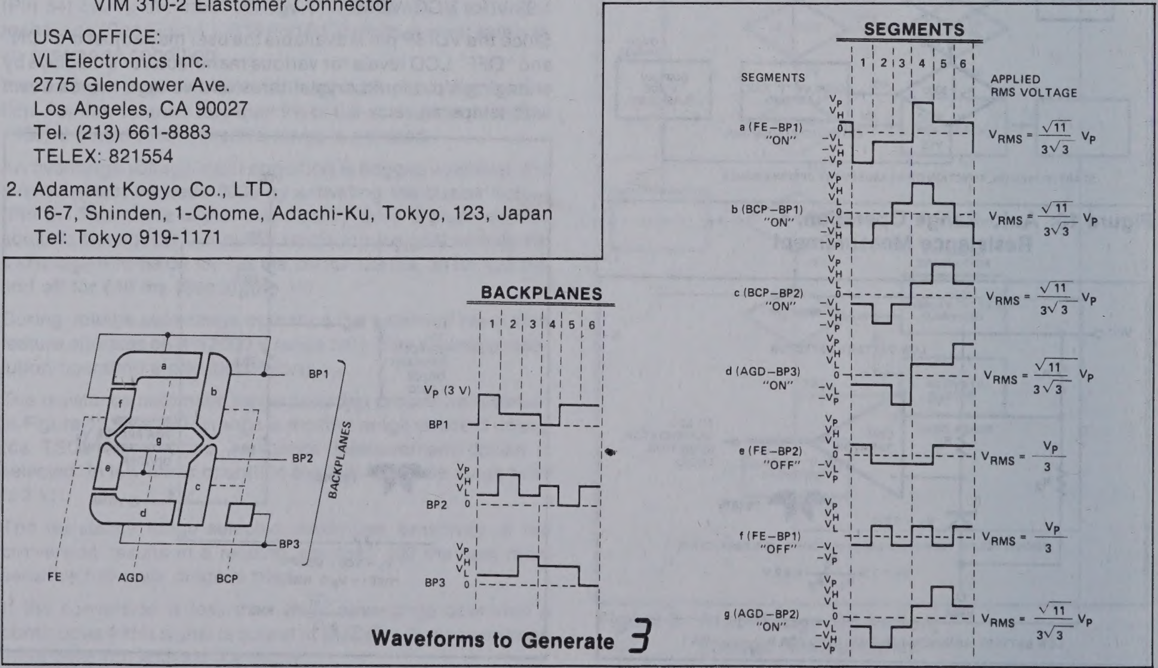

SEGMENTS
1 2 3 4 5 6
SEGMENTS
APPLIED RMS VOLTAGE
a (FE–BP1) "ON"
b (BCP–BP1) "ON"
c (BCP–BP2) "ON"
d (AGD–BP3) "ON"
e (FE–BP2) "OFF"
f (FE–BP1) "OFF"
g (AGD–BP2) "ON"
V_P V_H V_L 0 $-V_L$ $-V_H$ $-V_P$
$V_{RMS} = \frac{\sqrt{11}}{3\sqrt{3}} V_P$
$V_{RMS} = \frac{V_P}{3}$
BACKPLANES
1 2 3 4 5 6
V_P (3 V)
BP1
BP2
BP3
a b c d e f g
FE
AGD
BCP
BACKPLANES
Waveforms to Generate 3

Figure 13: Triplex LCD Drive Waveforms

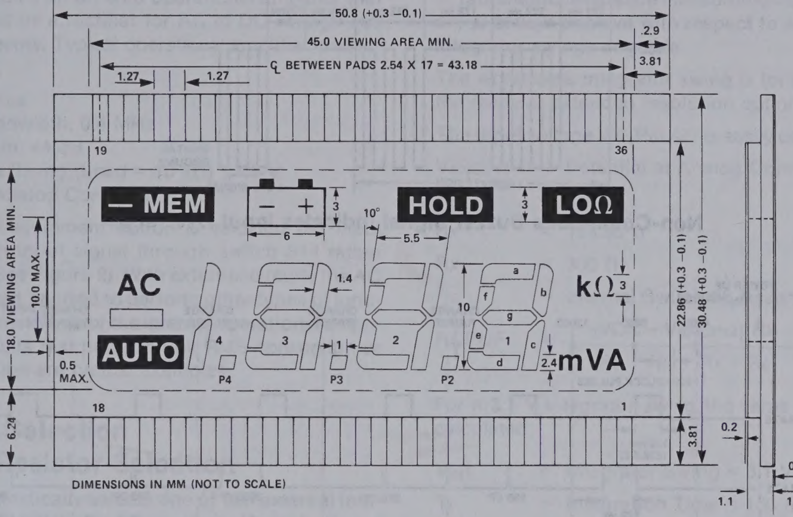

50.8 (+0.3 −0.1)
45.0 VIEWING AREA MIN.
℄ BETWEEN PADS 2.54 X 17 = 43.18
2.9
3.81
1.27
1.27
19
36
— MEM
− +
3
10°
HOLD
3
LOΩ
6
5.5
18.0 VIEWING AREA MIN.
10.0 MAX.
AC
1.4
a
f
b
10
g
kΩ
3
e
1
c
4
3
1
2
AUTO
0.5 MAX.
P4
P3
P2
2.4
mVA
22.86 (+0.3 −0.1)
30.48 (+0.3 −0.1)
18
1
6.24
3.81
0.2
0.2
1.1
1.1
DIMENSIONS IN MM (NOT TO SCALE)

Figure 14: Typical LCD Display Configuration TSC815 Triplex

PAD	BP1	BP2	BP3	PAD	COM1	COM2	COM3
1	BP1	/	/	19	/	/	/
2	/	BP2	/	20	/	/	/
3	/	/	BP3	21	/	/	/
4	/	LOΩ	A	22	/	/	/
5	/	Ω	V	23	/	/	/
6	HOLD	k	m	24	/	/	/
7	b1	c1	/	25	/	/	/
8	a1	g1	d1	26	/	/	/
9	f1	e1	/	27	/	/	/
10	b2	c2	P2	28	/	/	/
11	a2	g2	d2	29	/	/	/
12	f2	e2	/	30	/	/	/
13	b3	c3	P3	31	/	/	/
14	a3	g3	d3	32	/	/	/
15	f3	e3	/	33	/	/	/
16	b4	c4	P4	34	/	/	/
17	AC	▭	AUTO	35	/	/	/
18	🔋	−MEM	/	36	/	/	/

"Buzzer" Drive Signal

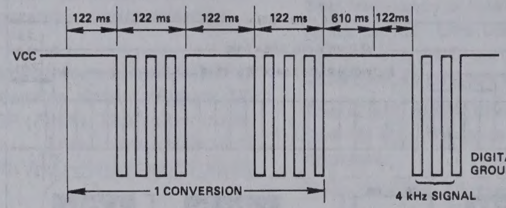
The TSC815 BUZ output (Pin 3) will drive a piezo electric audio transducer. The signal is activated to indicate an input overrange condition for current and voltage measurements or continuity during resistance measurements.

During a resistance measurement a reading less than 19 on any full-scale range causes a continuous 4 kHz signal to be output. This is used as a continuity indication.

A voltage or current input measurement overrange is indicated by a non-continuous 4 kHz signal at the BUZ output. The LCD display MSD also flashes and the three least significant digits are set to display zero. The buzzer drive signal for overrange is shown in Figure 15. The buzzer output is active for any reading over 2000 counts in both manual and auto-range operation. The buzzer is activated during an extended resolution measurement.

The BUZ signal swings from VCC (Pin 26) to Digital Ground (Pin 55). The signal is at VCC when not active.

The buz output is also activated for 15 ms whenever a range change is made in auto-range or manual operation. Changing the type of measurement (voltage, current, or resistance) or measurement option ($\overline{\text{AC}}$/DC, Ω/$\overline{\text{LO}\Omega}$) will also activate the buzzer output for 15 ms. A range change during a current measurement will not activate the buzzer output.


122 ms
122 ms
122 ms
122 ms
610 ms
122ms
VCC
DIGITAL GROUND
1 CONVERSION
4 kHz SIGNAL

Non-Continuous Buzzer Signal Indicates Input Overrange

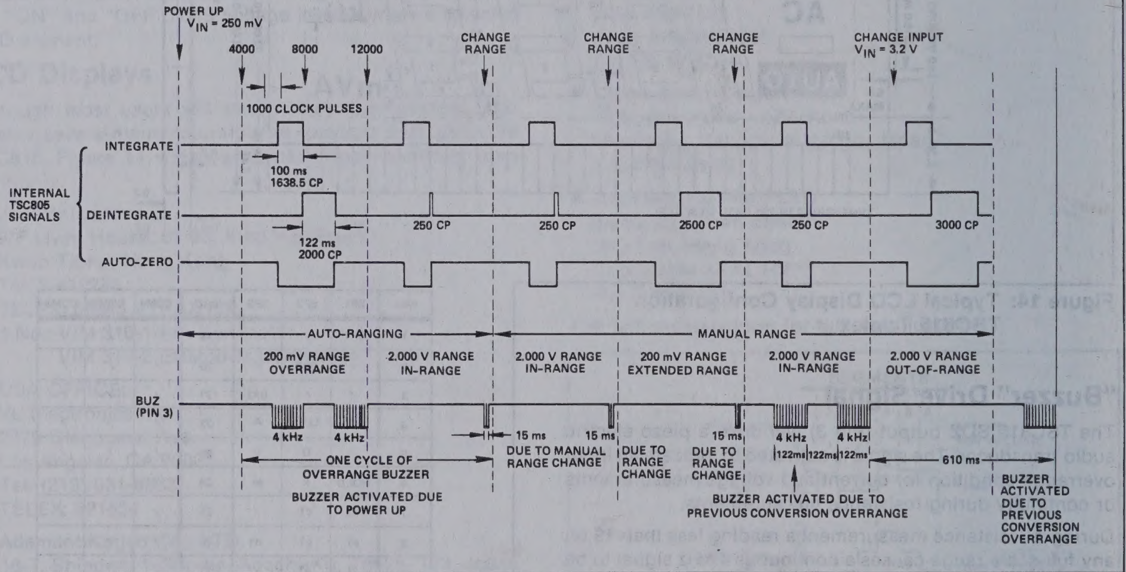

POWER UP
V_{IN} = 250 mV
4000
8000
12000
CHANGE RANGE
CHANGE RANGE
CHANGE RANGE
CHANGE INPUT V_{IN} = 3.2 V
1000 CLOCK PULSES
INTEGRATE
100 ms 1638.5 CP
INTERNAL TSC805 SIGNALS
DEINTEGRATE
250 CP
250 CP
2500 CP
250 CP
3000 CP
122 ms 2000 CP
AUTO-ZERO
AUTO-RANGING
MANUAL RANGE
200 mV RANGE OVERRANGE
2.000 V RANGE IN-RANGE
2.000 V RANGE IN-RANGE
200 mV RANGE EXTENDED RANGE
2.000 V RANGE IN-RANGE
2.000 V RANGE OUT-OF-RANGE
BUZ (PIN 3)
4 kHz
4 kHz
15 ms
15 ms
15 ms
4 kHz
4 kHz
122ms 122ms 122ms
610 ms
DUE TO MANUAL RANGE CHANGE
DUE TO RANGE CHANGE
DUE TO RANGE CHANGE
ONE CYCLE OF OVERRANGE BUZZER
BUZZER ACTIVATED DUE TO POWER UP
BUZZER ACTIVATED DUE TO PREVIOUS CONVERSION OVERRANGE
BUZZER ACTIVATED DUE TO PREVIOUS CONVERSION OVERRANGE

Figure 15: TSC815 Timing Waveform for Buzzer Output

Vendors for piezo electric audio transducers are:

1. Gulton Industries
   Piezo Products Division
   212 Durham Avenue
   Metuchen, New Jersey 08840
   (201) 548-2800
   Typical P/N's: 102-95NS, 101-FB-00
2. Taiyo Yuden (USA) Inc.
   Arlington Center
   714 West Algonquin Road
   Arlington Hts., Ill. 60005
   Typical P/N's: CB27BB, CB20BB, CB355BB

Display Decimal Point Selection

The TSC815 provides a decimal point LCD drive signal. The decimal point position is a function of the selected full-scale range as shown in Table 6.

Table 6: Decimal Point Selection

	1 • 9	• 9	• 9
Full-Scale Range	**DP3**	**DP2**	**DP1**
2000 V, 2000 kΩ	OFF	OFF	OFF
200.0 V, 200.0 kΩ	OFF	OFF	ON
20.00 V, 20.00 kΩ	OFF	ON	OFF
2.000 V, 2.000 kΩ	ON	OFF	OFF
200.0 mV, 200.0 Ω	OFF	OFF	ON
20.00 mA	OFF	ON	OFF
200.0 mA	OFF	OFF	ON

AC to DC Converter Operational Amplifier

The TSC815 contains an on chip operational amplifier that may be connected as a rectifier for AC to DC voltage and current measurements. Typical operational amplifier characteristics are:

- Slew Rate: 1 V/μs
- Unity Gain Bandwidth: 0.4 MHz
- Open Loop Gain: 44 dB
- Output Voltage Swing (Load = 10 kΩ) ±1.5 V (Reference to Analog Common)

When the AC measurement option is selected the input buffer receives an input signal through switch S14 rather than switch S11 (See Figure 2). With external circuits the AC operating mode can be used to perform other types of functions within the constraints of the internal operational amplifier. External circuits that perform true RMS conversion or a peak hold function are typical examples.

Component Selection
Integration Resistor Selection

The TSC815 automatically selects one of two external integration resistors. RVIBUF (Pin 52) is selected for voltage and current measurement. RΩBUF (Pin 51) is selected for resistance measurements.

RVIBUF Selection (PIN 52)

In auto-range operation the TSC815 operates with a 200 mV maximum full-scale potential at VI (Pin 42). Resistive dividers at VR2 (Pin 39), VR3 (Pin 38), VR4 (Pin 41) and VR5 (Pin 40) are automatically switched to maintain the 200 mV full-scale potential.

In manual mode the extended operating mode is activated giving a 300 mV full-scale potential at VI (Pin 42).

The integrator output swing should be maximized but saturations must be avoided. The integrator will swing within 0.45 V of VCC (Pin 26) and 0.5 V of VSSA (Pin 54) without saturating. A ±2 V swing is suggested. The value of RVIBUF is easily calculated assuming a worst case extended resolution input signal:

V_{INT} = Integrator Swing = ±2 V
T_I = Integration Time = 100 ms
C_I = Integration Capacitor = 0.1 μf
V_{MAX} = Maximum Input at V_I = 300 mV

$$\text{RVIBUF} = \frac{V_{MAX}(T_I)}{V_{INT}\,(C_I)} \approx 150\ \text{k}\Omega$$

RΩBUF Selection (Pin 51)

In ratiometric resistance measurements the signal at Rx (Pin 47) is always positive with respect to analog common. The integrator swings negative.

The worst case integrator swing is for the 200 Ω range with the manual, extended resolution option.

The input voltage VX (Pin 47) is easily calculated (Figure 16).

V_{ANCOM} = Potential at Analog Common ≈ 2.7 V
R_8 = 220 Ω
R_1 = 163.85 Ω
R_X = 300 Ω
R_S = Internal Switch 33 Resistance ≈ 600 Ω

$$R\Omega BUF = \frac{(VCC - V_{ANCOM})\ Rx}{(Rx + R_S + R_1 + R_8)} = 0.63\ \text{V}$$

For a 3.1 V integrator swing the value of RΩBUF is easily calculated:

V_{INT} = Integrator Swing = 3.1 V
T_I = Integration Time = 100 ms
C_I = Integration Cap. = 0.1 μf
Rx Max = 300 Ω
Vx Max = 700 mV

$$R\Omega BUF = \frac{(Vx\ MAX)\ (T_I)}{C_I\ (V_{INT})} \approx 220\ \text{k}\Omega$$

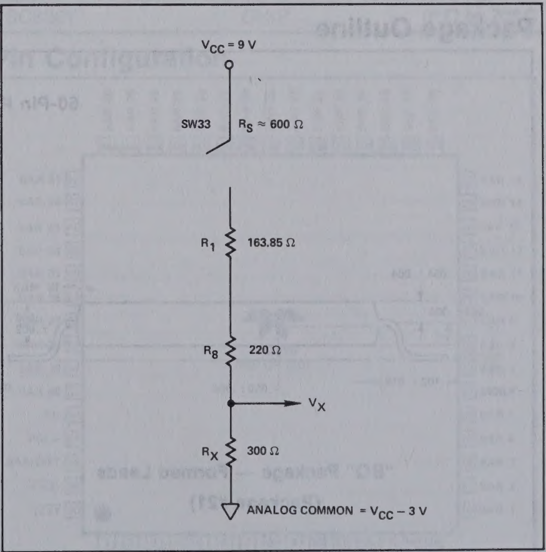


Figure 16: RΩBUF Calculation (200 Ω Manual Operation)

With a low battery voltage of 6.6 V analog common will be approximately 3.6 V above the negative supply terminal. With the integrator swinging down from analog common toward the negative supply a 3.1 V swing will set the integrator output to 0.5 V above the negative supply.

CINT, CAZ and CREF Capacitors

The integration capacitor, CINT, must have low dielectric absorption. A 0.1 uf polypropylene capacitor is suggested. The auto-zero capacitor, CAZ, and reference capacitor, CREF, should be selected for low leakage and dielectric absorption. Polystyrene capacitors are good choices.

Reference Voltage Adjustment

The TSC815 contains a low temperature drift internal voltage reference. The analog common potential (Pin 27) is established by this reference. Maximum drift is a low 75 ppm/° C. Analog common is designed to be approximately 2.6 V below VCC (Pin 26). A resistive divider (R18/R19, Figure 1) sets the TSC815 reference input voltage (REFHI, Pin 32) to approximately 163.85 mV.

With an input voltage near full-scale on the 200 mV range, R19 is adjusted for the proper reading.

Display Hold Feature

The LCD display will not be updated when HOLD (Pin 57) is connected to Ground (Pin 55). Conversions are made but the display is not updated. A HOLD Mode LCD annunciator is activated when HOLD is low.

The LCD HOLD annunciator is activated through the triplex LCD driver signal at Pin 12.

Flat Package Socket

Sockets suitable for prototype work are available. A USA source is:

Nepenthe Distribution
2471 East Bayshore
Suite 520
Palo Alto, CA 94303
(415) 856-9332
TWX: 910-373-2060

(a) "BQ" Socket Part No.: IC51-064-042 BQ

(b) "SQ" Socket Part No.: IC51-064-042 SQ

Resistive Ladder Networks

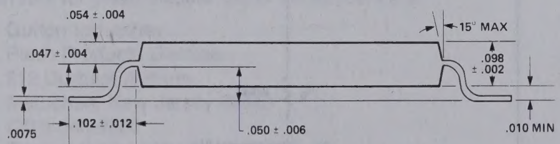
Resistor attenuator networks for voltage and resistance measurement are available from:

Caddock Electronics
1717 Chicago Avenue
Riverside, CA 92507
TEL: (714) 788-1700
TWX: 910-332-6108

Attenuator Accuracy	Attenuator Type	Caddock Part Number
0.1%	Voltage	1776-C441
0.25%	Voltage	1776-C44
0.25%	Resistance	T 1794-204-1

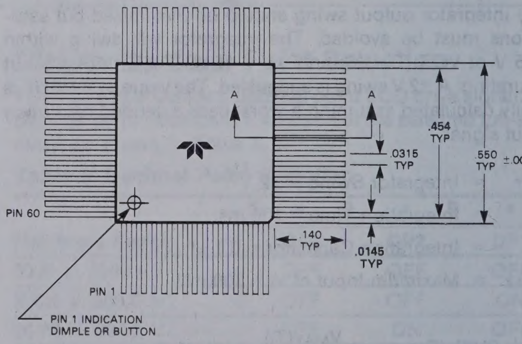
Package Outline

60-Pin Plastic Flat Package



"BQ" Package — Formed Leads

(Package #21)



"SQ" Package — Unformed Leads

(Package #22)

TSC826
A/D Converter With Bar Graph Display Output
- 2.5% Resolution
- Direct LCD Drive
- Bar/Dot Display Format

General Description

In many applications a graphical display is preferred over a digital display. Knowing a process or system operates, for example, within design limits is more valuable than a direct system variable readout. A bar or moving dot display supplies information precisely without requiring further interpretation by the viewer.

The TSC826 is a complete analog-to-digital converter with direct liquid crystal (LCD) display drive. The 40 LCD data segments plus zero driver give a 2.5% resolution bar display. Full-scale differential input voltage range extends from 20 mV to 2 V. The TSC826 sensitivity is 500 μV. A low drift 35 ppm/°C internal reference, LCD backplane oscillator and driver, input polarity LCD driver, and overrange LCD driver make designs simple and low cost. The CMOS design requires only 125 μA from a 9 V battery. In +5 V systems a TSC7660 DC to DC converter can supply the –5 V supply. The differential analog input leakage is a low 10 pA.

Two display formats are possible. The BAR mode display is like a "thermometer" scale. The LCD segment driver that equals the input plus all below it are on. The DOT mode activates only the segment equal to the input. In either mode the polarity signal is active for negative input signals. An overrange input signal causes the display to flash and activates the overrange annunciator. A hold mode can be selected that freezes the display and prevents updating.

The dual slope integrating conversion method with auto-zero phase maximizes noise immunity and eliminates zero-scale adjustment potentiometers. Zero-scale drift is a low 5 μV/°C. Conversion rate is typically 5 per second and is adjustable by a single external resistor.

A compact, 0.5" square, flat package minimizes PC board area. The high pin count LSI package makes multiplexed LCD displays unnecessary. Low cost, direct drive LCD displays offer the widest viewing angle and are readily available. A standard display is available now for TSC826 prototyping work.

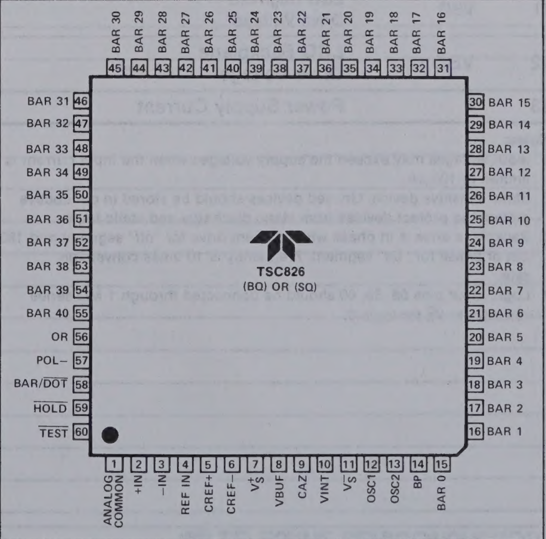
Features

- Bipolar A/D Conversion
- 2.5% Resolution
- Direct LCD Display Drive
- "Thermometer" Bar or Dot Display
- 40 Data Segments Plus Zero
- Overrange Plus Polarity Indication
- Precision On-Chip Reference .... 35 ppm/°C
- Differential Analog Input
- Low Input Leakage .... 10 pA
- Display Flashes on Overrange
- Display Hold Mode
- Auto-Zero Cycle Eliminates Zero Adjust Potentiometer
- 9 V Battery Operation
- Low Power Consumption .... 1.1 mW
- 20 mV to 2.0 V Full-Scale Operation
- Non-Multiplexed LCD Drive for Maximum Viewing Angle

Ordering Information

Part No.	Package	Temperature Range
TSC826CBQ	60-Pin Plastic Quad Flat Package Formed Leads	0°C to 70°C
TSC826CSQ	60-Pin Plastic Quad Flat Package Straight Leads	0°C to 70°C
TSC826Y	CHIP	0°C to 70°C

Pin Configuration


BAR 30 45
BAR 29 44
BAR 28 43
BAR 27 42
BAR 26 41
BAR 25 40
BAR 24 39
BAR 23 38
BAR 22 37
BAR 21 36
BAR 20 35
BAR 19 34
BAR 18 33
BAR 17 32
BAR 16 31
BAR 31 46
BAR 32 47
BAR 33 48
BAR 34 49
BAR 35 50
BAR 36 51
BAR 37 52
BAR 38 53
BAR 39 54
BAR 40 55
OR 56
POL– 57
BAR/$\overline{DOT}$ 58
$\overline{HOLD}$ 59
$\overline{TEST}$ 60
30 BAR 15
29 BAR 14
28 BAR 13
27 BAR 12
26 BAR 11
25 BAR 10
24 BAR 9
23 BAR 8
22 BAR 7
21 BAR 6
20 BAR 5
19 BAR 4
18 BAR 3
17 BAR 2
16 BAR 1
1 ANALOG COMMON
2 +IN
3 –IN
4 REF IN
5 CREF+
6 CREF–
7 V_S^+
8 VBUF
9 CAZ
10 VINT
11 V_S^-
12 OSC1
13 OSC2
14 BP
15 BAR 0
TSC826
(BQ) OR (SQ)

A/D Converter With Bar Graph Display Output

- **2.5% Resolution**
- **Direct LCD Drive**
- **Bar/Dot Display Format**

TSC826

Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) .... 15 V
Analog Input Voltage (either input)[1] .... V^+ to V^-
Package Power Dissipation
Flat Package (B, S) .... 500 mW
Operating Temperature
("C" Devices) .... 0° C to +70° C
Storage Temperature .... -65° C to +160° C
Lead Temperature (Soldering, 60 sec) .... 300° C

Electrical Characteristics: $V_S = 9$ V, ROSC = 430 kΩ, $T_A = 25°$C, Full-Scale = 20 mV unless otherwise stated.

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC826 MIN	TSC826 TYP	TSC826 MAX	UNIT
1	—	Zero Input Reading	$V_{IN} = 0.0$ V	-0	±0	+0	Display
2	—	Zero Reading Drift	$V_{IN} = 0.0$ V $0°C \le T_A \le 70°C$	—	0.2	1	μV/° C
3	NL	Linearity Error	Max Deviation From Best Straight Line	-1	0.5	+1	Count
4	—	Rollover Error	$-V_{IN} = +V_{IN}$	-1	0	+1	Count
5	EN	Noise	$V_{IN} = 0$ V	—	60	—	μV_{P-P}
6	ILK	Input Leakage Current	$V_{IN} = 0$ V	—	10	20	pA
7	CMRR	Common-Mode Rejection Ratio	VCM = ±1 V $V_{IN} = 0$ V	—	50	—	μV/V
8	—	Scale Factor Temperature Coefficient	$0 \le T_A \le 70°C$ External Ref. Temperature Coefficient = 0 ppm/° C	—	1	—	ppm/° C
9	VCTC	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ $0°C \le T_A \le 70°C$	—	35	100	ppm/° C
10		Analog Common Voltage	250 kΩ Between Common and V_S^+	2.7	2.9	3.35	V
11	VSD	LCD Segment Drive Voltage		4	5	6	V_{P-P}
12	VBD	LCD Backplane Drive Voltage		4	5	6	V_{P-P}
13	I	Power Supply Current		—	125	175	μA

Notes:

1. Input voltages may exceed the supply voltages when the input current is limited to 100 μA.
2. Static sensitive device. Unused devices should be stored in conductive material to protect devices from static discharge and static fields.
3. Backplane drive is in phase with segment drive for "off" segment and 180° C out of phase for "on" segment. Frequency is 10 times conversion rate.
4. Logic input pins 58, 59, 60 should be connected through 1 MΩ series resistors to V_S^- for logic 0.

A/D Converter With Bar Graph Display Output

- **2.5% Resolution**
- **Direct LCD Drive**
- **Bar/Dot Display Format**

TSC826

Pin Description and Function

PIN NO.	NAME	DESCRIPTION
1	Analog Common	Establishes the internal analog ground point. Analog common is set to 2.9 V below the positive supply by an internal zener reference circuit. The voltage difference between V_S^+ and analog-common can be used to supply the TSC826 voltage reference input at REF IN (Pin 4).
2	+IN	Positive analog signal input.
3	-In	Negative analog signal input.
4	REF IN	Reference voltage positive input. Measured relative to analog-common. REF IN ≈ Full-Scale/2.
5	C_{REF} +	Reference capacitor connection.
6	C_{REF} -	Reference capacitor connection.
7	V_S^+	Positive supply terminal.
8	VBUF	Buffer output. Integration resistor connection.
9	CAZ	Negative comparator input. Auto-zero capacitor connection.
10	VINT	Integrator output. Integration capacitor connection.
11	V_S^-	Negative supply terminal.
12	OSC1	Oscillator resistor (R_{OSC}) connection.
13	OSC2	Oscillator resistor (R_{OSC}) connection.
14	BP	LCD Backplane driver.
15	BAR 0	LCD Segment driver: Bar 0
16	1	1
17	2	2
18	3	3
19	4	4
20	5	5
21	6	6
22	7	7
23	8	8
24	9	9
25	10	10
26	11	11
27	12	12
28	13	13
29	14	14
30	15	15
31	16	16
32	17	17
33	18	18
34	19	19
35	20	20
36	21	21
37	22	22
38	23	23

Pin Description and Function (Cont.)

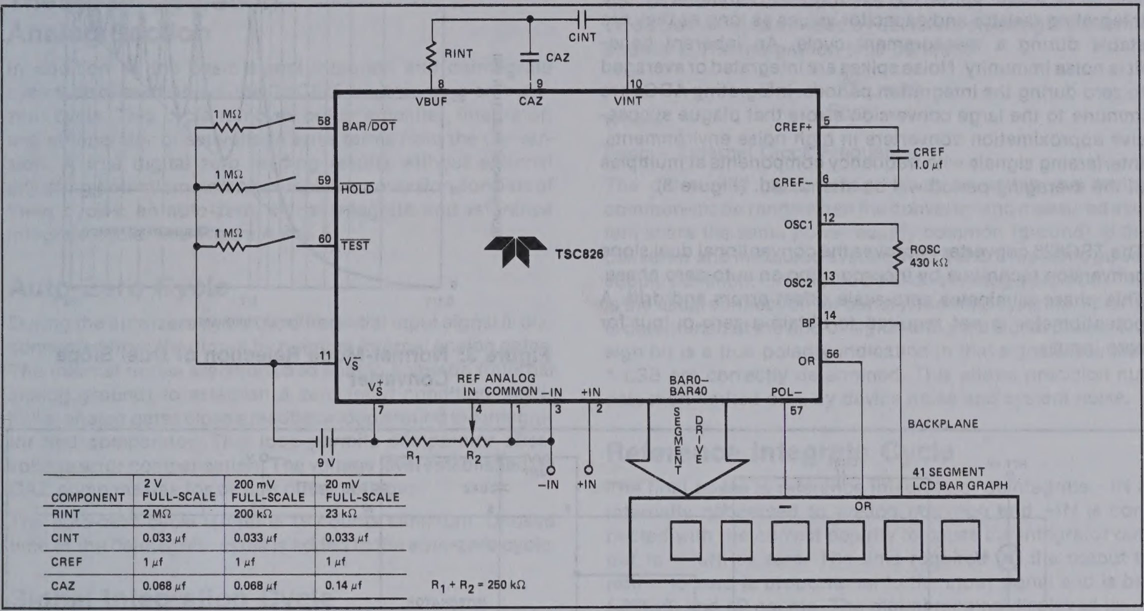
PIN NO.	NAME	DESCRIPTION
39	BAR 24	BAR Segment driver: Bar 24
40	25	25
41	26	26
42	27	27
43	28	28
44	29	29
45	30	30
46	31	31
47	32	32
48	33	33
49	34	34
50	35	35
51	36	36
52	37	37
53	38	38
54	39	39
55	40	40
56	OR	LCD segment driver that indicates input out-of-range condition.
57	POL-	LCD segment driver that indicates input signal is negative.
58	BAR/$\overline{\text{DOT}}$	Input logic signal that selects bar or dot display format. Normally in bar mode. Connect to $V_{\overline{S}}$ through 1MΩ resistor for Dot format.
59	$\overline{\text{HOLD}}$	Input logic signal that prevents display from changing. Pulled high internally to inactive state. Connect to $V_{\overline{S}}$ through 1MΩ series resistor for HOLD mode operation.
60	$\overline{\text{TEST}}$	Input logic signal. Sets TSC805 to BAR display mode. Bar 0 to 40, plus OR flash on and off. The POL- LCD driver is on. Pulled high internally to inactive state. Connect to $V_{\overline{S}}$ with 1 MΩ series resistor to activate.

A/D Converter With Bar Graph Display Output

- **2.5% Resolution**
- **Direct LCD Drive**
- **Bar/Dot Display Format**

TSC826

Typical TSC826 Circuit Connection (Figure 1)


CINT
RINT
CAZ
8
VBUF
9
CAZ
10
VINT
1 MΩ
58
BAR/DOT
1 MΩ
59
HOLD
1 MΩ
60
TEST
TSC826
CREF+
5
CREF
1.0 µf
CREF–
6
OSC1
12
ROSC
430 kΩ
OSC2
13
14
BP
56
OR
11
V_S^-
V_S^+
REF ANALOG
IN COMMON
–IN
+IN
7
4
1
3
2
BAR0–
BAR40
POL–
57
SEGMENT DRIVE
BACKPLANE
9 V
R1
R2
–IN
+IN
41 SEGMENT
LCD BAR GRAPH
–
OR

COMPONENT	2 V FULL-SCALE	200 mV FULL-SCALE	20 mV FULL-SCALE
RINT	2 MΩ	200 kΩ	23 kΩ
CINT	0.033 µf	0.033 µf	0.033 µf
CREF	1 µf	1 µf	1 µf
CAZ	0.068 µf	0.068 µf	0.14 µf

$R_1 + R_2 = 250\ k\Omega$

Dual Slope Conversion Principles

The TSC826 is a dual slope, integrating analog-to-digital converter. The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}). (Figure 2).

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal reference voltage and integration time:

$$\frac{1}{RC}\int_{0}^{T_{SI}} V_{IN}(t)\,dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage

V_{SI} = Signal Integration Time (Fixed)

T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}: $V_{IN} = V_R \dfrac{T_{RI}}{T_{SI}}$

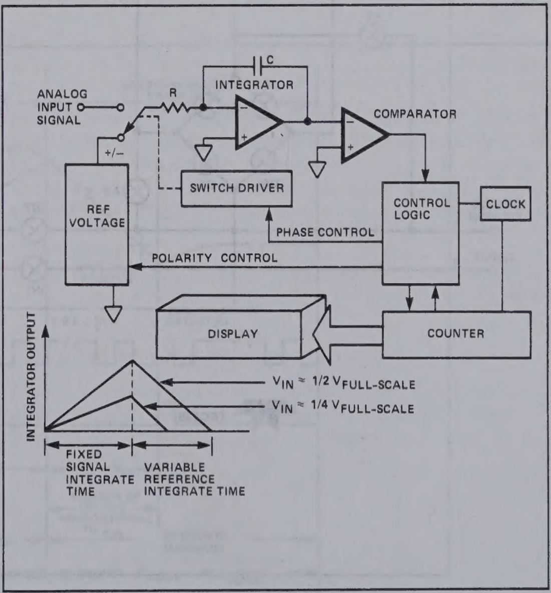

C
INTEGRATOR
ANALOG
INPUT
SIGNAL
R
COMPARATOR
+/–
SWITCH DRIVER
REF
VOLTAGE
CONTROL
LOGIC
CLOCK
PHASE CONTROL
POLARITY CONTROL
DISPLAY
COUNTER
INTEGRATOR OUTPUT
$V_{IN} \approx 1/2\ V_{FULL-SCALE}$
$V_{IN} \approx 1/4\ V_{FULL-SCALE}$
FIXED
SIGNAL
INTEGRATE
TIME
VARIABLE
REFERENCE
INTEGRATE TIME

Figure 2: Basic Dual Slope Converter

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfereing signals with frequency components at multiples of the averaging period will be attenuated. (Figure 3).

The TSC826 converter improves the conventional dual slope conversion technique by incorporating an auto-zero phase. This phase eliminates zero-scale offset errors and drift. A potentiometer is not required to obtain a zero output for zero input.

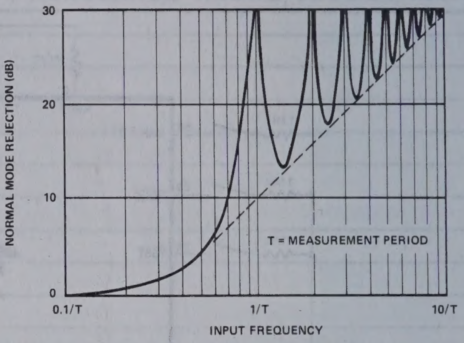


Figure 3: Normal-Mode Rejection of Dual Slope Converter

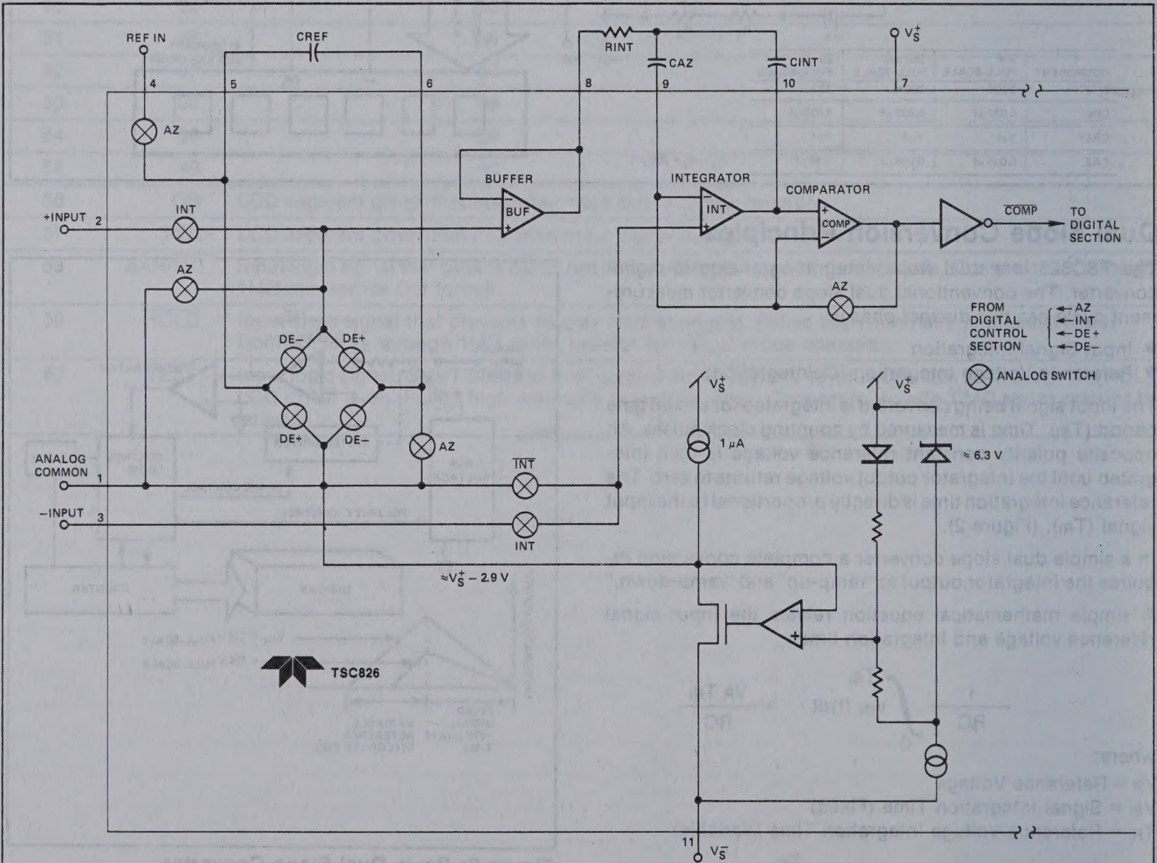

REF IN
CREF
RINT
CAZ
CINT
V_S^+
4
5
6
8
9
10
7
AZ
BUFFER
BUF
INTEGRATOR
INT
COMPARATOR
COMP
$\overline{COMP}$
TO DIGITAL SECTION
+INPUT 2
INT
AZ
DE−
DE+
DE+
DE−
AZ
AZ
ANALOG COMMON 1
−INPUT 3
$\overline{INT}$
INT
$\approx V_S^+ - 2.9$ V
FROM DIGITAL CONTROL SECTION
AZ
INT
DE+
DE−
ANALOG SWITCH
V_S^+
V_S^+
1 µA
≈ 6.3 V
11
V_S^-
TSC826

Figure 4: TSC826 Analog Section

Theory of Operation Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed above the TSC826 incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference integrate cycle. See Figure 4 and 5.

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (internal analog ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on CAZ compensates for device offset voltages.

The auto-zero cycle length is 19 counts minimum. Unused time in the deintegrate cycle is added to the auto-zero cycle.

Signal Integration Cycle

The auto-zero loop is opened and the internal differential inputs connect to +IN and -IN. The differential input signal is integrated for a fixed time period. The TSC826 signal integration period is 20 clock periods or counts. The externally set clock frequency is devided by 32 before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{32}{F_{OSC}} \times 20$$

Where:

F_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, -IN should be tied to analog-common. This is the usual connection for battery operated systems. Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and system noise.

Reference Integrate Cycle

The final phase is reference integrate or deintegrate. -IN is internally connected to analog common and +IN is connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 40 counts. The digital reading displayed is:

$$20\,\frac{V_{IN}}{V_{REF}}$$

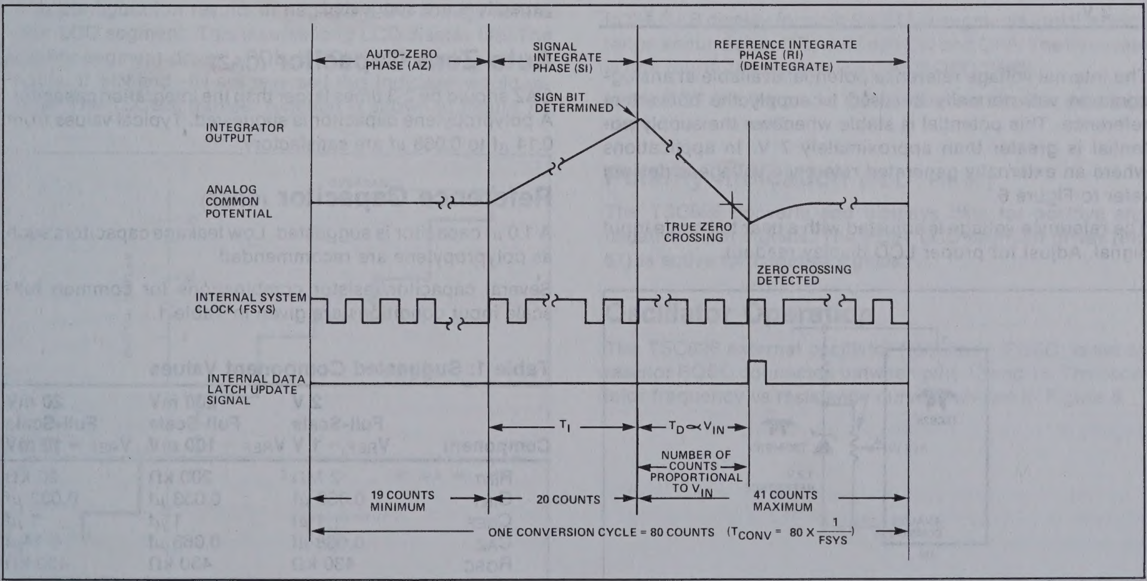

AUTO-ZERO PHASE (AZ)
SIGNAL INTEGRATE PHASE (SI)
REFERENCE INTEGRATE PHASE (RI) (DEINTEGRATE)
SIGN BIT DETERMINED
INTEGRATOR OUTPUT
ANALOG COMMON POTENTIAL
TRUE ZERO CROSSING
ZERO CROSSING DETECTED
INTERNAL SYSTEM CLOCK (FSYS)
INTERNAL DATA LATCH UPDATE SIGNAL
T_I
$T_D \propto V_{IN}$
NUMBER OF COUNTS PROPORTIONAL TO V_{IN}
19 COUNTS MINIMUM
20 COUNTS
41 COUNTS MAXIMUM
ONE CONVERSION CYCLE = 80 COUNTS ($T_{CONV} = 80 \times \frac{1}{F_{SYS}}$)

Figure 5: TSC826 Conversion Has Three Phases

System Timing

The oscillator frequency is divided by 32 prior to clocking the internal counters. The three phase measurement cycle takes a total of 80 clock pulses. The 80 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 19 to 59 Counts
  For signals less than full-scale the auto-zero phase is assigned the unused reference integrate time period.
- Signal Integrate: 20 Counts
  This time period is fixed. The integration period is:

$$T_{SI} = 20 \left[\frac{32}{F_{OSC}} \right]$$

Where F_{OSC} is the externally set clock frequency.

- Reference Integrate: 0 to 41 Counts

Reference Voltage Selection

A full-scale reading requires the input signal be twice the reference voltage. The reference potential is measured between REF IN (Pin 4) and Analog-Common (Pin 1).

Required Full-Scale Voltage	**V_{REF}**
20 mV	10 mV
2 V	1 V

The internal voltage reference potential available at analog-common will normally be used to supply the converters reference. This potential is stable whenever the supply potential is greater than approximately 7 V. In applications where an externally generated reference voltage is desired refer to Figure 6.

The reference voltage is adjusted with a near full-scale input signal. Adjust for proper LCD display readout.

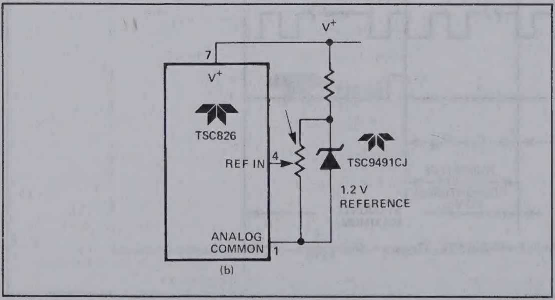


Figure 6: External Reference

Component Value Selection

Integrating Resistor (RINT)

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 1 μA drive current with minimal linearity error. RINT is easily calculated for a 1 μA full-scale current:

$$R_{INT} = \frac{\text{Full-Scale Input Voltage (V)}}{1 \times 10^{-6}} = \frac{VFS}{1 \times 10^{-6}}$$

Where: VFS = Full-Scale Analog Input

Integrating Capacitor (CINT)

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.4 V of V_S^+ or V_S^- without saturating.

The integrating capacitor is easily calculated:

$$C_{INT} = \frac{VFS}{RINT} \left(\frac{640}{FOSC \times VINT} \right)$$

Where: VINT = Integrator Swing
FOSC = Oscillator Frequency

The integrating capacitor should be selected for low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are suggested.

Auto-Zero Capacitor (CAZ)

CAZ should be 2-3 times larger than the integration capacitor. A polypropylene capacitor is suggested. Typical values from 0.14 μf to 0.068 μf are satisfactory.

Reference Capacitor (CREF)

A 1.0 μf capacitor is suggested. Low leakage capacitors such as polypropylene are recommended.

Several capacitor/resistor combinations for common full-scale input conditions are given in Table 1.

Table 1: Suggested Component Values

Component	**2 V Full-Scale $V_{REF} \approx 1$ V**	**200 mV Full-Scale $V_{REF} \approx 100$ mV**	**20 mV Full-Scale $V_{REF} \approx 10$ mV**
R_{INT}	2 MΩ	200 kΩ	20 kΩ
C_{INT}	0.033 μf	0.033 μf	0.033 μf
C_{REF}	1 μf	1 μf	1 μf
C_{AZ}	0.068 μf	0.068 μf	0.14 μf
R_{OSC}	430 kΩ	430 kΩ	430 kΩ

1. Approximately 5 conversions/sec.

Differential Signal Inputs (+IN (Pin 2), -IN (Pin 3))

The TSC826 is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). The typical range is $V^+ - 1.0$ to $V^- + 1$ V. Common-mode voltages are removed from the system when the TSC826 operates from a battery or floating power source (Isolated form measured system) and -IN is connected to analog-common (V_{COM}).

In systems where common-mode voltages exist the TSC826 72 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM}. For such applications, the integrator output swing can be reduced below the recommended 2.0 V full-scale swing. The integrator output will swing within 0.3 V of V_S^+ or V_S^- without increased linearity error.

Digital Section

The TSC826 contains all the segment drivers necessary to drive a liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 256. A 430 kΩ OSC gets the backplane frequency to approximately 55 Hz with a 5 V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF." An out-of-phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver, -POL, is "ON" for negative analog inputs. If +IN and -IN are reversed this indicator would reverse. The TSC826 transfer function is shown in Figure 7.

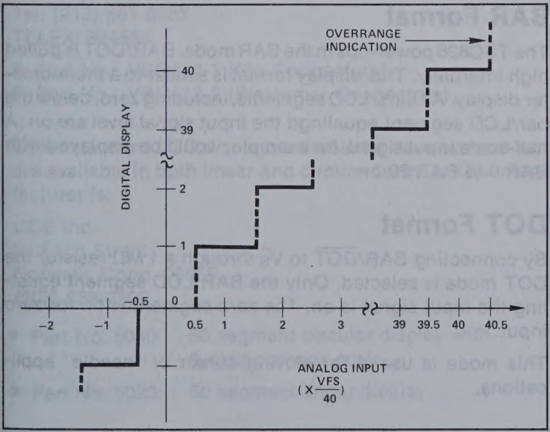


Figure 7: TSC826 Transfer Function

BAR/$\overline{\text{DOT}}$ Input (Pin 58)

The BAR/$\overline{\text{DOT}}$ input allows the user to select the display format. The TSC826 powers up in the BAR mode. Select the DOT display format by connecting BAR/$\overline{\text{DOT}}$ to the negative supply (Pin 11) through a 1 MΩ resistor.

$\overline{\text{HOLD}}$ Input (Pin 59)

The TSC826 data output latches are not updated at the end of each conversion if $\overline{\text{HOLD}}$ is tied to the negative supply (Pin 11) through a 1 MΩ series resistor. The LCD display continuously displays the previous conversion result.

The $\overline{\text{HOLD}}$ pin is normally pulled high by an internal pull-up.

$\overline{\text{TEST}}$ Input (Pin 60)

The TSC826 enters a test mode with the $\overline{\text{TEST}}$ input connected to the negative supply (Pin 11). The connection must be made through a 1 MΩ resistor. The $\overline{\text{TEST}}$ input is normally internally pulled high. A low input sets the output data latch to all ones. The BAR display mode is set. The 41 LCD output segments (zero plus 40 data segments) and overrange annunciator flash on and off at 1/4 the conversion rate. The polarity annunciator (POL-) segment will be on but not flashing.

Overrange Display Operation (OR, Pin 56)

An out-of-range input signal will be indicated on the LCD display by the OR annunciator driver (Pin 56) becoming active.

In the BAR display formate the 41 bar segments and the overrange annunciator, OR, will flash ON and OFF. The flash rate is one fourth the conversion rate (FOSC/2560).

In the DOT display mode, OR`flashes and all other data segment drivers are off.

Polarity Indication (POL-, Pin 57)

The TSC826 converts and displays data for positive and negative input signals. The POL- LCD segment driver (Pin 57) is active for negative signals.

Oscillator Operation

The TSC826 external oscillator frequency, FOSC, is set by resistor ROSC connected between pins 12 and 13. The oscillator frequency vs resistance curve is shown in Figure 8.

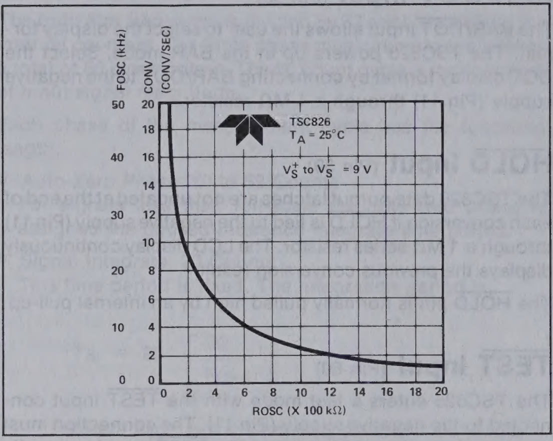


Figure 8: Oscillator Frequency vs. ROSC

FOSC is divided by 32 to provide an internal system clock, FSYS. Each conversion requires 80 internal clock cycles. The internal system clock is divided by 8 to provide the LCD backplane drive frequency. The display flash rate during an input out-of-range signal is set by dividing FSYS by 320. (See Figure 9)

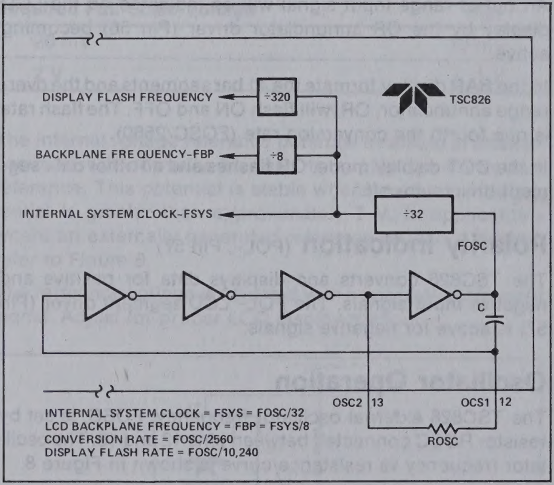

DISPLAY FLASH FREQUENCY
÷320
TSC826
BACKPLANE FREQUENCY-FBP
÷8
INTERNAL SYSTEM CLOCK-FSYS
÷32
FOSC
C
OSC2 13
OCS1 12
ROSC
INTERNAL SYSTEM CLOCK = FSYS = FOSC/32
LCD BACKPLANE FREQUENCY = FBP = FSYS/8
CONVERSION RATE = FOSC/2560
DISPLAY FLASH RATE = FOSC/10,240

Figure 9: Internal Oscillator Operation

The internal oscillator may be bypassed by driving OSCI (Pin 12) with an external signal generator. OSC2 (Pin 13) should be left unconnected.

The oscillator should swing from V_S^+ to V_S^- in single supply operation (Figure 10A). In dual supply operation the signal should swing from power supply ground to V_S^+.

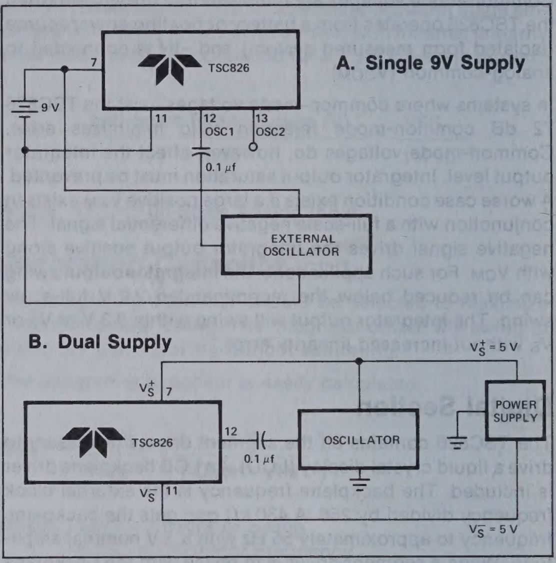

A. Single 9V Supply
TSC826
7
9 V
11
12
OSC1
13
OSC2
0.1 µf
EXTERNAL OSCILLATOR
B. Dual Supply
V_S^+ = 5 V
V_S^+ 7
TSC826
12
0.1 µf
OSCILLATOR
POWER SUPPLY
V_S^- 11
V_S^- = 5 V

Figure 10: External Oscillator Connection

LCD Display Format

The input signal can be displayed in two formats (Figure 11). The BAR/$\overline{\text{DOT}}$ input (Pin 58) selects the format. The TSC826 measurement cycle operates identically for either mode.

BAR Format

The TSC826 power-ups in the BAR mode. BAR/$\overline{\text{DOT}}$ is pulled high internally. This display format is similar to a thermometer display. All bars/LCD segments, including zero, below the bar/LCD segment equalingd the input signal level are on. A half-scale input signal, for example, would be displayed with BAR 0 to BAR 20 on.

DOT Format

By connecting BAR/$\overline{\text{DOT}}$ to V_S^- through a 1 MΩ resistor the DOT mode is selected. Only the BAR LCD segment equalling the input signal is on. The zero segment is on for zero input.

This mode is useful for moving cursor or "needle" applications.

A. BAR MODE

	1. INPUT = 0		2. INPUT = 5% of FULL-SCALE	
BAR 4	▭	OFF	▭	OFF
BAR 3	▭	OFF	▭	OFF
BAR 2	▭	OFF	▨	ON
BAR 1	▭	OFF	▨	ON
BAR 0	▨	ON	▨	ON

B. DOT MODE

	1. INPUT = 0		2. INPUT = 5% of FULL-SCALE	
BAR 4	▭	OFF	▭	OFF
BAR 3	▭	OFF	▭	OFF
BAR 2	▭	OFF	▨	ON
BAR 1	▭	OFF	▭	OFF
BAR 0	▨	ON	▭	OFF

Figure 11: Display Option Formats

LCD Displays

Most end products will use a custom LCD display for final production. Custom LCD displays are low cost and available from all manufacturers. The TSC826 interfaces to non-multiplexed LCD displays. A backplane driver is included on chip.

To speed initial evaluation and prototype work a standard TSC826 LCD display is available from Varitronix.

Varitronix Ltd.
9/F Linen House, 61-63, King Yip Street
Kwun Tjong, Hong Kong
Tel: 3-410286
TELEX: 36643 VTRAX HX

USA Office:
VL Electronics Inc.
2775 Glendower Avenue
Los Angeles, CA 900027
Tel: (213) 661-8883
TELEX: 821554

- Part No.: VBG412-1 (Pin Connectors)
- Part No.: VBG412-2 (Elastomer Connectors)

Other standard LCD displays suitable for development work are available in both linear and circular formats. One manufacturer is:

UCE Inc.
24 Fitch Street
Norwalk, Conn. 06855
(203) 838-7509

- Part No. 5040: 50 segment circular display with 3 digit numeric scale.
- Part No. 5020: 50 segment linear display.

LCD Backplane Driver (Pin 14)

Additional drive electronics is not required to interface the TSC826 to an LCD display. The TSC826 has an on-chip backplane generator and driver. The backplane frequency is:

$$F_{BP} = F_{OSC}/256$$

Figure 12 gives typical backplane driver rise/fall time vs backplane capacitance.

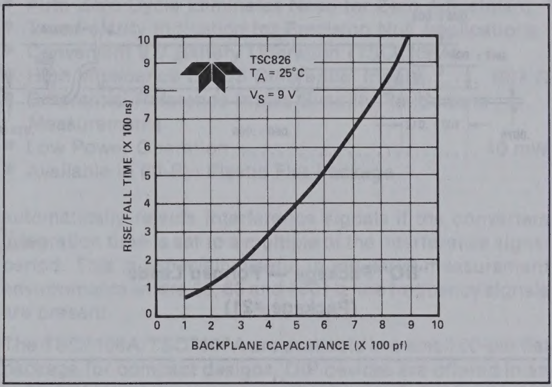


Figure 12: Backplane Driver Rise/Fall Time vs Capacitance

Flat Package Socket

Sockets suitable for prototype work are available. A USA source is:

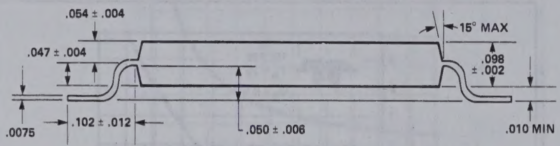
Nepenthe Distribution
2471 East Bayshore
Suite 520
Palo Alto, California 94303
(415) 856-9332
TWX: 910-373-2060

(a) "BQ" Socket Part No.: IC51-064-042 BQ

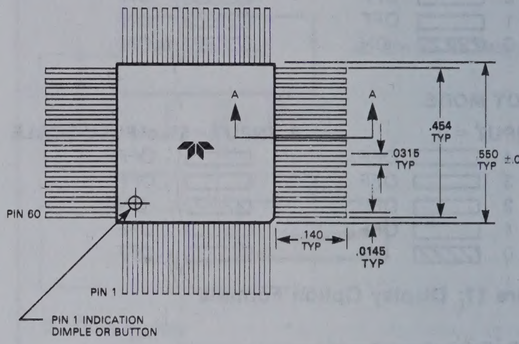
(b) "SQ" Socket Part No.: IC51-064-042 SQ

Package Outline

60-Pin Plastic Flat Package


.054 ± .004
15° MAX
.047 ± .004
.098
± .002
.0075
.102 ± .012
.050 ± .006
.010 MIN

"BQ" Package — Formed Leads
(Package #21)


A
A
.454
TYP
.0315
TYP
.550 ±.005
TYP
PIN 60
.140
TYP
.0145
TYP
PIN 1
PIN 1 INDICATION
DIMPLE OR BUTTON

"SQ" Package — Unformed Leads
(Package #22)

TELEDYNE SEMICONDUCTOR

TSC7106A (LCD Drive)
TSC7107A (LED Drive)
3 1/2 Digit A/D Converter
• Low Drift Internal Reference
• Automatic Zero Correction

General Description

The TSC7106A and TSC7107A 3 1/2 digit direct display drive analog-to-digital converters allow existing 7106/7107 based systems to be upgraded. Each device offers a precision internal voltage reference featuring a 20 ppm/° C typical, 50 ppm° C maximum temperature drift coefficient. This represents a 4 to 7 times improvement over similar 3 1/2 digit converters. Existing 7106 or 7107 based systems may be upgraded without changing external passive component values. The need for a costly, space consuming external reference is removed. The TSC7107A drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment. A low cost, high resolution indicating meter requires only a display, four resistors, and four capacitors. The TSC7106A low power drain and 9 V battery operation make it suitable for portable applications.

The TSC7106A/TSC7107A reduces linearity error to less than 1 count. Rollover error — the difference in readings for equal magnitude but opposite polarity input signals — is below ± 1 count. High impedance differential inputs offer 1 pA leakage current and a 10^{12} Ω input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μVp-p noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

The TSC7106A/TSC7107A dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The TSC7106A/TSC7107A are available in a small 60-pin flat package for compact designs. DIP devices are offered in an industrial temperature range and with burn-in lasting for 160 hours at +125° C.

Where long battery life is needed see the TSC7126 or the TSC7126A data sheets.

Features

- Internal Reference with Low Temperature Drift .... 20 ppm/° C Typical
  50 ppm/° C Maximum
- Drives LCD or LED Displays Directly
- Guaranteed Zero Reading with Zero Input
- Low Noise for Stable Display
- Auto-Zero Cycle Eliminates Need for Zero Adjustment
- True Polarity Indication for Precision Null Applications
- Convenient 9 V Battery Operation (TSC7106A)
- High Impedance CMOS Differential Inputs ..... 10^{12} Ω
- Differential Reference Inputs Simplify Ratiometric Measurements
- Low Power Operation .... 10 mW
- Available in 60-Pin Plastic Flat Package

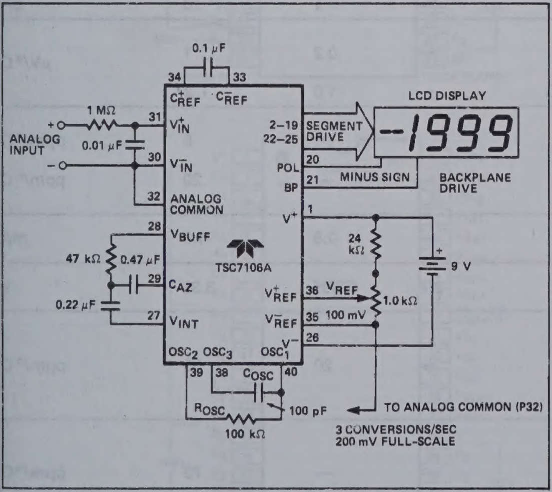
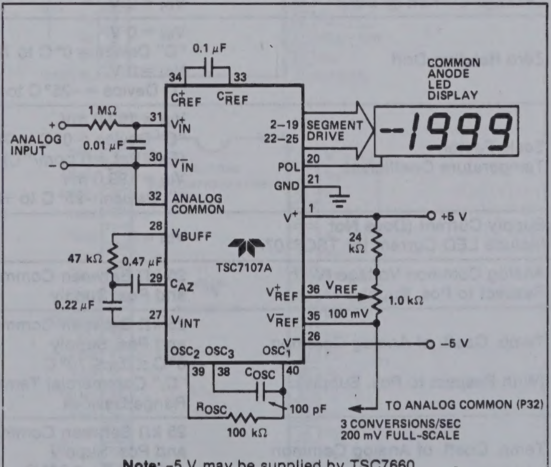

0.1 μF
34
33
C^+_{REF}
C^-_{REF}
1 MΩ
+
ANALOG INPUT
−
0.01 μF
31
V^+_{IN}
30
V^-_{IN}
32
ANALOG COMMON
2–19
22–25
SEGMENT DRIVE
LCD DISPLAY
-1999
POL
20
BP
21
MINUS SIGN
BACKPLANE DRIVE
1
V^+
28
V_{BUFF}
47 kΩ
0.47 μF
29
C_{AZ}
0.22 μF
27
V_{INT}
TSC7106A
24 kΩ
9 V
36
V_{REF}
V^+_{REF}
35
V^-_{REF}
100 mV
1.0 kΩ
26
V^-
OSC_2
OSC_3
OSC_1
39
38
C_{OSC}
40
R_{OSC}
100 pF
100 kΩ
TO ANALOG COMMON (P32)
3 CONVERSIONS/SEC
200 mV FULL-SCALE

Figure 1: Typical TSC7106A Operating Circuit


0.1 μF
34
33
C^+_{REF}
C^-_{REF}
COMMON ANODE LED DISPLAY
1 MΩ
+
ANALOG INPUT
−
0.01 μF
31
V^+_{IN}
30
V^-_{IN}
32
ANALOG COMMON
2–19
22–25
SEGMENT DRIVE
-1999
POL
20
GND
21
1
V^+
+5 V
28
V_{BUFF}
47 kΩ
0.47 μF
29
C_{AZ}
0.22 μF
27
V_{INT}
TSC7107A
24 kΩ
36
V_{REF}
V^+_{REF}
35
V^-_{REF}
100 mV
1.0 kΩ
26
V^-
−5 V
OSC_2
OSC_3
OSC_1
39
38
C_{OSC}
40
R_{OSC}
100 pF
100 kΩ
TO ANALOG COMMON (P32)
3 CONVERSIONS/SEC
200 mV FULL-SCALE

Note: -5 V may be supplied by TSC7660.

Figure 2: Typical TSC7107A Operating Circuit

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Absolute Maximum Ratings

TSC7106A

Supply Voltage (V^+ to V^-)	15 V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	Test to V^+
Power Dissipation (Note 2)	
CerDIP Package	1000 mW
Plastic Package	800 mW
Operating Temperature	
"C" Devices	0° C to +70° C
"I" Devices	-25° C to +85° C
Storage Temperature	-65° C to +160° C
Lead Temperature (Soldering, 60 sec)	300° C

TSC7107A

Supply Voltage	
V^+	+6 V
V^-	-9 V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	GND to V^+
Power Dissipation (Note 2)	
CerDIP Package	1000 mW
Plastic Package	800 mW
Operating Temperature	
"C" Devices	0° C to +70° C
"I" Devices	-25° C to +85° C
Storage Temperature	-65° C to +160° C
Lead Temperature (Soldering, 60 sec)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

Electrical Characteristics (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF} V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \simeq 200.0$ mV	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1 V, V_{IN} = 0 V. Full-Scale = 200.0 mV	—	50	—	µV/V
Noise (Pk - Pk Value Not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 200.0 mV	—	15	—	µV
Leakage Current @ Input	V_{IN} = 0 V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 V "C" Device = 0° C to 70° C V_{IN} = 0 V "I" Device = -25° C to +85° C	— —	0.2 1.0	1 2	µV/° C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, "C" Device = 0° C to 70° C (Ext. Ref = 0 ppm/° C) V_{IN} = 199.0 mV "I" Device: -25° C to +85° C	 —	1 —	5 20	ppm/° C ppm/° C
Supply Current (Does Not Include LED Current for TSC7107A)	V_{IN} = 0	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	2.7	3.05	3.35	V
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply 0° C ≤ T_A ≤ 70° C "C," Commercial Temp. Range Devices	—	20	50	ppm/° C
Temp. Coeff. of Analog Common (with Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply -25° C ≤ T_A ≤ 85° C "I," Industrial Temp. Range Devices	—	—	75	ppm/° C
TSC7106A ONLY Pk - Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V

3 1/2 Digit A/D Converter

- **Low Drift Internal Reference**
- **Automatic Zero Correction**

TSC7106A (LCD Drive)
TSC7107A (LED Drive)

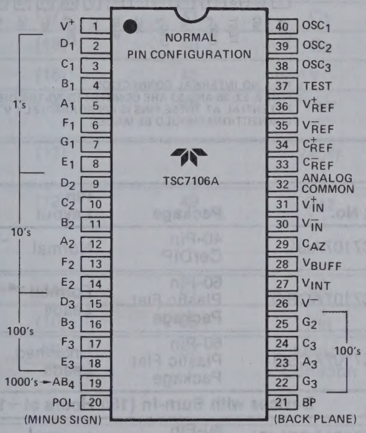
Electrical Characteristics (Note 3)

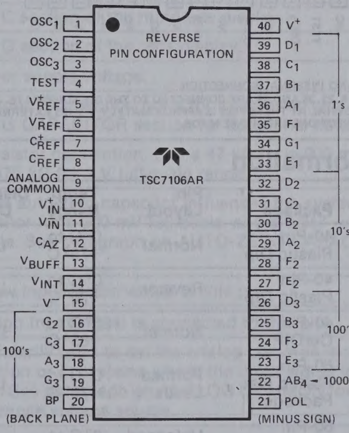
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
TSC7106A ONLY Pk - Pk Backplane Drive Voltage (Note 5)	V^+ to $V^- = 9$ V	4	5	6	V
TSC7107A ONLY Segment Sinking Current (Except Pin 19)	$V^+ = 5.0$ V Segment Voltage = 3 V	5	8.0	—	mA
TSC7107A ONLY Segment Sinking Current (Pin 19 Only)	$V^+ = 5.0$ V Segment Voltage = 3 V	10	16	—	mA

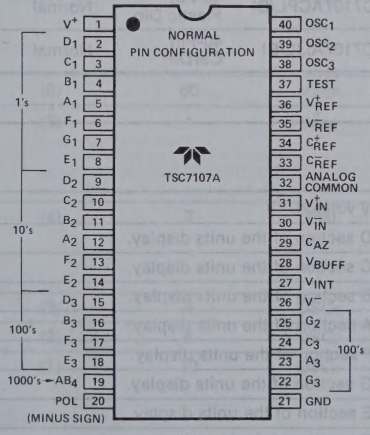
NOTES:

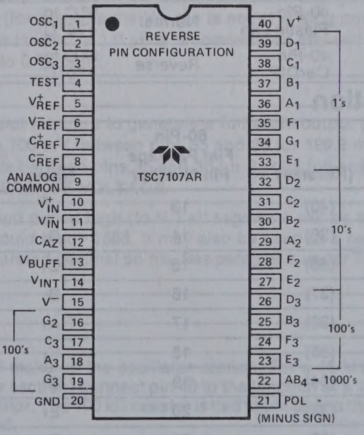
1. Input voltages may exceed the supply voltages provided the input current is limited to ± 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless other wise noted, specifications apply to both the TSC7106A and TSC7107A at $T_A = 25°$ C, $f_{CLOCK} = 48$ kHz. TSC7106A is tested in the circuit of Figure 1. TSC7107A is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average dc component is less than 50 mV.

Pin Configuration

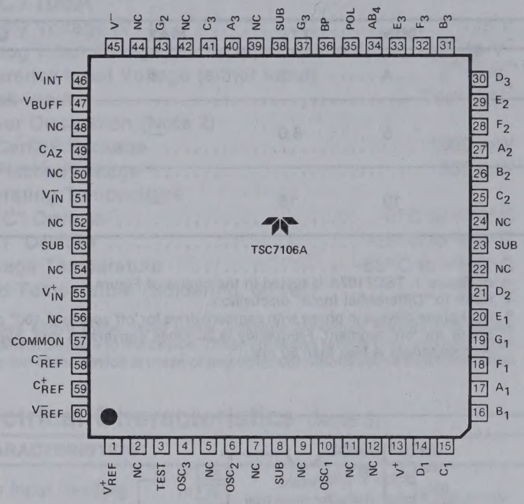

NORMAL
PIN CONFIGURATION
TSC7106A
V^+ 1
D_1 2
C_1 3
B_1 4
A_1 5
F_1 6
G_1 7
E_1 8
D_2 9
C_2 10
B_2 11
A_2 12
F_2 13
E_2 14
D_3 15
B_3 16
F_3 17
E_3 18
1000's ← AB_4 19
POL 20
(MINUS SIGN)
1's
10's
100's
40 OSC_1
39 OSC_2
38 OSC_3
37 TEST
36 V^+_{REF}
35 V^-_{REF}
34 C^+_{REF}
33 C^-_{REF}
32 ANALOG COMMON
31 V^+_{IN}
30 V^-_{IN}
29 C_{AZ}
28 V_{BUFF}
27 V_{INT}
26 V^-
25 G_2
24 C_3
23 A_3
22 G_3
21 BP
(BACK PLANE)
100's


REVERSE
PIN CONFIGURATION
TSC7106AR
OSC_1 1
OSC_2 2
OSC_3 3
TEST 4
V^+_{REF} 5
V^-_{REF} 6
C^+_{REF} 7
C^-_{REF} 8
ANALOG COMMON 9
V^+_{IN} 10
V^-_{IN} 11
C_{AZ} 12
V_{BUFF} 13
V_{INT} 14
V^- 15
G_2 16
C_3 17
A_3 18
G_3 19
BP 20
(BACK PLANE)
100's
40 V^+
39 D_1
38 C_1
37 B_1
36 A_1
35 F_1
34 G_1
33 E_1
32 D_2
31 C_2
30 B_2
29 A_2
28 F_2
27 E_2
26 D_3
25 B_3
24 F_3
23 E_3
22 AB_4 → 1000's
21 POL
(MINUS SIGN)
1's
10's
100's

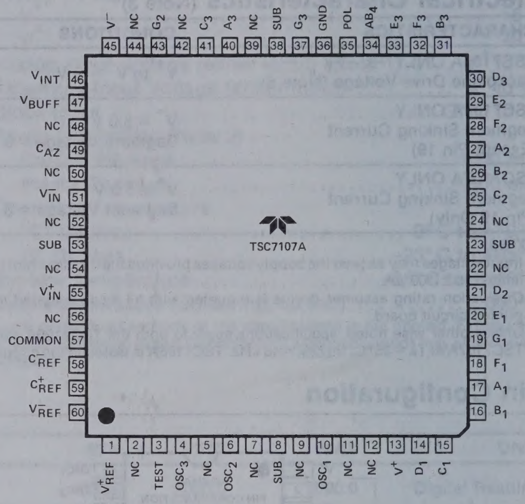

NORMAL
PIN CONFIGURATION
TSC7107A
V^+ 1
D_1 2
C_1 3
B_1 4
A_1 5
F_1 6
G_1 7
E_1 8
D_2 9
C_2 10
B_2 11
A_2 12
F_2 13
E_2 14
D_3 15
B_3 16
F_3 17
E_3 18
1000's ← AB_4 19
POL 20
(MINUS SIGN)
1's
10's
100's
40 OSC_1
39 OSC_2
38 OSC_3
37 TEST
36 V^+_{REF}
35 V^-_{REF}
34 C^+_{REF}
33 C^-_{REF}
32 ANALOG COMMON
31 V^+_{IN}
30 V^-_{IN}
29 C_{AZ}
28 V_{BUFF}
27 V_{INT}
26 V^-
25 G_2
24 C_3
23 A_3
22 G_3
21 GND
100's


REVERSE
PIN CONFIGURATION
TSC7107AR
OSC_1 1
OSC_2 2
OSC_3 3
TEST 4
V^+_{REF} 5
V^-_{REF} 6
C^+_{REF} 7
C^-_{REF} 8
ANALOG COMMON 9
V^+_{IN} 10
V^-_{IN} 11
C_{AZ} 12
V_{BUFF} 13
V_{INT} 14
V^- 15
G_2 16
C_3 17
A_3 18
G_3 19
GND 20
100's
40 V^+
39 D_1
38 C_1
37 B_1
36 A_1
35 F_1
34 G_1
33 E_1
32 D_2
31 C_2
30 B_2
29 A_2
28 F_2
27 E_2
26 D_3
25 B_3
24 F_3
23 E_3
22 AB_4 → 1000's
21 POL
(MINUS SIGN)
1's
10's
100's

Pin Configuration (Cont.)


V−
NC
G2
NC
C3
A3
NC
SUB
G3
BP
POL
AB4
E3
F3
B3
45 44 43 42 41 40 39 38 37 36 35 34 33 32 31
VINT 46
VBUFF 47
NC 48
CAZ 49
NC 50
V−IN 51
NC 52
SUB 53
NC 54
V+IN 55
NC 56
COMMON 57
C−REF 58
C+REF 59
V−REF 60
30 D3
29 E2
28 F2
27 A2
26 B2
25 C2
24 NC
23 SUB
22 NC
21 D2
20 E1
19 G1
18 F1
17 A1
16 B1
TSC7106A
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
V+REF
NC
TEST
OSC3
NC
OSC2
NC
SUB
NC
OSC1
NC
NC
V+
D1
C1

Notes:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.


V−
NC
G2
NC
C3
A3
NC
SUB
G3
GND
POL
AB4
E3
F3
B3
45 44 43 42 41 40 39 38 37 36 35 34 33 32 31
VINT 46
VBUFF 47
NC 48
CAZ 49
NC 50
V−IN 51
NC 52
SUB 53
NC 54
V+IN 55
NC 56
COMMON 57
C−REF 58
C+REF 59
V−REF 60
30 D3
29 E2
28 F2
27 A2
26 B2
25 C2
24 NC
23 SUB
22 NC
21 D2
20 E1
19 G1
18 F1
17 A1
16 B1
TSC7107A
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
V+REF
NC
TEST
OSC3
NC
OSC2
NC
SUB
NC
OSC1
NC
NC
V+
D1
C1

Notes:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7106ACPL	40-Pin Plastic Dip	Normal	0° C to +70° C	LCD
TSC7106ARCPL	40-Pin Plastic Dip	Reverse	0° C to +70° C	LCD
TSC7106AIJL	40-Pin CerDIP	Normal	-25° C to +85° C	LCD
TSC7106ACBQ	60-Pin Plastic Flat Package	Formed Leads	0° C to +70° C	LCD
TSC7106ACSQ	60-Pin Plastic Flat Package	Unformed Leads	0° C to +70° C	LCD
TSC7107ACPL	40-Pin Plastic Dip	Normal	0° C to +70° C	LED
TSC7107ARCPL	40-Pin CerDIP	Reverse	0° C to +70° C	LED
TSC7107AIJL	40-Pin CerDIP	Normal	-25° C to +85° C	LED
TSC7107ACBQ	60-Pin Plastic Flat Package	Formed Leads	0° C to +70° C	LED
TSC7107ACSQ	60-Pin Plastic Flat Package	Unformed Leads	0° C to +70° C	LED
Devices with Burn-In (160 Hours at +125° C)				
TSC7106ACPL/BI	40-Pin Plastic Dip	Normal	0° C to +70° C	LCD
TSC7107ACPL/BI	40-Pin Plastic Dip	Normal	0° C to +70° C	LED
TSC7107AIJL/BI	40-Pin CerDIP	Normal	-25° C to +85° C	LED

Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.
9	(32)	21	D_2	Activates the D section of the tens display.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP GND	TSC7106A: LCD Backplane drive output. TSC7107A: Digital Ground.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ for a 200 mV full-scale range and a 470 kΩ for 2 V full-scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 µF capacitor for a 200 mV full-scale, and a 0.047 µF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The analog low input is connected to this pin.
31	(10)	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.
34	(7)	59	C_{REF}^+	A 0.1 µF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1.0 µF is recommended and will hold the rollover error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.
36	(5)	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

General Theory of Operation

Dual Slope Conversion Principles

The TSC7106A and TSC7107A are dual slope, integrating analog-to-digital converters. An understanding of the dual slope conversion technique will aid in following the detailed operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}). (Figure 3A).

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

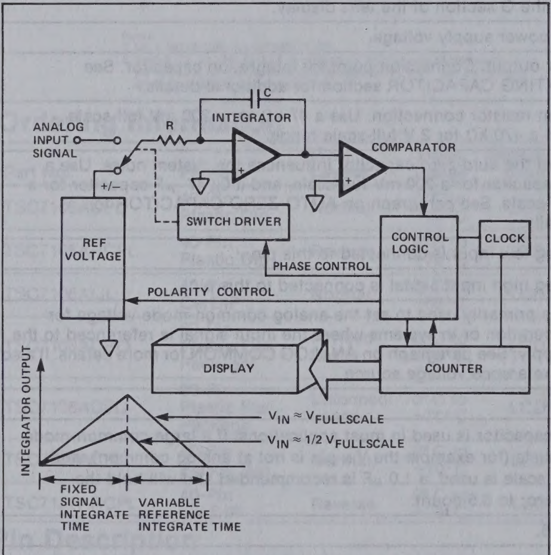

C
INTEGRATOR
ANALOG INPUT SIGNAL
R
COMPARATOR
+/–
SWITCH DRIVER
REF VOLTAGE
CONTROL LOGIC
CLOCK
PHASE CONTROL
POLARITY CONTROL
DISPLAY
COUNTER
INTEGRATOR OUTPUT
$V_{IN} \approx V_{FULLSCALE}$
$V_{IN} \approx 1/2\ V_{FULLSCALE}$
FIXED SIGNAL INTEGRATE TIME
VARIABLE REFERENCE INTEGRATE TIME

Figure 3A: Basic Dual Slope Converter

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_{0}^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage
T_{SI} = signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period. (Figure 3B)

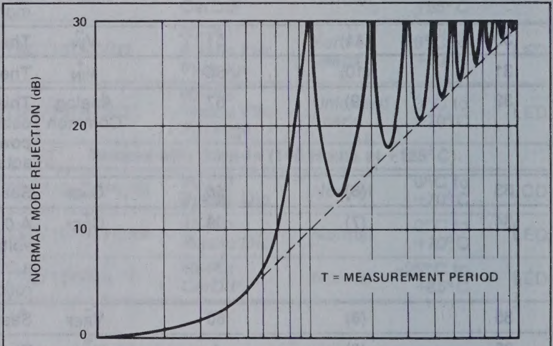


Figure 3B: Normal-Mode Rejection of Dual Slope Converter

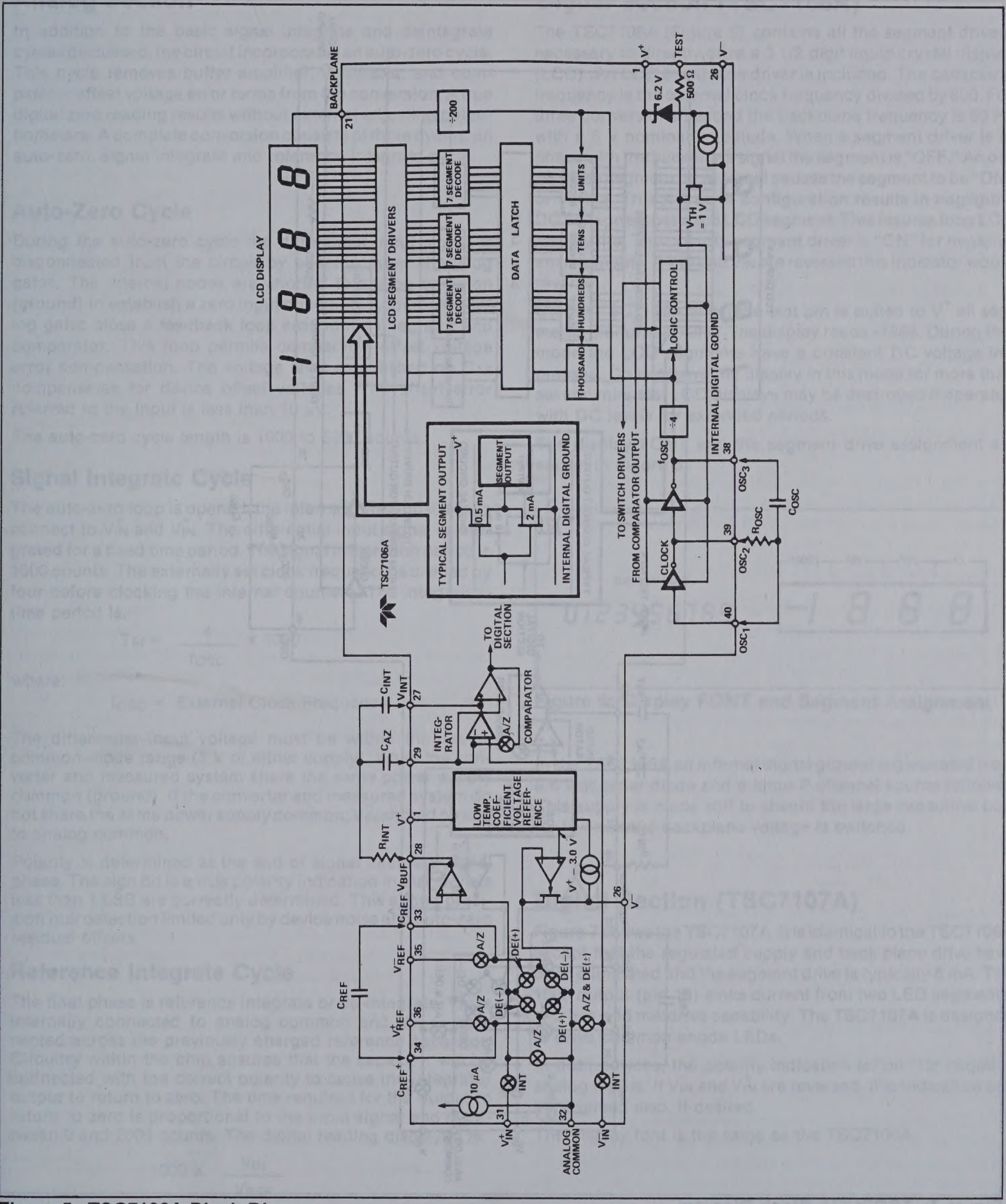

BACKPLANE
21
÷200
LCD DISPLAY
LCD SEGMENT DRIVERS
7 SEGMENT DECODE
7 SEGMENT DECODE
7 SEGMENT DECODE
DATA LATCH
UNITS
TENS
HUNDREDS
THOUSAND
LOGIC CONTROL
1
V+
TEST
6.2 V
500 Ω
26
V−
V_{TH} = 1 V
INTERNAL DIGITAL GOUND
38
÷4
f_{OSC}
OSC_3
C_{OSC}
39
R_{OSC}
OSC_2
40
OSC_1
CLOCK
TO SWITCH DRIVERS FROM COMPARATOR OUTPUT
TYPICAL SEGMENT OUTPUT
V+
0.5 mA
2 mA
SEGMENT OUTPUT
INTERNAL DIGITAL GROUND
TSC7106A
TO DIGITAL SECTION
COMPARATOR
A/Z
INTEG-RATOR
C_{INT}
V_{INT}
27
C_{AZ}
29
LOW TEMP. COEF-FICIENT VOLTAGE REFER-ENCE
V+
1
R_{INT}
28
V_{BUF}
$V^+ - 3.0$ V
26
V−
C_{REF}^-
33
V_{REF}^-
35
C_{REF}
V_{REF}^+
36
C_{REF}^+
34
A/Z
DE(+)
DE(−)
A/Z & DE(±)
10 μA
INT
V_{IN}^+
31
ANALOG COMMON
32
V_{IN}^-

Figure 5: TSC7106A Block Diagram

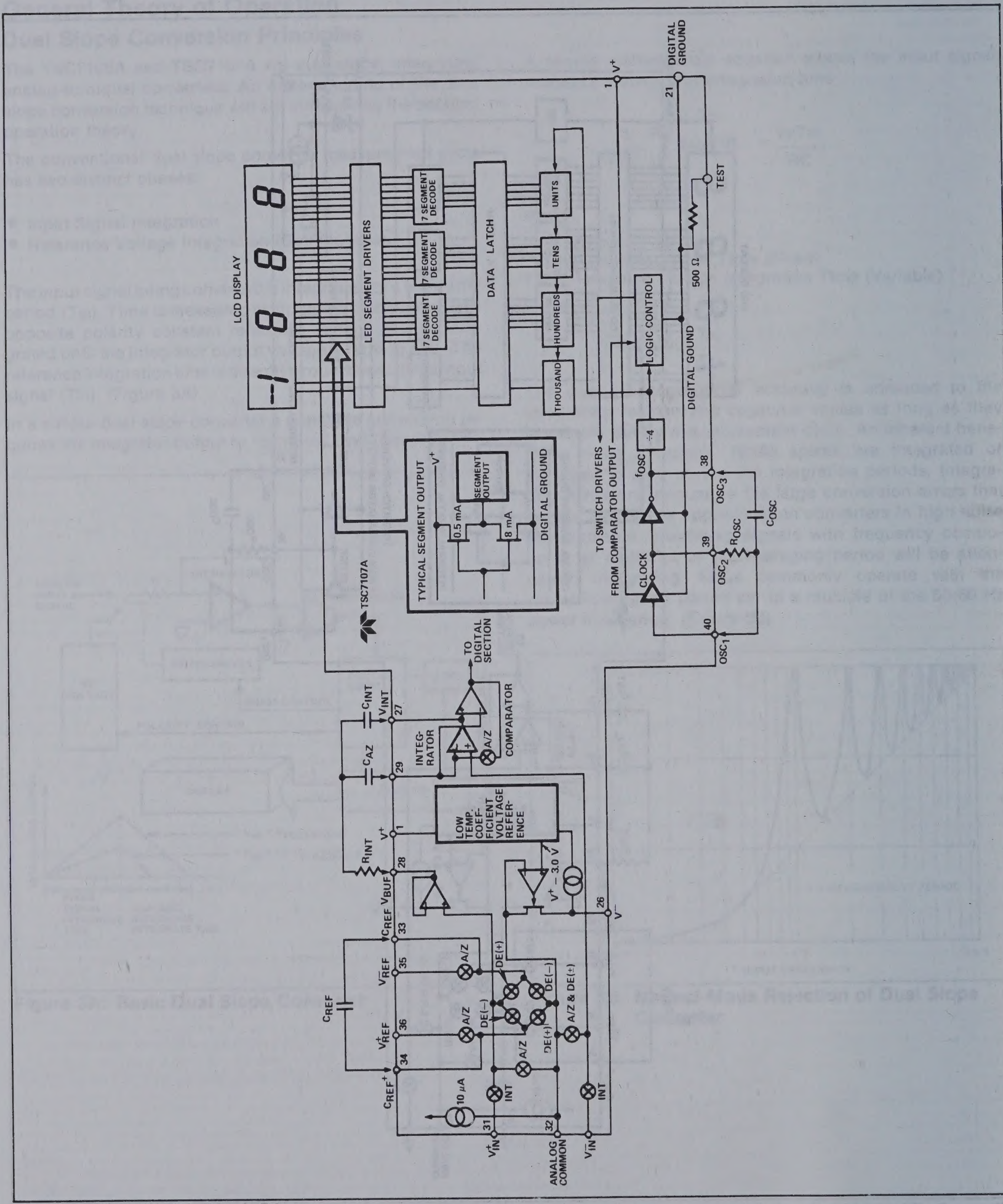

LCD DISPLAY
-1 8 8 8
LED SEGMENT DRIVERS
7 SEGMENT DECODE
7 SEGMENT DECODE
7 SEGMENT DECODE
DATA LATCH
UNITS
TENS
HUNDREDS
THOUSAND
1
V+
21
DIGITAL GROUND
TEST
500 Ω
LOGIC CONTROL
DIGITAL GOUND
÷4
TO SWITCH DRIVERS
FROM COMPARATOR OUTPUT
fOSC
38
OSC3
COSC
CLOCK
39
OSC2
ROSC
40
OSC1
TYPICAL SEGMENT OUTPUT
V+
0.5 mA
SEGMENT OUTPUT
8 mA
DIGITAL GROUND
TSC7107A
TO DIGITAL SECTION
COMPARATOR
CINT
VINT
27
INTEG-RATOR
A/Z
CAZ
29
LOW TEMP. COEF-FICIENT VOLTAGE REFER-ENCE
V+
1
RINT
28
VBUF
V+ – 3.0 V
26
V−
CREF
33
V−REF
35
CREF
V+REF
36
CREF+
34
A/Z
DE(+)
DE(−)
DE(−)
A/Z
A/Z
DE(+)
A/Z & DE(±)
10 μA
INT
INT
31
V+IN
32
ANALOG COMMON
V−IN

Figure 7: TSC7107A Block Diagram

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed, the circuit incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference integrate cycle.

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The offset error referred to the input is less than 10 μV.

The auto-zero cycle length is 1000 to 3000 counts.

Signal Integrate Cycle

The auto-zero loop is opened, the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is integrated for a fixed time period. The signal integration period is 1000 counts. The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{4}{f_{OSC}} \times 1000$$

where:

f_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range (1 V of either supply) when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference Integrate Cycle

The final phase is reference integrate or de-integrate. V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 counts. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Digital Section (TSC7106A)

The TSC7106A (Figure 5) contains all the segment drivers necessary to directly drive a 3 1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60 Hz with a 5 V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF." An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^+ and V_{IN}^- are reversed this indicator would reverse.

On the TSC7106A when the test pin is pulled to V^+ all segments are turned "ON." The display reads -1888. During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and the segment drive assignment are shown in Figure 6.

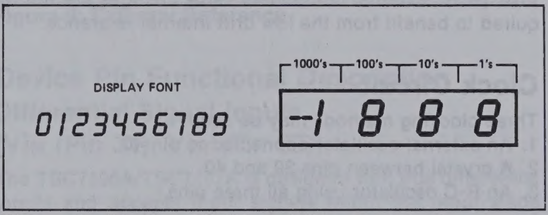


Figure 6: Display FONT and Segment Assignment

In the TSC7106A an internal digital ground is generated from a 6 volt zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the backplane voltage is switched.

Digital Section (TSC7107A)

Figure 7 shows the TSC7107A. It is identical to the TSC7106A except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TSC7107A is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

The display font is the same as the TSC7106A.

System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The three phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 1000 to 3000 Counts
  (4000 to 12000 Clock Pulses)
  For signals less than full-scale the auto-zero phase is assigned the unused reference integrate time period.
- Signal Integrate: 1000 Counts
  (4000 Clock Pulses)
  This time period is fixed. The integration period is:

$$T_{SI} = 4000 \left[\frac{1}{f_{OSC}} \right]$$

Where f_{OSC} is the externally set clock frequency.

- Reference Integrate: 0 to 2000 Counts
  (0 to 8000 Clock Pulses)

The TSC7106A/7107A are drop replacements for the 7106/7107 parts. External component value changes are not required to benefit from the low drift internal reference.

Clock Circuit

Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

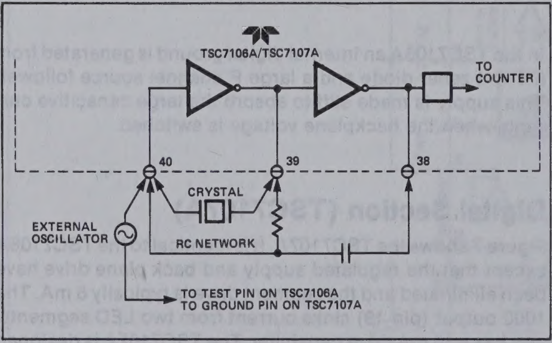


Figure 8: Clock Circuits

Component Value Selection

Auto-Zero Capacitor - C_{AZ}

The C_{AZ} capacitor size has some influence on system noise. A 0.47 µF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 µV. A 0.047 µF capacitor is adequate for 2.0 V full-scale applications. A mylar type dielectric capacitor is adequate.

Reference Voltage Capacitor - C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 µF capacitor is acceptable when $V_{\overline{IN}}$ is tied to analog common. If a large common-mode voltage exists ($V_{\overline{REF}} \neq$ analog common) and the application requires a 200 mV full-scale increase C_{REF} to 1.0 µF. Rollover error will be held to less than 0.5 count. A mylar type dielectric capacitor is adequate.

Integrating Capacitor - C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Due to the TSC7106A/7107A superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case a ±2 V full-scale integrator output swing is satisfactory. For 3 readings/second (f_{OSC} = 48 kHz) a 0.22 µF value is suggested. If a different oscillator frequency is used C_{INT} must be changed in inverse proportion to maintain the nominal ±2 V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}}$$

Where:

f_{OSC} = Clock frequency at Pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{ING} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize rollover error. An inexpensive polypropylene capacitor is recommended.

Integrating Resistor - R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 100 µA. The integrator and buffer can supply 20 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200 mV full-scale R_{INT} is 47 kΩ. A 2.0 V full-scale requires 470 kΩ.

Component	Nominal Full-Scale Voltage	
Value	200.0 mV	2.000 V
C_{AZ}	0.47 µF	0.047 µF
R_{INT}	47 kΩ	470 kΩ
C_{INT}	0.22 µF	0.22 µF

Note:
1. f_{OSC} = 48 kHz (3 readings/sec)

Oscillator Components

R_{OSC} (Pin 40 to Pin 39) should be 100 kΩ. C_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}$$

For f_{OSC} of 48 kHz, C_{OSC} is 100 pF nominally.

Note that f_{OSC} is divided by four to generate the TSC7106A internal control clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, 33 1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66 2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	V_{REF}
200.0 mV	100.0 mV
2.000 V	1.000 V

* $V_{FS} = 2\,V_{REF}$

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400 mV for 2000 lb/in². Rather than dividing the input voltage by two the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

The internal voltage reference potential available at analog common will normally be used to supply the converters reference. This potential is stable whenever the supply potential is greater than approximately 7 V. In applications where an externally generated reference voltage is desired refer to Figure 9.

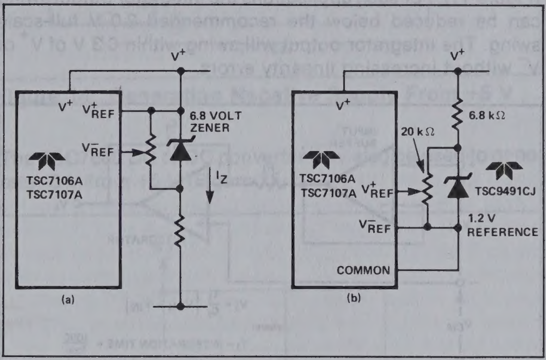


Figure 9: External Reference

Device Pin Functional Description

Differential Signal Inputs

(V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30))

The TSC7106A/TSC7107A is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The typical range is V^+ −1.0 to V^- +1 V. Common-mode voltages are removed from the system when the TSC7106A/TSC7107A operates from a battery or floating power source (isolated from measured system) and V_{IN}^- is connected to analog common (V_{COM}): See Figure 10.

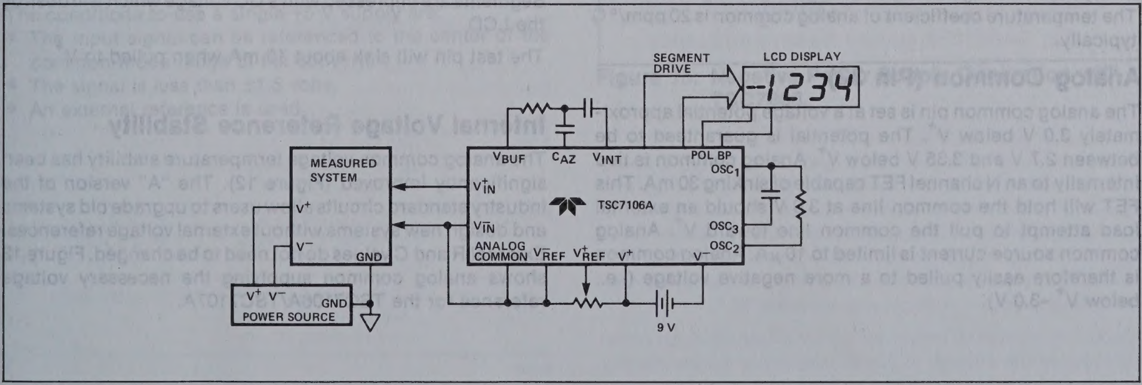


Figure 10: Common-Mode Voltage Removed in Battery Operation with V_{IN}^- = Analog Common

Differential Signal Inputs (Cont.)

In systems where common-mode voltages exist the 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 11). For such applications the integrator output swing can be reduced below the recommended 2.0 V full-scale swing. The integrator output will swing within 0.3 V of V^+ or V^- without increasing linearity errors.

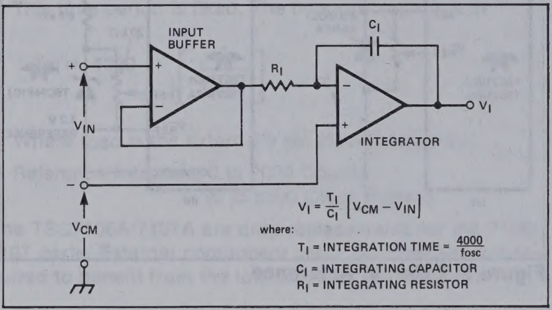

INPUT BUFFER
C_I
R_I
+
−
V_I
INTEGRATOR
V_{IN}
V_{CM}
$V_I = \frac{T_I}{C_I}\left[V_{CM} - V_{IN}\right]$
where:
T_I = INTEGRATION TIME = $\frac{4000}{f_{OSC}}$
C_I = INTEGRATING CAPACITOR
R_I = INTEGRATING RESISTOR

Figure 11: Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

Differential Reference
(V_{REF}^{+} (Pin 36), V_{REF}^{-} (Pin 39))

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent rollover type errors being induced by large common-mode voltages C_{REF} should be large compared to stray node capacitance.

The TSC7106A/TSC7107A circuits have a significantly lower analog common temperature coefficient. This potential gives a very stable voltage suitable for use as a voltage reference. The temperature coefficient of analog common is 20 ppm/° C typically.

Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3.0 V below V^+. The potential is guaranteed to be between 2.7 V and 3.35 V below V^+. Analog common is tied internally to an N channel FET capable of sinking 30 mA. This FET will hold the common line at 3.0 V should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 10 μA. Analog common is therefore easily pulled to a more negative voltage (i.e., below V^+ −3.0 V).

The TSC7106A connects the internal V_{IN}^{+} and V_{IN}^{-} inputs to analog common during the auto-zero cycle. During the reference integrate phase V_{IN}^{-} is connected to analog common. If V_{IN}^{-} is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converters 86 dB common-mode rejection ratio. In battery operation analog common and V_{IN}^{-} are usually connected removing common-mode voltage concerns. In systems where V_{IN}^{-} is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}^{-}.

The analog common pin serves to set the analog section reference or common point. The TSC7106A is specificially designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TSC7106A power source. The analog common potential of V^+ −3.0 V gives a 6 V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient and 15 Ω output impedance.

With sufficiently high total supply voltage ($V^+ - V^- > 7.0$ V) analog common is a very stable potential with excellent temperature stability — typically 20 ppm/° C. This potential can be used to generate the reference voltage. An external voltage reference will be unnecessary in most cases because of the 50 ppm/° C maximum temperature coefficient. See Internal Voltage Reference discussion.

Test (Pin 37)

The test pin potential is 5 V less than V^+. Test may be used as the negative power supply connection for external CMOS logic. The test pin is tied to the internally generated negative logic supply (Internal Logic Ground) through a 500 Ω resistor in the TSC7106A. The test pin load should be no more than 1 mA.

If test is pulled high to V^+ all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes with the TSC7106A. With Test = V^+ the LCD Segments are impressed with a DC voltage which will destroy the LCD.

The test pin will sink about 10 mA when pulled to V^+.

Internal Voltage Reference Stability

The analog common voltage termperature stability has been significantly improved (Figure 12). The "A" version of the industry standard circuits allow users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 13 shows analog common supplying the necessary voltage reference for the TSC7106A/TSC7107A.

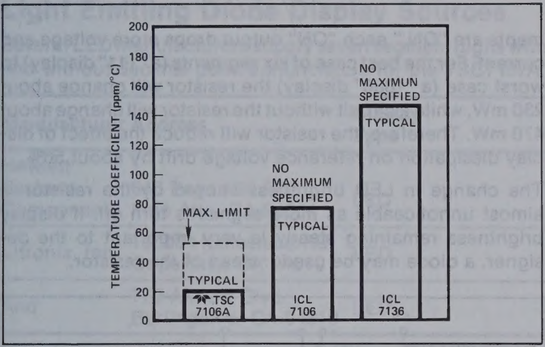


Figure 12: Analog Common Temperature Coefficient

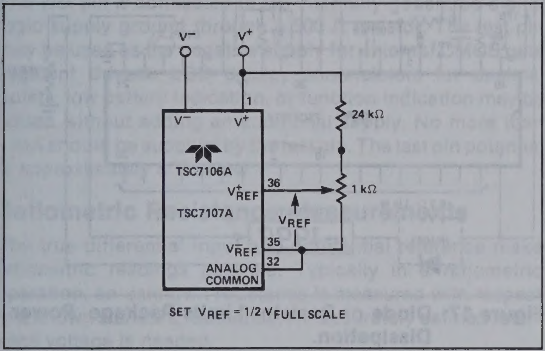

V⁻
V⁺
1
V⁻
V⁺
24 kΩ
TSC7106A
V^+_{REF}
36
1 kΩ
TSC7107A
V_{REF}
V^-_{REF}
35
32
ANALOG COMMON
SET V_{REF} = 1/2 $V_{FULL\ SCALE}$

Figure 13: Internal Voltage Reference Connection

TSC7107A Power Supplies

The TSC7107A is designed to work from ±5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors and an inexpensive IC. Figure 13 shows this application.

In selected applications a negative supply is not required. The conditions to use a single +5 V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5 volts.
- An external reference is used.

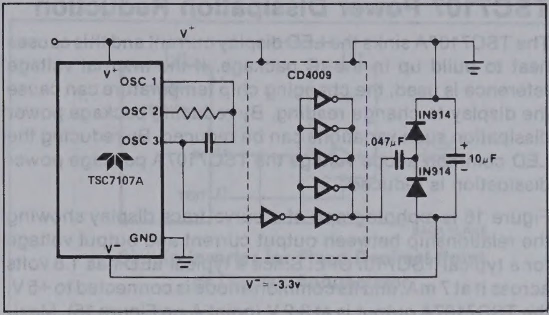

V⁺
V⁺
OSC 1
OSC 2
OSC 3
TSC7107A
GND
V⁻
CD4009
IN914
.047μF
10μF
IN914
V⁻ = -3.3v

Figure 14: Generating Negative Supply From +5 V

The TSC7660 DC to DC converter may also be used to generate -5 V from +5 V (Figure 15).

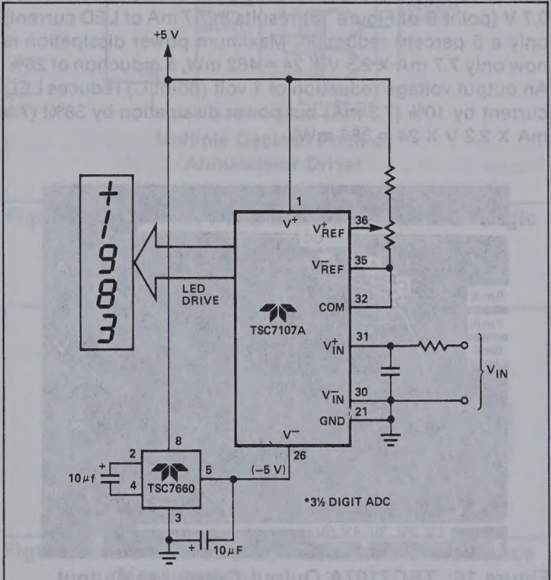

+5 V
1
V⁺
V^+_{REF}
36
V^-_{REF}
35
LED DRIVE
COM
32
TSC7107A
V^+_{IN}
31
V_{IN}
V^-_{IN}
30
GND
21
V⁻
26
2
8
10μf
4
TSC7660
5
(−5 V)
3
10μF
*3½ DIGIT ADC

Figure 15: Negative Power Supply Generation with TSC7660.

TSC7107 Power Dissipation Reduction

The TSC7107A sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TSC7107A package power dissipation is reduced.

Figure 16 is a photograph of a curve-trace display showing the relationship between output current and output voltage for a typical TSC7107CPL. Since a typical LED has 1.8 volts across it at 7 mA, and its common anode is connected to +5 V, the TSC7107A output is at 3.2 V (point A on Figure 15). Maximum power dissipation is 8.1 mA X 3.2 V X 24 segments = 622 mW.

Notice, however, that once the TSC7107A output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B of Figure 15) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is now only 7.7 mA X 2.5 V X 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA X 2.2 V X 24 = 385 mW).

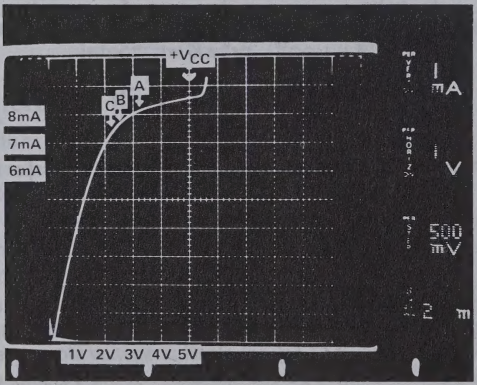


Figure 16: TSC7107A Output Current vs Output Voltage

Reduced power dissipation is very easy to obtain. Fig. 17 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TSC7107A). The resistor will reduce the TSC7107A output voltage, when all 24 segments are "ON," to point "C" of Fig. 16. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, a diode may be used instead of the resistor.

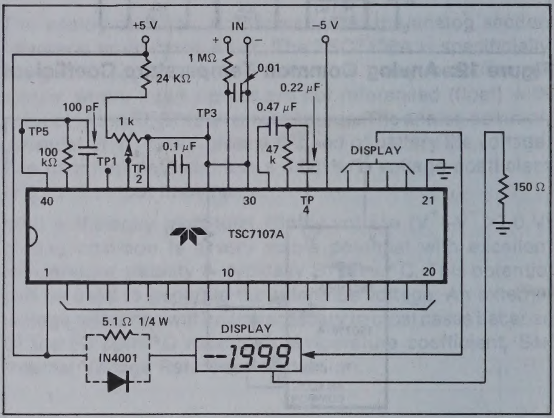


Figure 17: Diode or Resistor Limits Package Power Dissipation.

Applications Information

Liquid Crystal Display Sources

Several LCD manufacturers supply standard LCD displays to interface with the TSC7106A 3 1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers[1]
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216/655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415/347-9916	FE 0801 FE 0203
EPSON	3415 Kashikawa St., Torrance, CA 90505 213/534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414/648-2361	3902, 3933, 3903

Note:

1. Contact LCD manufacturer for full product listing/specifications.

Light Emitting Diode Display Sources

Several LED manufacturers supply seven segment digits with and without decimal point annunciators for the TSC7107A.

Manufacturer	Address	Display Type
Hewlett Packard Components	640 Page Mill Rd. Palo Alto, CA 94304	LED
Litronix, Inc.	19000 Homestead Rd. Cupertino, CA 94010	LED
And	770 Airport Blvd. Burlingame, CA 94010	LED

Decimal Point and Annunciator Drive

The test pin is connected to the internally-generated digital logic supply ground through a 500 Ω resistor. The test pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the test pin. The test pin potential is approximately 5 V below V^+.

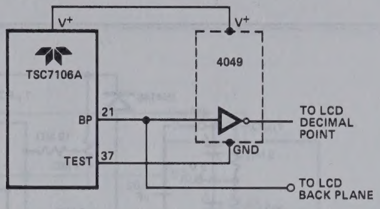
Ratiometric Resistance Measurements

The true differential input and differential reference make ratiometric readings possible. Typically in a ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

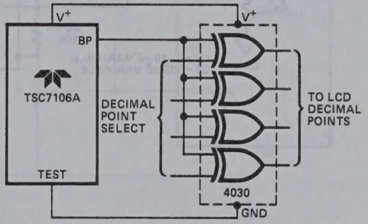
The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{\text{R Unknown}}{\text{R Standard}} \times 1000$$

The display will overrange for R Unknown ≥ 2 x R Standard.



Simple Inverter for Fixed Decimal Point or Display Annunciator



Multiple Decimal Point or Annunciator Driver

Figure 18: Decimal Point Drive Using Test as Logic Ground.

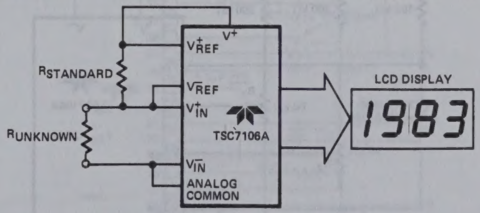


Figure 19: Low Parts Count Ratiometric Resistance Measurement

Application Circuits

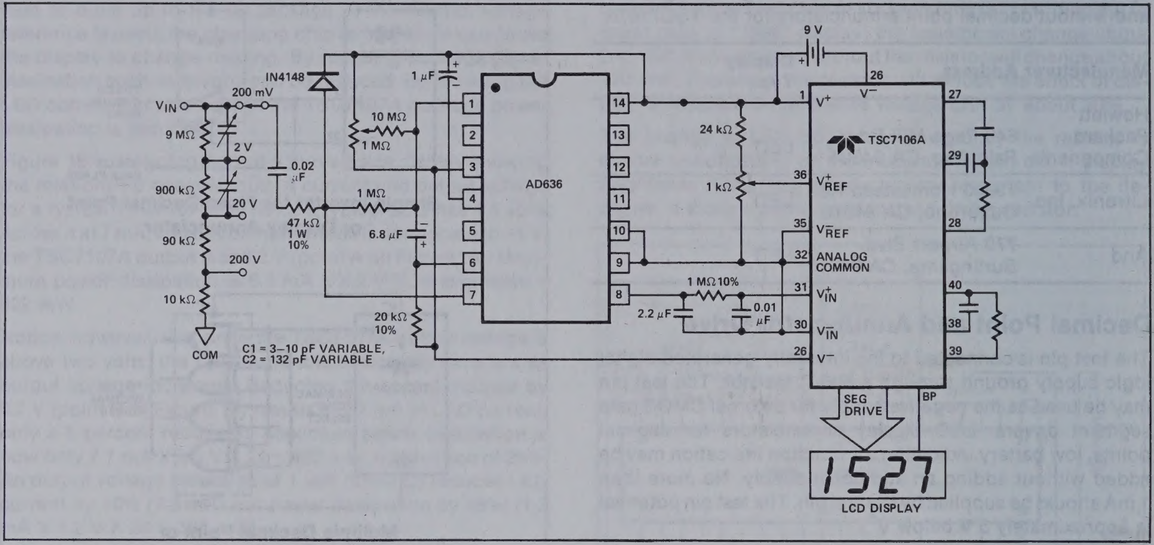

9 V
IN4148
1 µF
200 mV
V_IN
9 MΩ
2 V
0.02 µF
10 MΩ
1 MΩ
900 kΩ
20 V
1 MΩ
47 kΩ 1 W 10%
6.8 µF
90 kΩ
200 V
10 kΩ
COM
20 kΩ 10%
C1 = 3–10 pF VARIABLE,
C2 = 132 pF VARIABLE
AD636
1
2
3
4
5
6
7
14
13
12
11
10
9
8
24 kΩ
1 kΩ
1 MΩ 10%
2.2 µF
0.01 µF
TSC7106A
1
26
27
29
28
36
35
32
31
30
26
40
38
39
V+
V−
V+REF
V−REF
ANALOG COMMON
V+IN
V−IN
SEG DRIVE
BP
1527
LCD DISPLAY

Figure 20: 3 1/2 Digit True RMS AC DMM

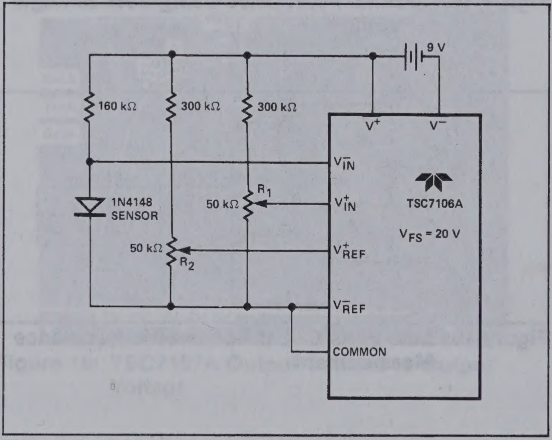

9 V
160 kΩ
300 kΩ
300 kΩ
V+
V−
V−IN
V+IN
V+REF
V−REF
COMMON
TSC7106A
V_FS = 20 V
1N4148 SENSOR
50 kΩ
R1
50 kΩ
R2

Figure 21: Temperature Sensor

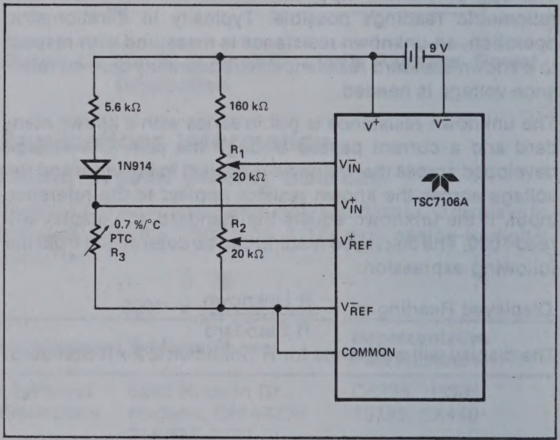

9 V
5.6 kΩ
160 kΩ
1N914
R1
20 kΩ
0.7 %/°C PTC R3
R2
20 kΩ
V+
V−
V−IN
V+IN
V+REF
V−REF
COMMON
TSC7106A

Figure 22: Positive Temperature Coefficient Resistor Temperature Sensor

Application Circuits (Cont.)

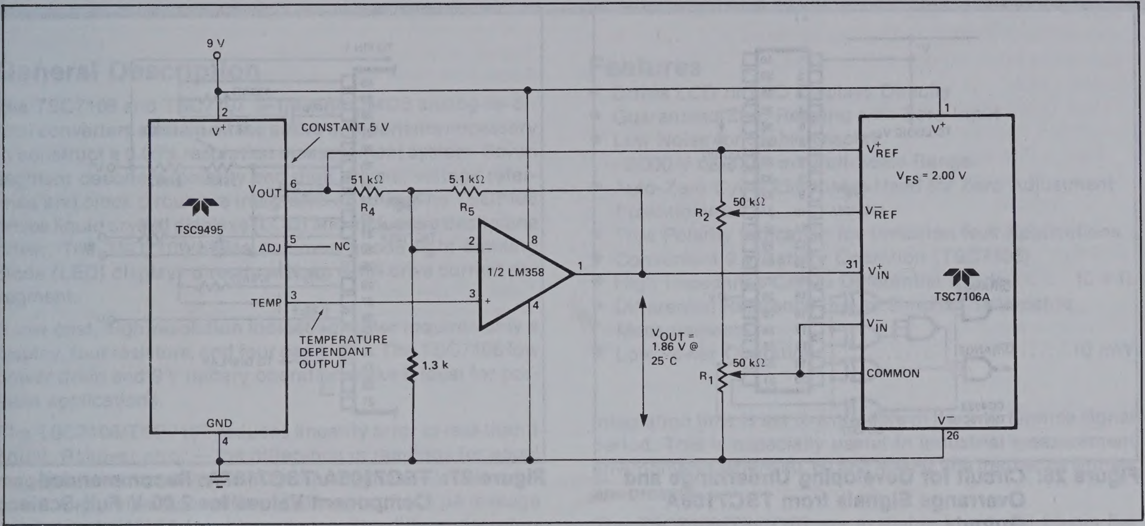

9 V
2
V+
CONSTANT 5 V
TSC9495
VOUT
6
ADJ
5
NC
TEMP
3
TEMPERATURE DEPENDANT OUTPUT
GND
4
51 kΩ
R4
5.1 kΩ
R5
2
3
8
4
1/2 LM358
1
1.3 k
VOUT = 1.86 V @ 25 C
1
V+
V+REF
VFS = 2.00 V
50 kΩ
R2
V−REF
31
V+IN
TSC7106A
V−IN
50 kΩ
R1
COMMON
V−
26

Figure 23: Integrated Circuit Temperature Sensor

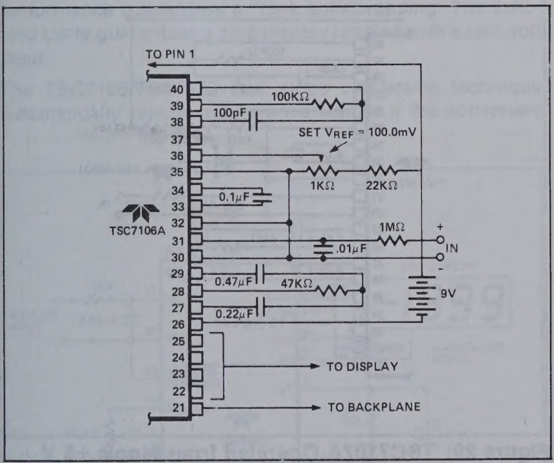

TO PIN 1
40
39
38
37
36
35
34
33
32
31
30
29
28
27
26
25
24
23
22
21
100KΩ
100pF
SET VREF = 100.0mV
1KΩ
22KΩ
0.1μF
TSC7106A
1MΩ
+
IN
-
.01μF
0.47μF
47KΩ
9V
0.22μF
TO DISPLAY
TO BACKPLANE

Figure 24: TSC7106A Using the Internal Reference. (200 mV Full-Scale, 3 RPS).

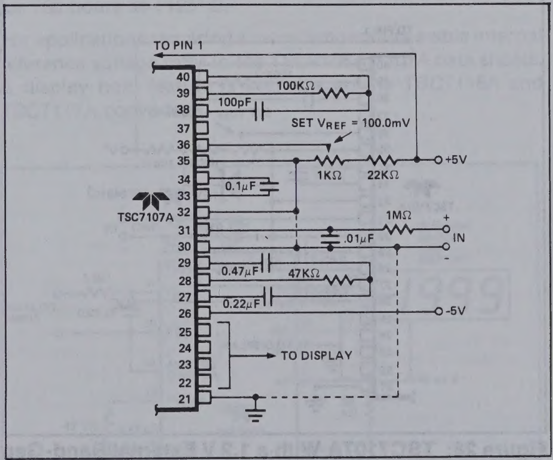

TO PIN 1
40
39
38
37
36
35
34
33
32
31
30
29
28
27
26
25
24
23
22
21
100KΩ
100pF
SET VREF = 100.0mV
1KΩ
22KΩ
+5V
0.1μF
TSC7107A
1MΩ
+
IN
-
.01μF
0.47μF
47KΩ
0.22μF
-5V
TO DISPLAY

Figure 25: TSC7107A Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN}^- Tied to GND for Single Ended Inputs).

Application Circuits (Cont.)

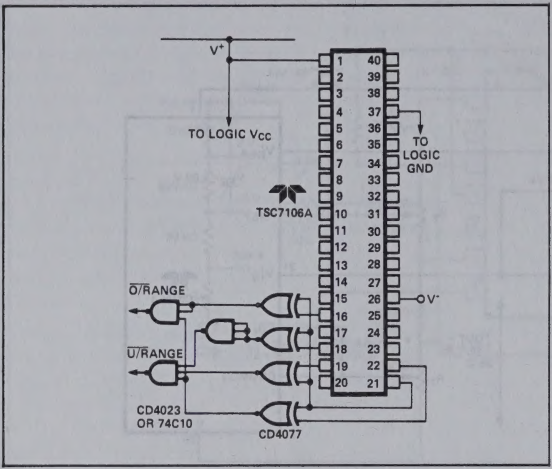

V+
TO LOGIC V_{CC}
TO LOGIC GND
TSC7106A
V-
O/RANGE
U/RANGE
CD4023 OR 74C10
CD4077

Figure 26: Circuit for Developing Underrange and Overrange Signals from TSC7106A Outputs.

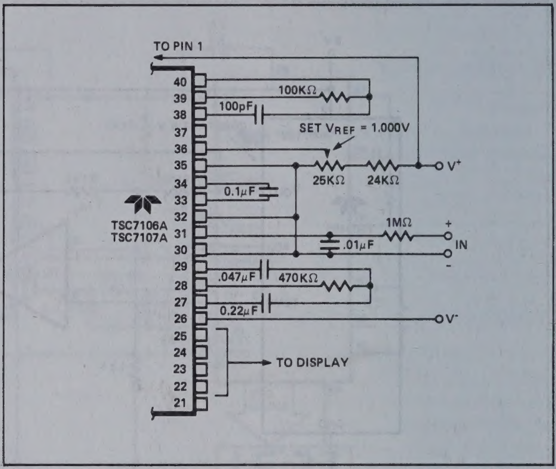

TO PIN 1
100KΩ
100pF
SET V_{REF} = 1.000V
25KΩ
24KΩ
V+
0.1μF
TSC7106A
TSC7107A
1MΩ
.01μF
IN
.047μF
470KΩ
0.22μF
V-
TO DISPLAY

Figure 27: TSC7106A/TSC7107A: Recommended Component Values for 2.00 V Full-Scale.

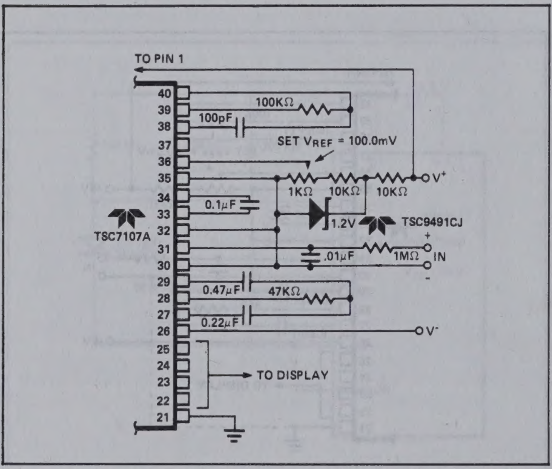

TO PIN 1
100KΩ
100pF
SET V_{REF} = 100.0mV
1KΩ
10KΩ
10KΩ
V+
0.1μF
1.2V
TSC9491CJ
TSC7107A
.01μF
1MΩ
IN
0.47μF
47KΩ
0.22μF
V-
TO DISPLAY

Figure 28: TSC7107A With a 1.2 V External Band-Gap Reference. V_{IN}^- Tied to Common).

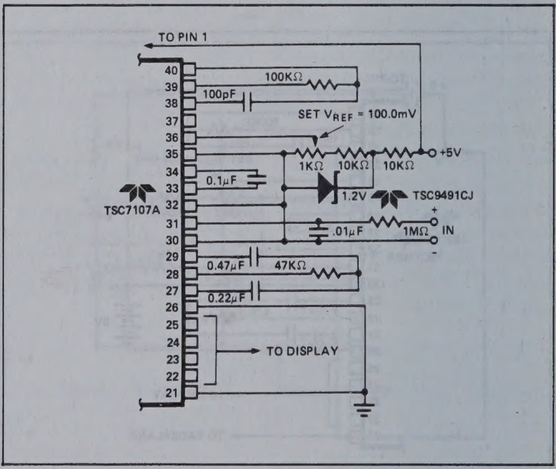

TO PIN 1
100KΩ
100pF
SET V_{REF} = 100.0mV
1KΩ
10KΩ
10KΩ
+5V
0.1μF
1.2V
TSC9491CJ
TSC7107A
.01μF
1MΩ
IN
0.47μF
47KΩ
0.22μF
TO DISPLAY

Figure 29: TSC7107A Operated from Single +5 V Supply. An External Reference Must Be Used in This Application.

TSC7106 (LCD Drive)
TSC7107 (LED Drive)
3 1/2 Digit A/D Converter

- **Direct Display Drive**
- **Automatic Zero Correction**

General Description

The TSC7106 and TSC7107 3-1/2 digit CMOS analog-to-digital converters contain all the active components necessary to construct a 0.05% resolution measurement system. Seven segment decoders, polarity and digit drivers, voltage reference and clock circuit are integrated on chip. The TSC7106 drives liquid crystal displays (LCD) and includes a backplane driver. The TSC7107 drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment.

A low cost, high resolution indicating meter requires only a display, four resistors, and four capicitors. The TSC7106 low power drain and 9 V battery operation make it ideal for portable applications.

The TSC7106/TSC7107 reduces linearity error to less than 1 count. Rollover error — the difference in readings for equal magnitude but opposite polarity input signals — is below ± 1 count. High impedance differential inputs offer 1 pA leakage current and a $10^{12}\ \Omega$ input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μVp-p noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

The TSC7106/TSC7107 dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The TSC7106/TSC7107 are available in a small 60-pin flat package for compact designs. Standard devices are offered in an industrial temperature range and with burn-in lasting for 160 hours at +125° C.

For applications requiring a more temperature stable internal reference voltage refer to the TSC7106A/7107A data sheets. A display hold feature is available on the TSC7116A and TSC7117A converters.

Features

- Drives LCD or LED Displays Directly
- Guaranteed Zero Reading with Zero Input
- Low Noise for Stable Display
  -2.000 V or 200.0 mV Full-Scale Range
- Auto-Zero Cycle Eliminates Need for Zero Adjustment Potentiometer
- True Polarity Indication for Precision Null Applications
- Convenient 9 V Battery Operation (TSC7106)
- High Impedance CMOS Differential Inputs ..... $10^{12}\ \Omega$
- Differential Reference Inputs Simplify Ratiometric Measurements
- Low Power Operation .... 10 mW

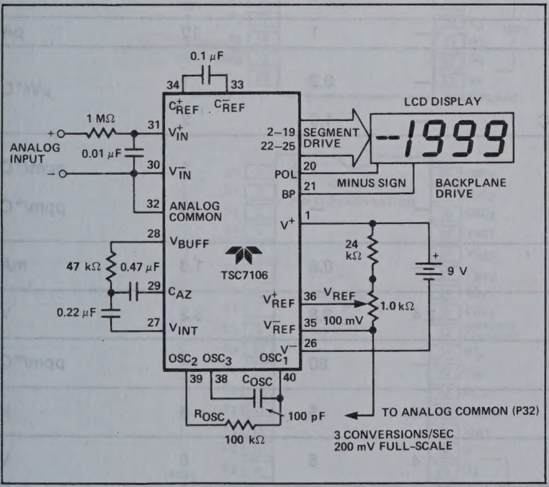

0.1 µF
34
33
C+REF
C−REF
LCD DISPLAY
1 MΩ
31
+
ANALOG INPUT
−
0.01 µF
V+IN
30
V−IN
2–19
22–25
SEGMENT DRIVE
-1999
20
POL
21
BP
MINUS SIGN
BACKPLANE DRIVE
32
ANALOG COMMON
V+
1
28
VBUFF
24 kΩ
9 V
47 kΩ
0.47 µF
TSC7106
29
CAZ
V+REF
36
VREF
1.0 kΩ
0.22 µF
27
VINT
V−REF
35
100 mV
V−
26
OSC2
OSC3
OSC1
39
38
COSC
40
ROSC
100 pF
100 kΩ
TO ANALOG COMMON (P32)
3 CONVERSIONS/SEC
200 mV FULL-SCALE

Figure 1: Typical TSC7106 Operating Circuit

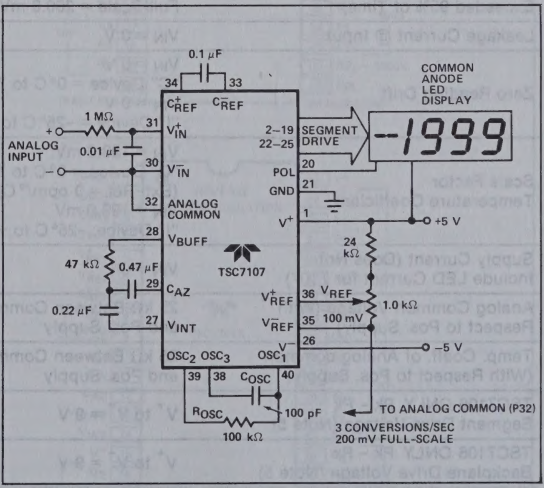

0.1 µF
34
33
C+REF
C−REF
COMMON ANODE LED DISPLAY
1 MΩ
31
+
ANALOG INPUT
−
0.01 µF
V+IN
30
V−IN
2–19
22–25
SEGMENT DRIVE
-1999
20
POL
21
GND
32
ANALOG COMMON
V+
1
+5 V
28
VBUFF
24 kΩ
47 kΩ
0.47 µF
TSC7107
29
CAZ
V+REF
36
VREF
1.0 kΩ
0.22 µF
27
VINT
V−REF
35
100 mV
V−
26
−5 V
OSC2
OSC3
OSC1
39
38
COSC
40
ROSC
100 pF
100 kΩ
TO ANALOG COMMON (P32)
3 CONVERSIONS/SEC
200 mV FULL-SCALE

Figure 2: Typical TSC7107 Operating Circuit

© 1983

Absolute Maximum Ratings

TSC7106

Supply Voltage (V^+ to V^-)	15 V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	Test to V^+
Power Dissipation (Note 2)	
CerDIP Package	1000 mW
Plastic Package	800 mW
Operating Temperature	
"C" Devices	0° C to +70° C
"I" Devices	-25° C to +85° C
Storage Temperature	-65° C to +160° C
Lead Temperature (Soldering, 60 sec)	300° C

TSC7107

Supply Voltage	
V^+	+6 V
V^-	-9 V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	GND to V^+
Power Dissipation (Note 1)	
CerDIP Package	1000 mW
Plastic Package	800 mW
Operating Temperature	
"C" Devices	0° C to +70° C
"I" Devices	-25° C to +85° C
Storage Temperature	-65° C to +160° C
Lead Temperature (Soldering, 60 sec)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

Electrical Characteristics (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF} V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \simeq 200.0$ mV	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1 V, V_{IN} = 0 V. Full-Scale = 200.0 mV	—	50	—	µV/V
Noise (Pk - Pk Value Not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 200.0 mV	—	15	—	µV
Leakage Current @ Input	V_{IN} = 0 V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 V "C" Device = 0° C to 70° C	—	0.2	1	µV/° C
	V_{IN} = 0 V "I" Device = -25° C to +85° C	—	1.0	2	
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, "C" Device = 0° C to 70° C (Ext. Ref = 0 ppm/° C)		1	5	ppm/° C
	V_{IN} = 199.0 mV "I" Device: -25° C to +85° C	—	—	20	ppm/° C
Supply Current (Does Not Include LED Current for 7107)	V_{IN} = 0	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog common (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	—	80	—	ppm/° C
TSC7106 ONLY Pk - Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7106 ONLY Pk - Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V

3 1/2 Digit A/D Converter
- **Direct Display Drive**
- **Automatic Zero Correction**

TSC7106 (LCD Drive)
TSC7107 (LED Drive)

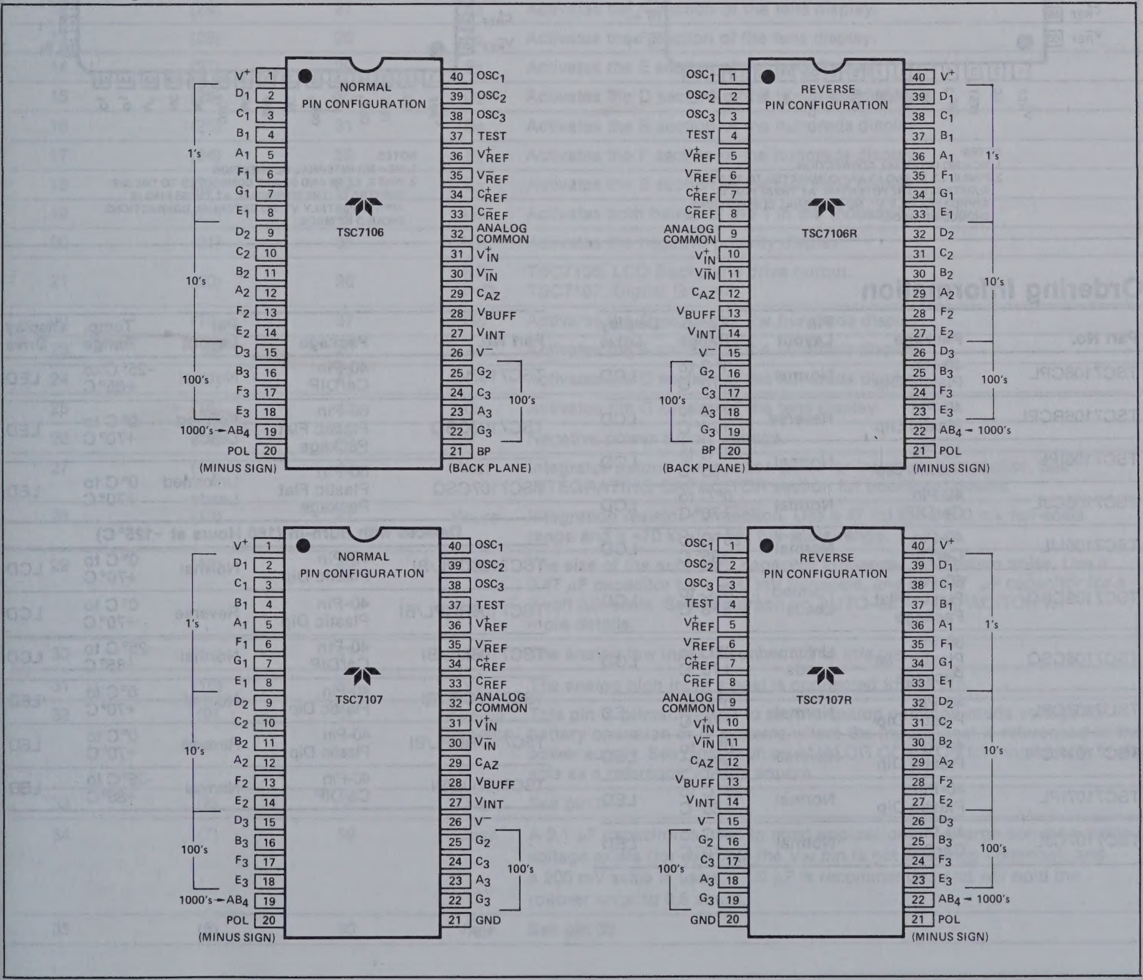
Electrical Characteristics (Note 3) (Continued)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
TSC7107 ONLY Segment Sinking Current (Except Pin 19)	$V^+ = 5.0$ V Segment Voltage = 3 V	5	8.0	—	mA
TSC7107 ONLY Segment Sinking Current (Pin 19 Only)	$V^+ = 5.0$ V Segment Voltage = 3 V	10	16	—	mA

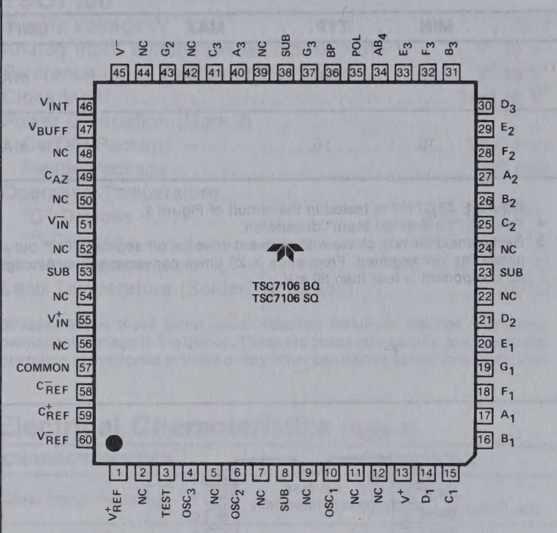
NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to ± 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless other wise noted, specifications apply to both the TSC7106 and TSC7107 at $T_A = 25°C$, $f_{CLOCK} = 48$ kHz. TSC7106 is tested in the circuit of Figure 1. TSC7107 is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average dc component is less than 50 mV.

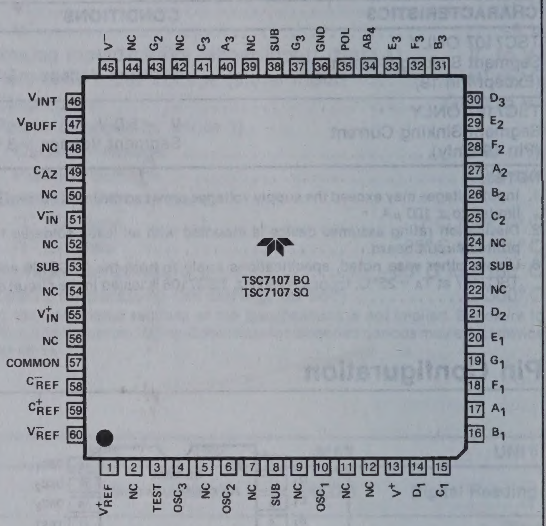
Pin Configuration


NORMAL PIN CONFIGURATION
TSC7106
1 V+
2 D1
3 C1
4 B1
5 A1
6 F1
7 G1
8 E1
9 D2
10 C2
11 B2
12 A2
13 F2
14 E2
15 D3
16 B3
17 F3
18 E3
19 AB4
20 POL
(MINUS SIGN)
1's
10's
100's
1000's
40 OSC1
39 OSC2
38 OSC3
37 TEST
36 V+REF
35 V−REF
34 C+REF
33 C−REF
32 ANALOG COMMON
31 V+IN
30 V−IN
29 CAZ
28 VBUFF
27 VINT
26 V−
25 G2
24 C3
23 A3
22 G3
21 BP
(BACK PLANE)
100's
REVERSE PIN CONFIGURATION
TSC7106R
1 OSC1
2 OSC2
3 OSC3
4 TEST
5 V+REF
6 V−REF
7 C+REF
8 C−REF
9 ANALOG COMMON
10 V+IN
11 V−IN
12 CAZ
13 VBUFF
14 VINT
15 V−
16 G2
17 C3
18 A3
19 G3
20 BP
(BACK PLANE)
100's
40 V+
39 D1
38 C1
37 B1
36 A1
35 F1
34 G1
33 E1
32 D2
31 C2
30 B2
29 A2
28 F2
27 E2
26 D3
25 B3
24 F3
23 E3
22 AB4
21 POL
(MINUS SIGN)
1's
10's
100's
1000's
NORMAL PIN CONFIGURATION
TSC7107
1 V+
2 D1
3 C1
4 B1
5 A1
6 F1
7 G1
8 E1
9 D2
10 C2
11 B2
12 A2
13 F2
14 E2
15 D3
16 B3
17 F3
18 E3
19 AB4
20 POL
(MINUS SIGN)
1's
10's
100's
1000's
40 OSC1
39 OSC2
38 OSC3
37 TEST
36 V+REF
35 V−REF
34 C+REF
33 C−REF
32 ANALOG COMMON
31 V+IN
30 V−IN
29 CAZ
28 VBUFF
27 VINT
26 V−
25 G2
24 C3
23 A3
22 G3
21 GND
100's
REVERSE PIN CONFIGURATION
TSC7107R
1 OSC1
2 OSC2
3 OSC3
4 TEST
5 V+REF
6 V−REF
7 C+REF
8 C−REF
9 ANALOG COMMON
10 V+IN
11 V−IN
12 CAZ
13 VBUFF
14 VINT
15 V−
16 G2
17 C3
18 A3
19 G3
20 GND
100's
40 V+
39 D1
38 C1
37 B1
36 A1
35 F1
34 G1
33 E1
32 D2
31 C2
30 B2
29 A2
28 F2
27 E2
26 D3
25 B3
24 F3
23 E3
22 AB4
21 POL
(MINUS SIGN)
1's
10's
100's
1000's

Pin Configuration (Continued)


45 V⁻
44 NC
43 G2
42 NC
41 C3
40 A3
39 NC
38 SUB
37 G3
36 BP
35 POL
34 AB4
33 E3
32 F3
31 B3
46 VINT
47 VBUFF
48 NC
49 CAZ
50 NC
51 V−IN
52 NC
53 SUB
54 NC
55 V+IN
56 NC
57 COMMON
58 C−REF
59 C+REF
60 V−REF
30 D3
29 E2
28 F2
27 A2
26 B2
25 C2
24 NC
23 SUB
22 NC
21 D2
20 E1
19 G1
18 F1
17 A1
16 B1
1 V+REF
2 NC
3 TEST
4 OSC3
5 NC
6 OSC2
7 NC
8 SUB
9 NC
10 OSC1
11 NC
12 NC
13 V+
14 D1
15 C1
TSC7106 BQ
TSC7106 SQ

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.


45 V⁻
44 NC
43 G2
42 NC
41 C3
40 A3
39 NC
38 SUB
37 G3
36 GND
35 POL
34 AB4
33 E3
32 F3
31 B3
46 VINT
47 VBUFF
48 NC
49 CAZ
50 NC
51 V−IN
52 NC
53 SUB
54 NC
55 V+IN
56 NC
57 COMMON
58 C−REF
59 C+REF
60 V−REF
30 D3
29 E2
28 F2
27 A2
26 B2
25 C2
24 NC
23 SUB
22 NC
21 D2
20 E1
19 G1
18 F1
17 A1
16 B1
1 V+REF
2 NC
3 TEST
4 OSC3
5 NC
6 OSC2
7 NC
8 SUB
9 NC
10 OSC1
11 NC
12 NC
13 V+
14 D1
15 C1
TSC7107 BQ
TSC7107 SQ

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7106CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7106RCPL	40-Pin Plastic Dip	Reverse	0°C to +70°C	LCD
TSC7106IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LCD
TSC7106CJL	40-Pin CerDIP	Normal	0°C to +70°C	LCD
TSC7106IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7106CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TSC7106CSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LCD
TSC7107CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7107RCPL	40-Pin Plastic Dip	Reverse	0°C to +70°C	LED
TSC7107IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LED
TSC7107CJL	40-Pin CerDIP	Normal	0°C to +70°C	LED

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7107IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LED
TSC7107CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TSC7107CSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LED
Devices with Burn-In (160 Hours at +125°C)				
TSC7106CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7106RCPL/BI	40-Pin Plastic Dip	Reverse	0°C to +70°C	LCD
TSC7106IJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7107CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7107RCPL/BI	40-Pin Plastic Dip	Reverse	0°C to +70°C	LED
TSC7107IJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C	LED

Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.
9	(32)	21	D_2	Activates the D section of the tens display.
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP GND	TSC7106: LCD Backplane drive output. TSC7107: Digital Ground.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ for a 200 mV full-scale range and a 470 kΩ for 2 V full-scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for a 200 mV full-scale, and a 0.047 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The analog low input is connected to this pin.
31	(10)	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.
34	(7)	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
36	(5)	1	V^{+}_{REF}	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^{+}) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the TSC7106 and TSC7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) reference (REF).

Auto-Zero Phase

Input high and low are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

Signal Integrate Phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between V^{+}_{IN} and V^{-}_{IN} for a fixed time. This differential voltage can be within a wide common-mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, V^{-}_{IN} can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Reference Integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is:

$$1000 \text{ X } \frac{V_{IN}}{V_{REF}}$$

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. By selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worse case condition. (See Component Values Selection.)

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2 V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

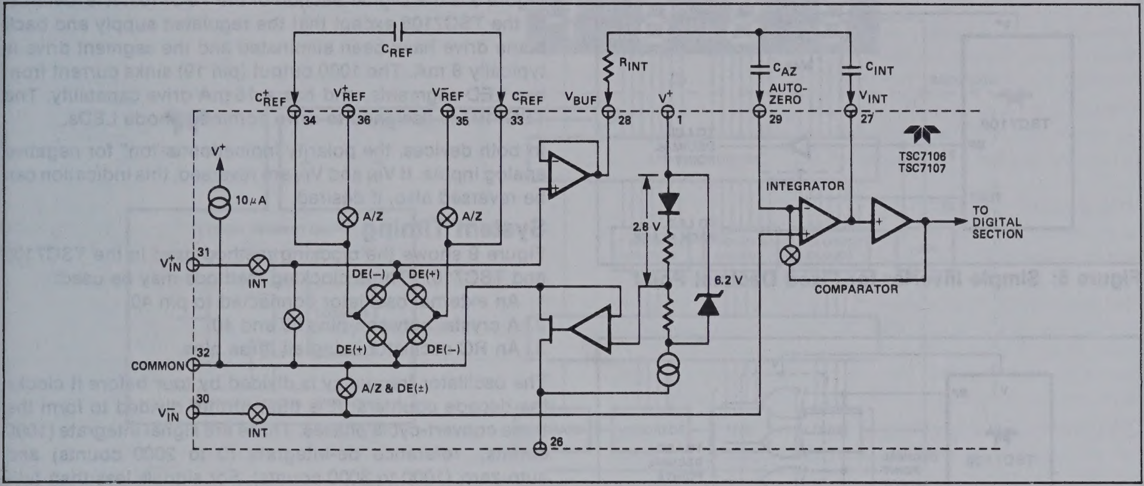

C_{REF}
C_{REF}^+
34
V_{REF}^+
36
V_{REF}^-
35
C_{REF}^-
33
V_{BUF}
28
R_{INT}
V^+
1
C_{AZ}
AUTO-ZERO
29
C_{INT}
V_{INT}
27
TSC7106
TSC7107
INTEGRATOR
TO DIGITAL SECTION
COMPARATOR
2.8 V
6.2 V
V^+
10 μA
A/Z
A/Z
V_{IN}^+
31
INT
DE(−)
DE(+)
DE(+)
DE(−)
COMMON
32
A/Z & DE(±)
V_{IN}^-
30
INT
26

Figure 3: Analog Section of TSC7106/TSC7107

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation (TSC7106) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6 V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7 V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈15 Ω), and a temperature coefficient of 80 ppm/°C typically.

An external reference may be added to improve temperature stability or the TSC7106A/TSC7107A devices with lower analog common temperature drift may be used. The circuit is shown in Figure 4.

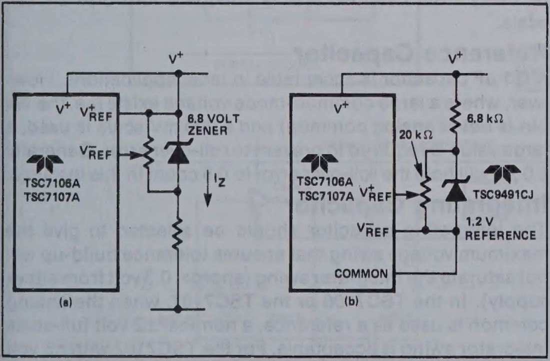

V^+
V^+
V_{REF}^+
V_{REF}^-
6.8 VOLT ZENER
I_Z
TSC7106A
TSC7107A
(a)
V^+
V^+
6.8 kΩ
20 kΩ
TSC7106A
TSC7107A
V_{REF}^+
V_{REF}^-
TSC9491CJ
1.2 V REFERENCE
COMMON
(b)

Figure 4: Using an External Reference

Analog common is also used as the V_{IN}^- return during auto-zero and deintegrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications V_{IN}^- will be set at a fixed known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog common, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET that can sink 30 mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10 μA of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. On the TSC7107 it is coupled to the internally generated digital supply through a 500 Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read −1888. The TEST pin will sink about 10 mA under these conditions.

Caution: On the TSC7106, in the lamp test mode the segments have a constant dc voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

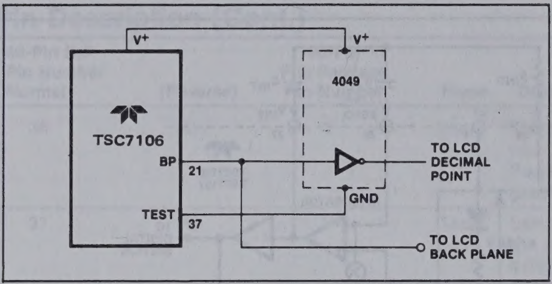


Figure 5: Simple Inverter for Fixed Decimal Point

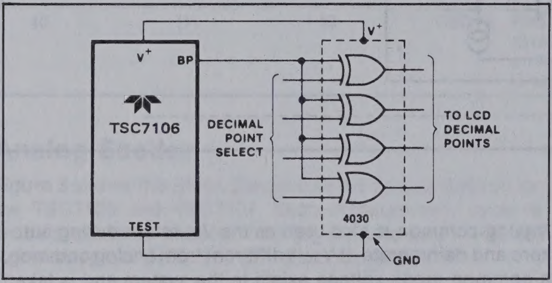


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

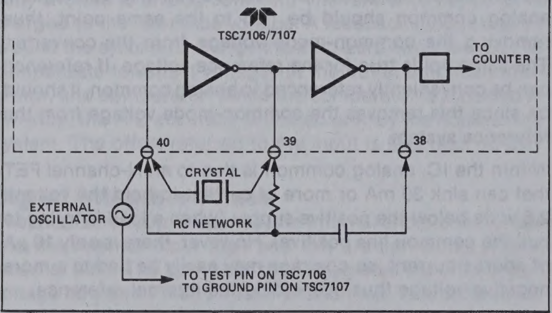


Figure 7: Clock Circuits

Digital Section

Figures 8 and 9 show the digital section for the TSC7106 and TSC7107, respectively. In the TSC7106 (Figure 8), an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible dc voltage exists across the segments.

Figure 9 is the Digital Section of the TSC7107. It is identical to the TSC7106 except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TSC7107 is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

System Timing

Figure 9 shows the clocking method used in the TSC7106 and TSC7107. Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full-scale auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Component Value Selection

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full-scale where noise is very important, a 0.47 μF capacitor is recommended. On the 2 volt scale, a 0.047 μF capacitor increase the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common-mode voltage exists (i.e. the V_{IN}^- pin is not at analog common) and a 200 mV scale is used, a large value is required to prevent to roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the TSC7106 or the TSC7107, when the analog common is used as a reference, a nominal ±2 volt full-scale integrator swing is acceptable. For the TSC7107 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to

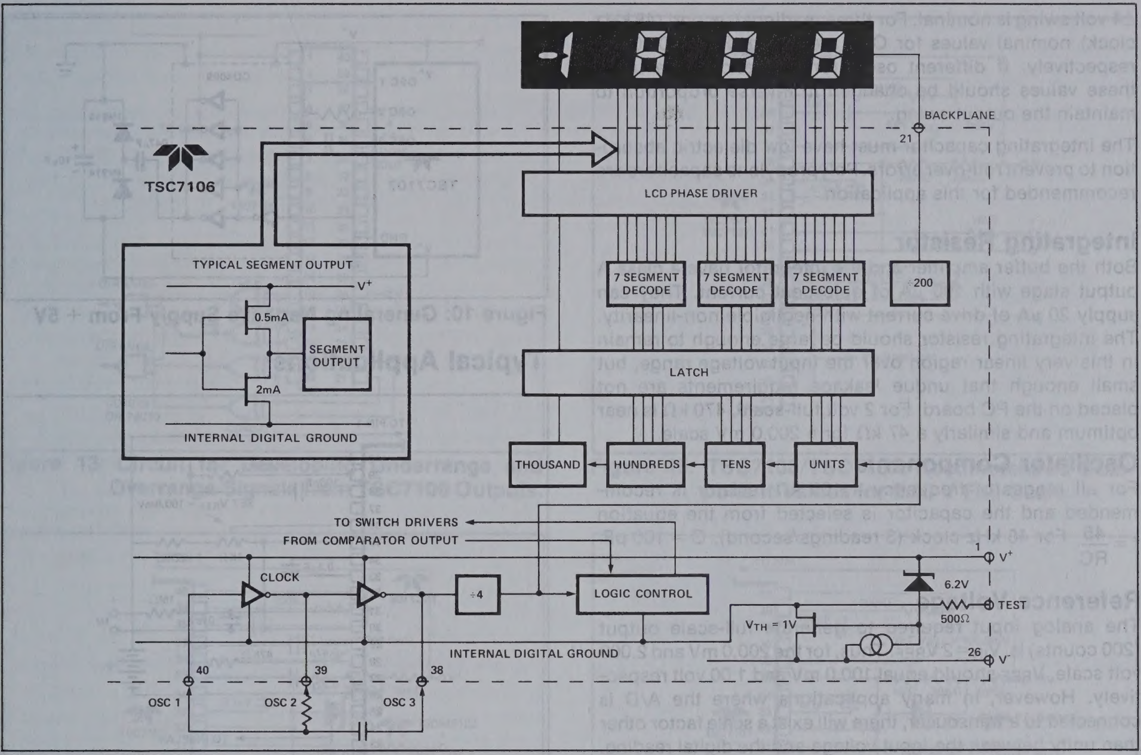

-1 8 8 8
BACKPLANE
21
TSC7106
LCD PHASE DRIVER
TYPICAL SEGMENT OUTPUT
V+
0.5mA
SEGMENT OUTPUT
2mA
INTERNAL DIGITAL GROUND
7 SEGMENT DECODE
7 SEGMENT DECODE
7 SEGMENT DECODE
÷200
LATCH
THOUSAND
HUNDREDS
TENS
UNITS
TO SWITCH DRIVERS
FROM COMPARATOR OUTPUT
1
V+
CLOCK
÷4
LOGIC CONTROL
6.2V
TEST
500Ω
VTH = 1V
INTERNAL DIGITAL GROUND
26
V-
40
39
38
OSC 1
OSC 2
OSC 3

Figure 8: TSC7106 Digital Section

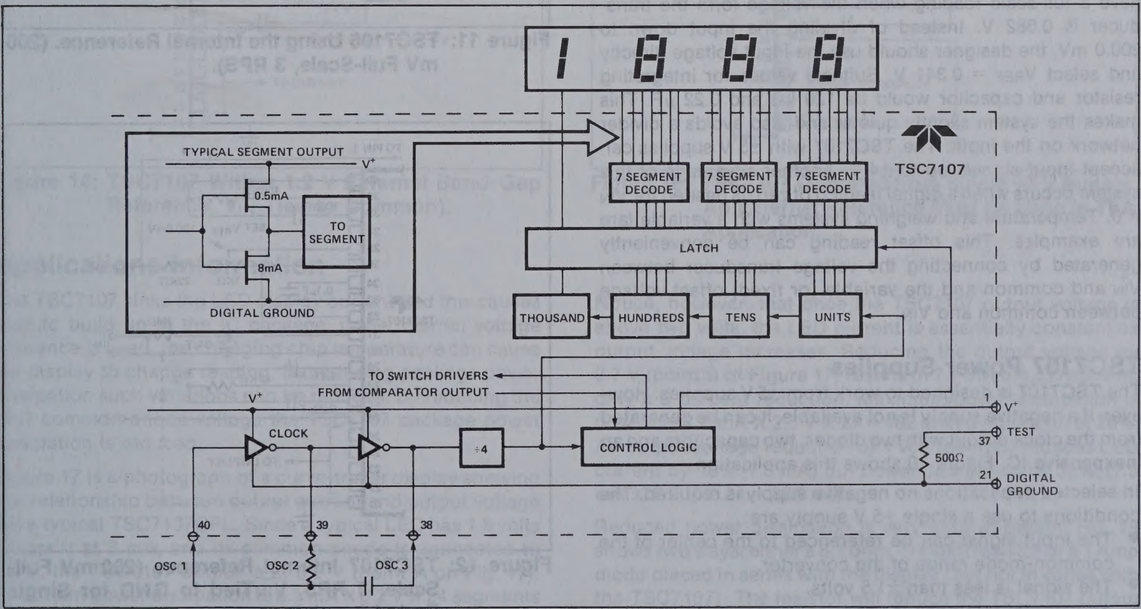

1 8 8 8
TSC7107
TYPICAL SEGMENT OUTPUT
V+
0.5mA
TO SEGMENT
8mA
DIGITAL GROUND
7 SEGMENT DECODE
7 SEGMENT DECODE
7 SEGMENT DECODE
LATCH
THOUSAND
HUNDREDS
TENS
UNITS
TO SWITCH DRIVERS
FROM COMPARATOR OUTPUT
V+
CLOCK
÷4
CONTROL LOGIC
1
V+
TEST
37
500Ω
21
DIGITAL GROUND
40
39
38
OSC 1
OSC 2
OSC 3

Figure 9: TSC7107 Digital Section

±4 volt swing is nominal. For three readings/second (48 kHz clock) nominal values for C_{INT} are 0.22 µ1F and 0.10 µF, respectively. If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 µA of quiescent current. They can supply 20 µA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full-scale, 470 kΩ is near optimum and similarly a 47 kΩ for a 200.0 mV scale.

Oscillator Components

For all ranges of frequency a 100 kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$ For 48 kHz clock (3 readings/second), C = 100 pF.

Reference Voltage

The analog input required to generate full-scale output (200 counts) is: $V_{IN} = 2\,V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.00 volt respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage form the transducer is 0.682 V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select V_{REF} = 0.341 V. Suitable values for integrating resistor and capacitor would be 120 kΩ and 0.22 µF. This makes the system slightly quieter and also avoids a divider network on the input. The TSC7107 with ±5 V supplies can accept input signals up to ±4 V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between V_{IN}^{+} and common and the variable (or fixed) offset voltage between common and V_{IN}^{-}.

TSC7107 Power Supplies

The TSC7107 is designed to work from ±5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors and an inexpensive IC. Figure 10 shows this application.

In selected applications no negative supply is required. The conditions to use a single +5 V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5 volts.
- An external reference is used.

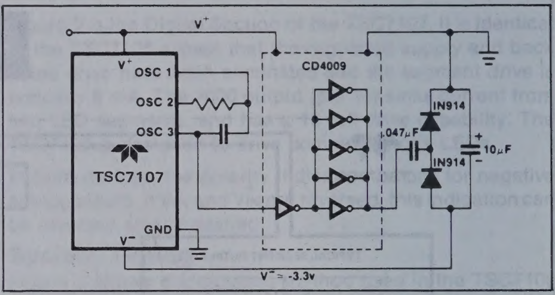

V+
V+
OSC 1
OSC 2
OSC 3
TSC7107
GND
V−
CD4009
IN914
.047µF
+
10µF
IN914
−
V− = -3.3v

Figure 10: Generating Negative Supply From + 5V

Typical Applications

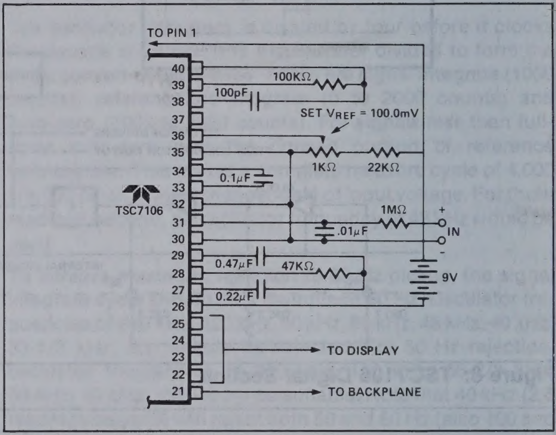

TO PIN 1
40
39
38
37
36
35
34
33
32
31
30
29
28
27
26
25
24
23
22
21
100KΩ
100pF
SET VREF = 100.0mV
1KΩ
22KΩ
0.1µF
TSC7106
1MΩ
+
IN
.01µF
−
0.47µF
47KΩ
9V
0.22µF
TO DISPLAY
TO BACKPLANE

Figure 11: TSC7106 Using the Internal Reference. (200 mV Full-Scale, 3 RPS).

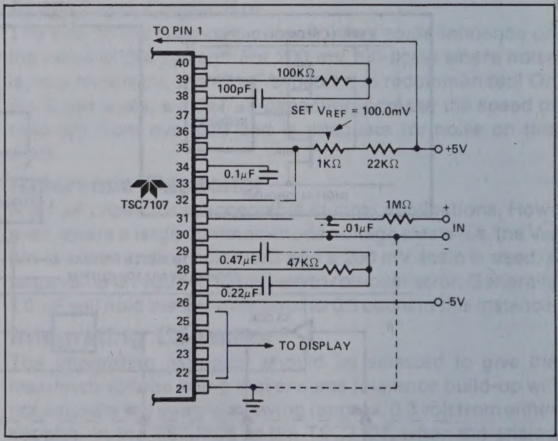

TO PIN 1
40
39
38
37
36
35
34
33
32
31
30
29
28
27
26
25
24
23
22
21
100KΩ
100pF
SET VREF = 100.0mV
+5V
1KΩ
22KΩ
0.1µF
TSC7107
1MΩ
+
IN
.01µF
−
0.47µF
47KΩ
0.22µF
-5V
TO DISPLAY

Figure 12: TSC7107 Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN}^{-} Tied to GND for Single Ended Inputs).

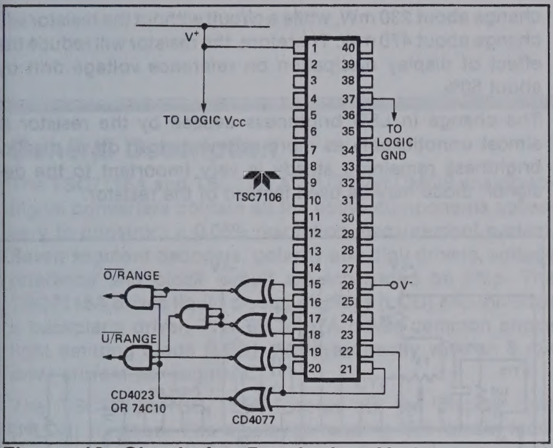

V+
TO LOGIC VCC
TO LOGIC GND
TSC7106
O/RANGE
U/RANGE
V-
CD4023 OR 74C10
CD4077

Figure 13: Circuit for Developing Underrange and Overrange Signals from TSC7106 Outputs.

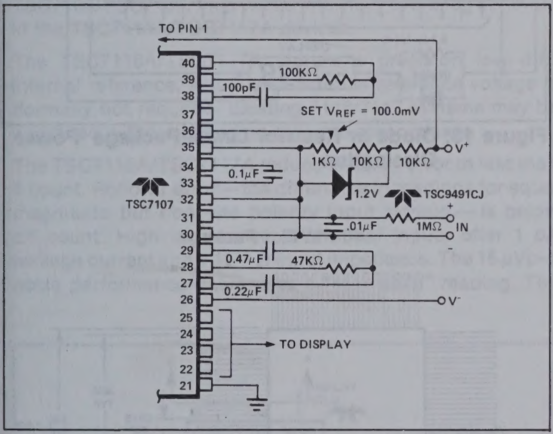

TO PIN 1
100KΩ
100pF
SET VREF = 100.0mV
1KΩ
10KΩ
10KΩ
V+
0.1μF
TSC7107
1.2V
TSC9491CJ
.01μF
1MΩ
IN
0.47μF
47KΩ
0.22μF
V-
TO DISPLAY

Figure 14: TSC7107 With a 1.2 V External Band-Gap Reference. V_{IN} Tied to Common).

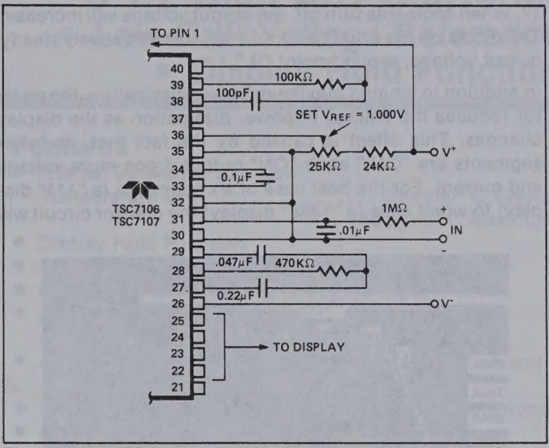

TO PIN 1
100KΩ
100pF
SET VREF = 1.000V
25KΩ
24KΩ
V+
0.1μF
TSC7106
TSC7107
1MΩ
.01μF
IN
.047μF
470KΩ
0.22μF
V-
TO DISPLAY

Figure 15: TSC7106/TSC7107: Recommended Component Values for 2.00 V Full-Scale.

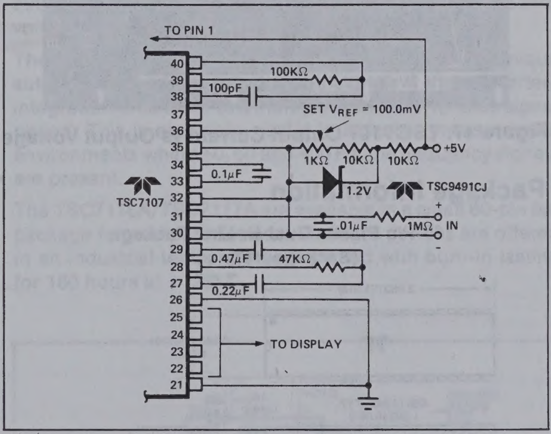

TO PIN 1
100KΩ
100pF
SET VREF = 100.0mV
1KΩ
10KΩ
10KΩ
+5V
0.1μF
TSC7107
1.2V
TSC9491CJ
.01μF
1MΩ
IN
0.47μF
47KΩ
0.22μF
TO DISPLAY

Figure 16: TSC7107 Operated from Single +5 V Supply. An External Reference Must Be Used in This Application.

Applications Information

The TSC7107 sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TSC7107 package power dissipation is reduced.

Figure 17 is a photograph of a curve-tracer display showing the relationship between output current and output voltage for a typical TSC7107CPL. Since a typical LED has 1.8 volts across it at 8 mA, and its common anode is connected to +5 V, the TSC7107 output is at 3.2 V (point A on Fig. 17). Maximum power dissipation is 8.1 mA X 3.2 V X 24 segments = 622 mW.

Notice, however, that once the TSC7107 output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B of Figure 17) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is now only 7.7 mA X 2.5 V X 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA X 2.2 V X 24 = 385 mW).

Reduced power dissipation is very easy to obtain. Fig. 18 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TSC7107). The resistor will reduce the TSC7107 output voltage, when all 24 segments are "ON," to point "C" of Fig.

17. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor circuit will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, diode may be used instead of the resistor.

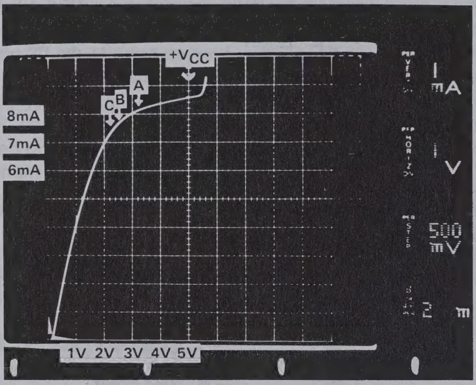


Figure 17: TSC7107 Output Current vs Output Voltage

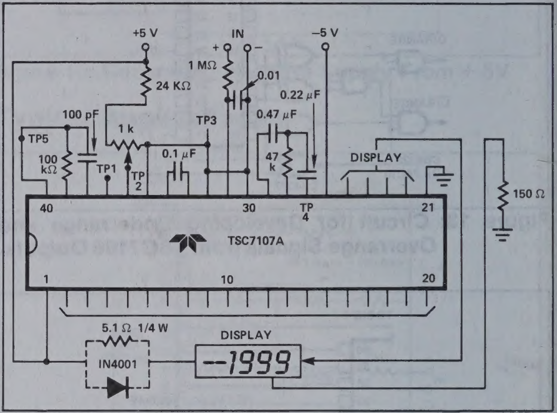
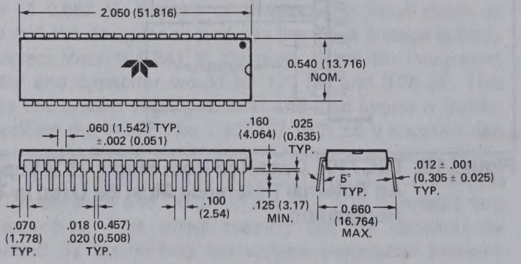

+5 V
IN
+
–
–5 V
1 MΩ
24 KΩ
0.01
0.22 μF
0.47 μF
100 pF
TP3
1 k
TP5
100 kΩ
TP1
TP 2
0.1 μF
47 k
DISPLAY
150 Ω
40
30
TP 4
21
TSC7107A
1
10
20
5.1 Ω 1/4 W
IN4001
DISPLAY
-1999

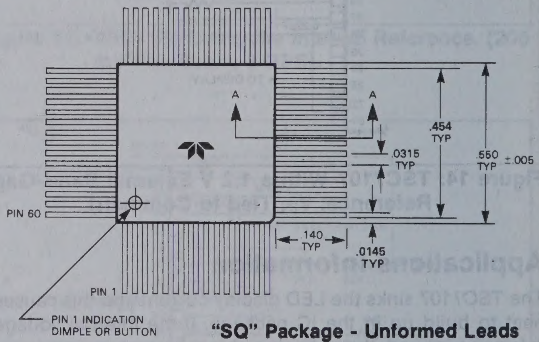
Figure 18: Diode or Resistor Limits Package Power Dissipation

Package Information

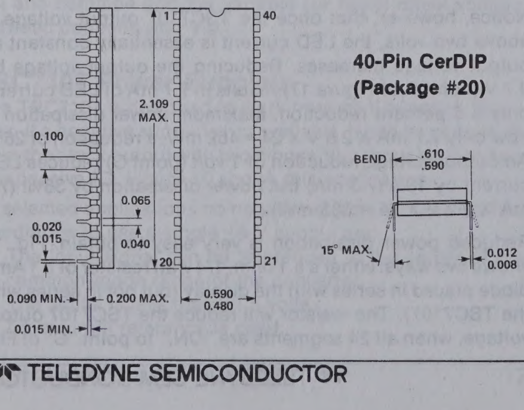
40-Pin Plastic Dual-In-Line Package (Package #17)


2.050 (51.816)
0.540 (13.716) NOM.
.060 (1.542) TYP.
±.002 (0.051)
.160 (4.064)
.025 (0.635) TYP.
.012 ± .001 (0.305 ± 0.025) TYP.
5° TYP.
.100 (2.54)
.125 (3.17) MIN.
0.660 (16.764) MAX.
.070 (1.778) TYP.
.018 (0.457)
.020 (0.508) TYP.

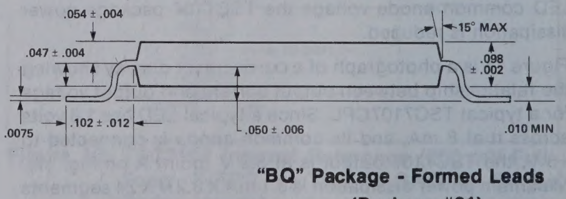
60-Pin Flat Package


A
A
.454 TYP
.550 ±.005 TYP
.0315 TYP
PIN 60
140 TYP
.0145 TYP
PIN 1
PIN 1 INDICATION DIMPLE OR BUTTON

"SQ" Package - Unformed Leads (Package #22)


1
40
2.109 MAX.
0.100
0.065
0.020
0.015
0.040
20
21
0.090 MIN.
0.200 MAX.
0.590
0.480
0.015 MIN.
BEND
.610
.590
15° MAX.
0.012
0.008

40-Pin CerDIP (Package #20)


.054 ± .004
.047 ± .004
15° MAX
.098 ± .002
.0075
.102 ± .012
.050 ± .006
.010 MIN

"BQ" Package - Formed Leads (Package #21)

TELEDYNE SEMICONDUCTOR

TSC7116A (LCD Drive)
TSC7117A (LED Drive)
3 1/2 Digit A/D Converter
• Low Drift Voltage Reference
• Display Hold Function

General Description

The TSC7116A and TSC7117A 3-1/2 digit CMOS analog-to-digital converters contain all the active components necessary to construct a 0.05% resolution measurement system. Seven segment decoders, polarity and digit drivers, voltage reference and clock circuit are integrated on chip. The TSC7116A drives liquid crystal displays (LCD) and includes a backplane driver. The TSC7117A drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment.

The TSC7116A/TSC7117A incorporate the display hold (HLDR) function. The displayed reading will remain indefinitely as long as HLDR is held high. Conversions continue but the output data display latches are not updated. The V_{REF}^- or reference low input is not available as it is with the TSC7106/TSC7107. V_{REF}^- is tied internally to analog common in the TSC7116A/TSC7117A devices.

The TSC7116A/TSC7117A feature a precision low drift internal reference. A low drift external reference voltage is normally not required. Existing 7116/7117 systems may be upgraded without changing external components.

The TSC7116A/TSC7117A reduce linearity error to less than 1 count. Rollover error—the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High impedance differential inputs offer 1 pA leakage current and a $10^{12}\ \Omega$ input impedance. The 15 μVp-p noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

The TSC7116A/TSC7117A dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The TSC7116A/TSC7117A are available in a small 60-pin flat package for compact designs. Standard devices are offered in an industrial temperature range and with burn-in lasting for 160 hours at +125° C.

Features

- Internal Reference with Low Temperature Drift .... 20 ppm/° C Typical
  50 ppm/° C Maximum
- Display Hold Function
- Drives LCD or LED Displays Directly
- Guaranteed Zero Reading with Zero Input
- Low Noise for Stable Display
  -2.000 V or 200.0 mV Full-Scale Range
- Auto-Zero Cycle Eliminates Need for Zero Adjustment Potentiometer
- True Polarity Indication for Precision Null Applications
- Convenient 9 V Battery Operation (TSC7116A)
- High Impedance CMOS Differential Inputs ..... $10^{12}\ \Omega$
- Low Power Operation .... 10 mW

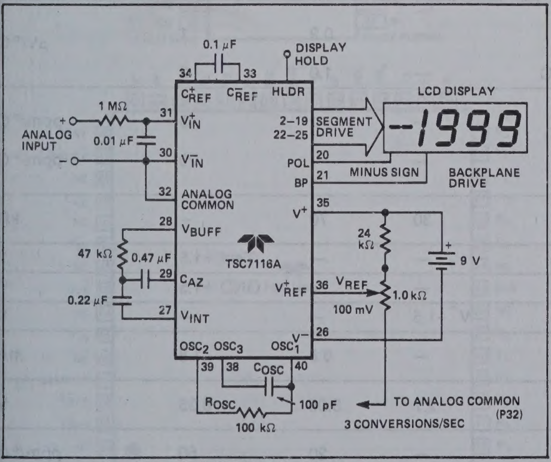

0.1 µF
DISPLAY HOLD
34
33
C_{REF}^+
C_{REF}^-
HLDR
LCD DISPLAY
1 MΩ
+
ANALOG INPUT
–
31
V_{IN}^+
0.01 µF
30
V_{IN}^-
2–19
22–25
SEGMENT DRIVE
-1999
20
POL
21
BP
MINUS SIGN
BACKPLANE DRIVE
32
ANALOG COMMON
V+
35
28
V_{BUFF}
24 kΩ
9 V
47 kΩ
0.47 µF
29
C_{AZ}
TSC7116A
0.22 µF
27
V_{INT}
36
V_{REF}^+
1.0 kΩ
100 mV
26
V–
OSC2 OSC3 OSC1
39 38 40
C_{OSC}
R_{OSC}
100 kΩ
100 pF
TO ANALOG COMMON (P32)
3 CONVERSIONS/SEC

Figure 1: Typical TSC7116A Operating Circuit

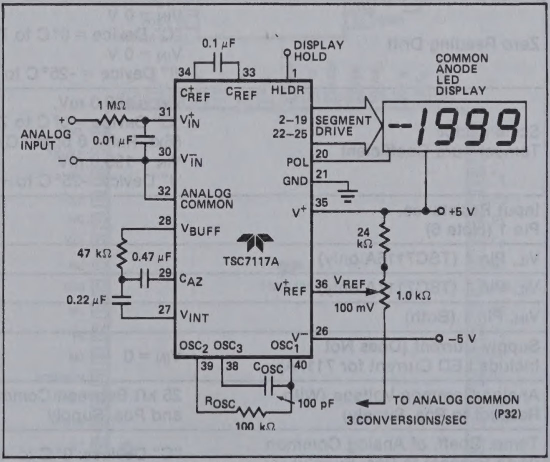

0.1 µF
DISPLAY HOLD
1
34
33
C_{REF}^+
C_{REF}^-
HLDR
COMMON ANODE LED DISPLAY
1 MΩ
+
ANALOG INPUT
–
31
V_{IN}^+
0.01 µF
30
V_{IN}^-
2–19
22–25
SEGMENT DRIVE
-1999
20
POL
21
GND
32
ANALOG COMMON
V+
35
+5 V
28
V_{BUFF}
24 kΩ
47 kΩ
0.47 µF
29
C_{AZ}
TSC7117A
0.22 µF
27
V_{INT}
36
V_{REF}^+
1.0 kΩ
100 mV
26
V–
–5 V
OSC2 OSC3 OSC1
39 38 40
C_{OSC}
R_{OSC}
100 kΩ
100 pF
TO ANALOG COMMON (P32)
3 CONVERSIONS/SEC

Figure 2: Typical TSC7117A Operating Circuit

Absolute Maximum Ratings

TSC7116A

Supply Voltage (V^+ to V^-)	15 V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	Test to V^+
Power Dissipation (Note 2)	
CerDIP Package	1000 mW
Plastic Package	800 mW
Operating Temperature	
"C" Devices	0° C to +70° C
"I" Devices	-25° C to +85° C
Storage Temperature	-65° C to +160° C
Lead Temperature (Soldering, 60 sec)	300° C

TSC7117A

Supply Voltage	
V^+	+6 V
V^-	-9 V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	GND to V^+
Power Dissipation (Note 1)	
CerDIP Package	1000 mW
Plastic Package	800 mW
Operating Temperature	
"C" Devices	0° C to +70° C
"I" Devices	-25° C to +85° C
Storage Temperature	-65° C to +160° C
Lead Temperature (Soldering, 60 sec)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

Electrical Characteristics (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	$V_{IN} = 0.0$ V Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ $V_{REF} = 100$ mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \simeq 200.0$ mV or ≈ 2.000 V	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	$V_{CM} = \pm 1$ V, $V_{IN} = 0$ V. Full-Scale = 200.0 mV	—	50	—	µV/V
Noise (Pk - Pk Value Not Exceeded 95% of Time)	$V_{IN} = 0$ V Full-Scale = 200.0 mV	—	15	—	µV
Leakage Current @ Input	$V_{IN} = 0$ V	—	1	10	pA
Zero Reading Drift	$V_{IN} = 0$ V "C" Device = 0° C to 70° C	—	0.2	1	µV/° C
	$V_{IN} = 0$ V "I" Device = -25° C to +85° C	—	1.0	2	
Scale Factor Temperature Coefficient	$V_{IN} = 199.0$ mV, "C" Device = 0° C to 70° C (Ext. Ref = 0 ppm/° C)	—	1	5	ppm/° C
	$V_{IN} = 199.0$ mV "I" Device: -25° C to +85° C	—	—	20	ppm/° C
Input Resistance, Pin 1 (Note 6)		30	70	—	kΩ
V_{IL}, Pin 1 (TSC7116A only)		—	—	Test +1.5	V
V_{IL}, Pin 1 (TSC7117A only)		—	—	GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ -1.5	—	—	V
Supply Current (Does Not Include LED Current for 7117A)	$V_{IN} = 0$	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	2.7	3.05	3.35	V
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	"C" Devices: 0° C to +70° C	—	20	50	ppm/° C
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply "I" Devices: -25° C to +85° C	—	—	75	ppm/° C

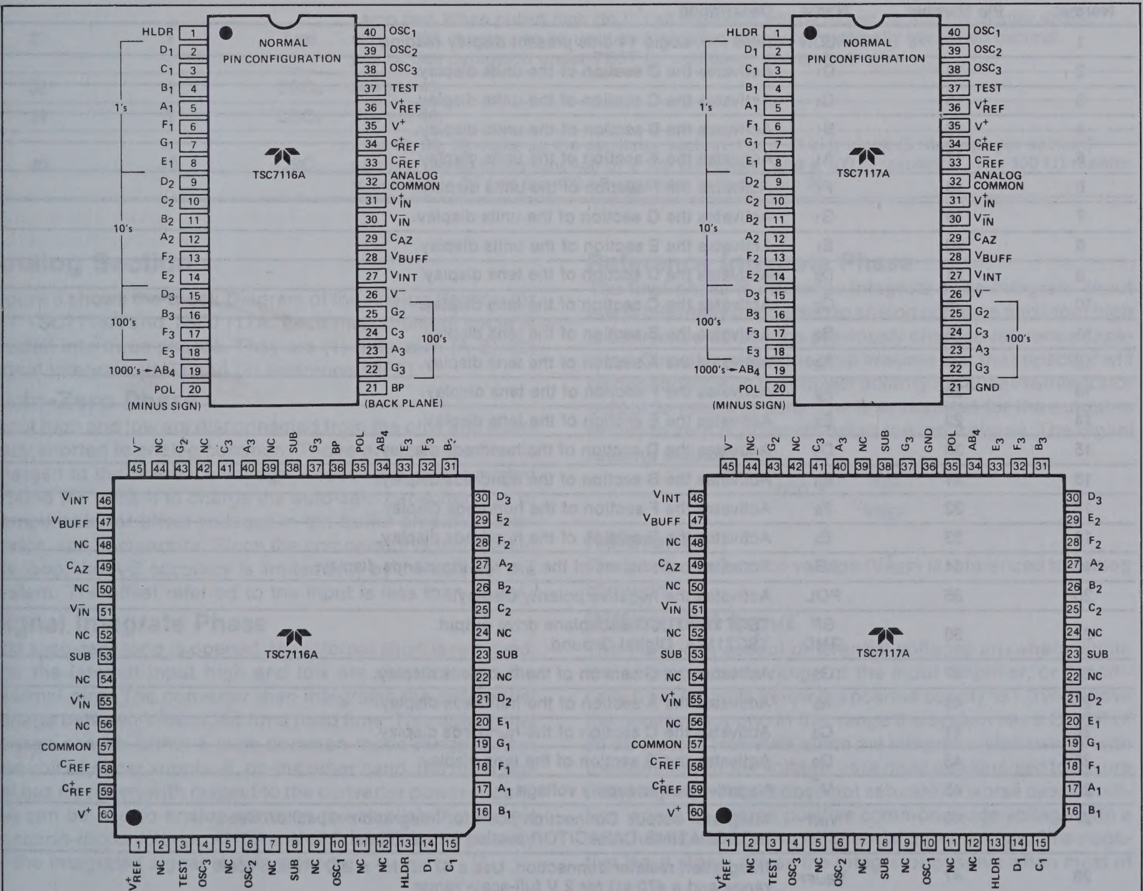
Electrical Characteristics (Cont.)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
TSC7116A ONLY Pk - Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7116A ONLY Pk - Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7117A ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	5	8.0	—	mA
TSC7117A ONLY Segment Sinking Current (Pin 19 Only)	V^+ = 5.0 V Segment Voltage = 3 V	10	16	—	mA

NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to ± 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless other wise noted, specifications apply to both the TSC7116A and TSC7117A at T_A = 25° C, f_{CLOCK} = 48 kHz. TSC7116A is tested in the circuit of Figure 1. TSC7117A is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average dc component is less than 50 mV.
6. The TSC7116A logic input has an internal pull-down resistor connected from HLDR, Pin 1, to TEST, Pin 37. The TSC7117A logic input has an internal pull-down resistor connected from HLDR, Pin 1 to GROUND, Pin 21.

Pin Configuration


NORMAL PIN CONFIGURATION
TSC7116A
1 HLDR
2 D1
3 C1
4 B1
5 A1
6 F1
7 G1
8 E1
9 D2
10 C2
11 B2
12 A2
13 F2
14 E2
15 D3
16 B3
17 F3
18 E3
19 AB4
20 POL
1's
10's
100's
1000's
(MINUS SIGN)
40 OSC1
39 OSC2
38 OSC3
37 TEST
36 V+REF
35 V+
34 C+REF
33 C−REF
32 ANALOG COMMON
31 V+IN
30 V−IN
29 CAZ
28 VBUFF
27 VINT
26 V−
25 G2
24 C3
23 A3
22 G3
21 BP
(BACK PLANE)
NORMAL PIN CONFIGURATION
TSC7117A
21 GND
45 V−
44 NC
43 G2
42 NC
41 C3
40 A3
39 NC
38 SUB
37 G3
36 BP
36 GND
35 POL
34 AB4
33 E3
32 F3
31 B3
46 VINT
47 VBUFF
48 NC
49 CAZ
50 NC
51 V−IN
52 NC
53 SUB
54 NC
55 V+IN
56 NC
57 COMMON
58 C−REF
59 C+REF
60 V+
30 D3
29 E2
28 F2
27 A2
26 B2
25 C2
24 NC
23 SUB
22 NC
21 D2
20 E1
19 G1
18 F1
17 A1
16 B1
1 V+REF
2 NC
3 TEST
4 OSC3
5 NC
6 OSC2
7 NC
8 SUB
9 NC
10 OSC1
11 NC
12 NC
13 HLDR
14 D1
15 C1

Notes: 1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7116ACPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7116AIJL	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7116ACBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TSC7116ACSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LCD
TSC7117ACPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LED

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7117AIJL	40-Pin CerDIP	Normal	-25°C to +85°C	LED
TSC7117ACBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TSC7117ACSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LED
Devices with Burn-In (160 Hours at +125°C)				
TSC7116ACPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7117ACPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LED

Pin Description

40-Pin DIP Pin Number Normal	60-Pin Flat Package Pin Number	Name	Description
1	13	HLDR	Hold Pin, Logic 1 holds present display reading.
2	14	D_1	Activates the D section of the units display.
3	15	C_1	Activates the C section of the units display.
4	16	B_1	Activates the B section of the units display.
5	17	A_1	Activates the A section of the units display.
6	18	F_1	Activates the F section of the units display.
7	19	G_1	Activates the G section of the units display.
8	20	E_1	Activates the E section of the units display.
9	21	D_2	Activates the D section of the tens display.
10	25	C_2	Activates the C section of the tens display.
11	26	B_2	Activates the B section of the tens display.
12	27	A_2	Activates the A section of the tens display.
13	28	F_2	Activates the F section of the tens display.
14	29	E_2	Activates the E section of the tens display.
15	30	D_3	Activates the D section of the hundreds display.
16	31	B_3	Activates the B section of the hundreds display.
17	32	F_3	Activates the F section of the hundreds display.
18	33	E_3	Activates the E section of the hundreds display.
19	34	AB_4	Activates both halves of the 1 in the thousands display.
20	35	POL	Activates the negative polarity display.
21	36	BP GND	TSC7116A: LCD Backplane drive output. TSC7117A: Digital Ground.
22	37	G_3	Activates the G section of the hundreds display.
23	40	A_3	Activates the A section of the hundreds display.
24	41	C_3	Activates the C section of the hundreds display.
25	43	G_2	Activates the G section of the tens display.
26	45	V^-	Negative power supply voltage.
27	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for additional details.
28	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ for a 200 mV full-scale range and a 470 kΩ for 2 V full-scale range.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	60-Pin Flat Package Pin Number	Name	Description
29	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 µF capacitor for a 200 mV full-scale, and a 0.047 µF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	51	V_{IN}^-	The analog low input is connected to this pin.
31	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	58	C_{REF}^-	See pin 34.
34	59	C_{REF}^+	A 0.1 µF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1.0 µF is recommended and will hold the rollover error to 0.5 count.
35	60	V^+	Positive Power Supply Voltage.
36	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 32 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 32 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	4	OSC_3	See pin 40.
39	6	OSC_2	See pin 40.
40	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the TSC7116A and TSC7117A. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) reference (REF).

Auto-Zero Phase

Input high and low are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 µV.

Signal Integrate Phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between V_{IN}^+ and V_{IN}^- for a fixed time. This differential voltage can be within a wide common-mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, V_{IN}^- can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Reference Integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Reference

The positive reference voltage (V_{REF}^+) is referenced to analog common.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of

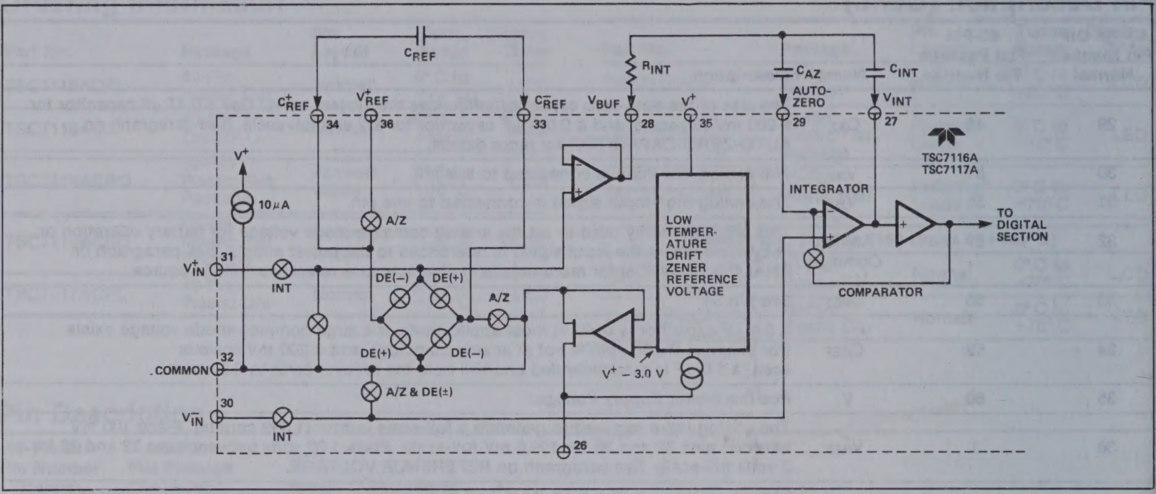


Figure 3: Analog Section of TSC7116A/TSC7117A

its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2 V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation (TSC7116A) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 3.0 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6 V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7 V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≃15 Ω), and a temperature coefficient of 20 ppm/° C typically.

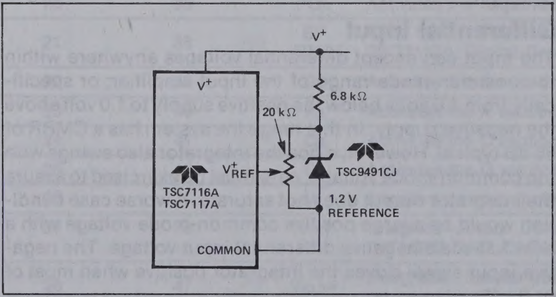


Figure 4: Using an External Reference

An external reference may be may be used if necessary. The circuit is shown in Figure 4.

Analog common is also used as the V_{IN}^- return during auto-zero and deintegrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications V_{IN}^- will be set at a fixed known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog common, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET that can sink 30 mA or more of current to hold the voltage 3.0 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10 μA of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. On the TSC7117A it is coupled to the internally generated digital supply through a 500 Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read −1888. The TEST pin will sink about 10 mA under these conditions.

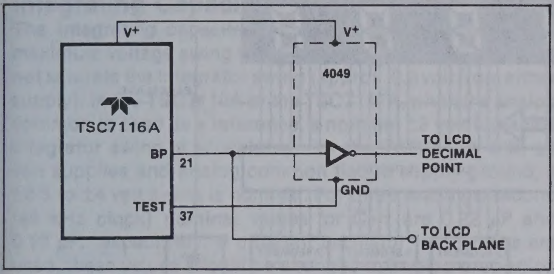


Figure 5: Simple Inverter for Fixed Decimal Point

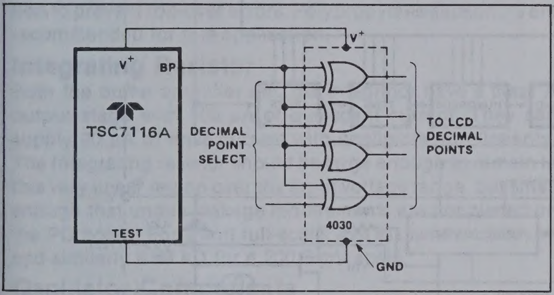


Figure 6: Exclusive "OR" Gate for Decimal Point Drive

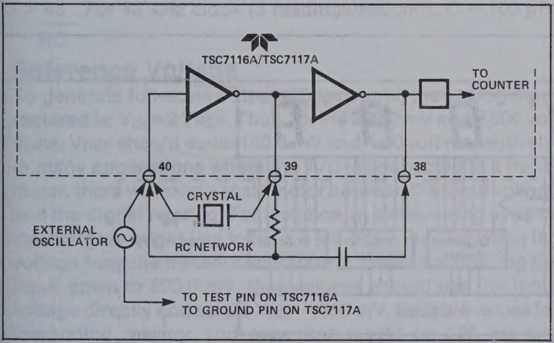


Figure 7: Clock Circuits

Digital Section

Figures 8 and 9 show the digital section for the TSC7116A and TSC7117A, respectively. In the TSC7116A (Figure 8), an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible dc voltage exists across the segments.

Figure 9 is the Digital Section of the TSC7117A. It is identical to the TSC7116A except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TSC7117A is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

System Timing

Figure 9 shows the clocking method used in the TSC7116A and TSC7117A. Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full-scale auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

HOLD Reading Input

When HLDR is at a logic "HI" the latch will not be updated. A/D conversions will continue but will not be updated until the HLDR is returned to "LOW". To continuously update the display connect to TEST (TSC7116A) or GROUND (TSC7117A) or disconnect. This input is CMOS compatible with 70K typical resistance to TEST (TSC7116A) or GROUND (TSC7117A).

Component Value Selection

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full-scale where noise is very important, a 0.47 µF capacitor is recommended. On the 2 volt scale, a 0.047 µF capacitor increase the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1 µF capacitor is acceptable in most applications. However, where a large common-mode voltage exists (i.e. the V_{IN}^- pin is not at analog common) and a 200 mV scale is used, a large value is required to prevent to roll-over error. Generally 1.0 µF will hold the roll-over error to 0.5 count in this instance.

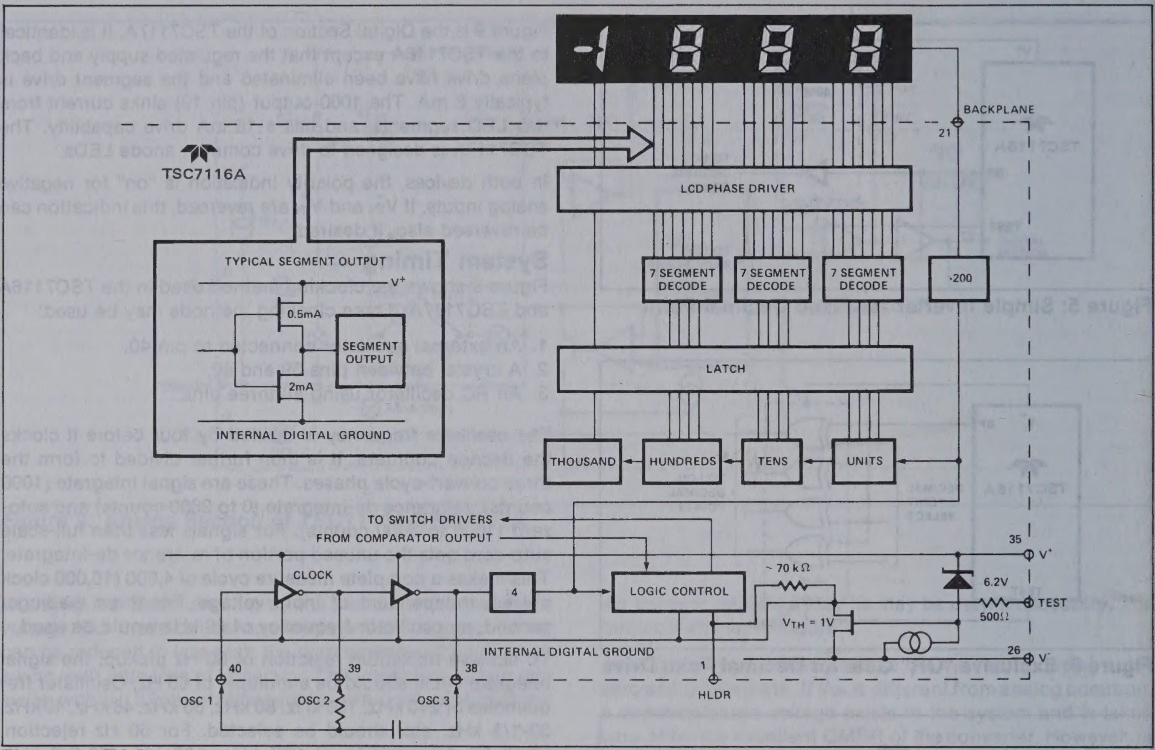

TSC7116A
BACKPLANE
21
LCD PHASE DRIVER
TYPICAL SEGMENT OUTPUT
V+
0.5mA
SEGMENT OUTPUT
2mA
INTERNAL DIGITAL GROUND
7 SEGMENT DECODE
7 SEGMENT DECODE
7 SEGMENT DECODE
÷200
LATCH
THOUSAND
HUNDREDS
TENS
UNITS
TO SWITCH DRIVERS
FROM COMPARATOR OUTPUT
CLOCK
4
LOGIC CONTROL
~ 70 kΩ
VTH = 1V
35
V+
6.2V
TEST
500Ω
26
V-
INTERNAL DIGITAL GROUND
40
39
38
OSC 1
OSC 2
OSC 3
1
HLDR

Figure 8: TSC7116A Digital Section

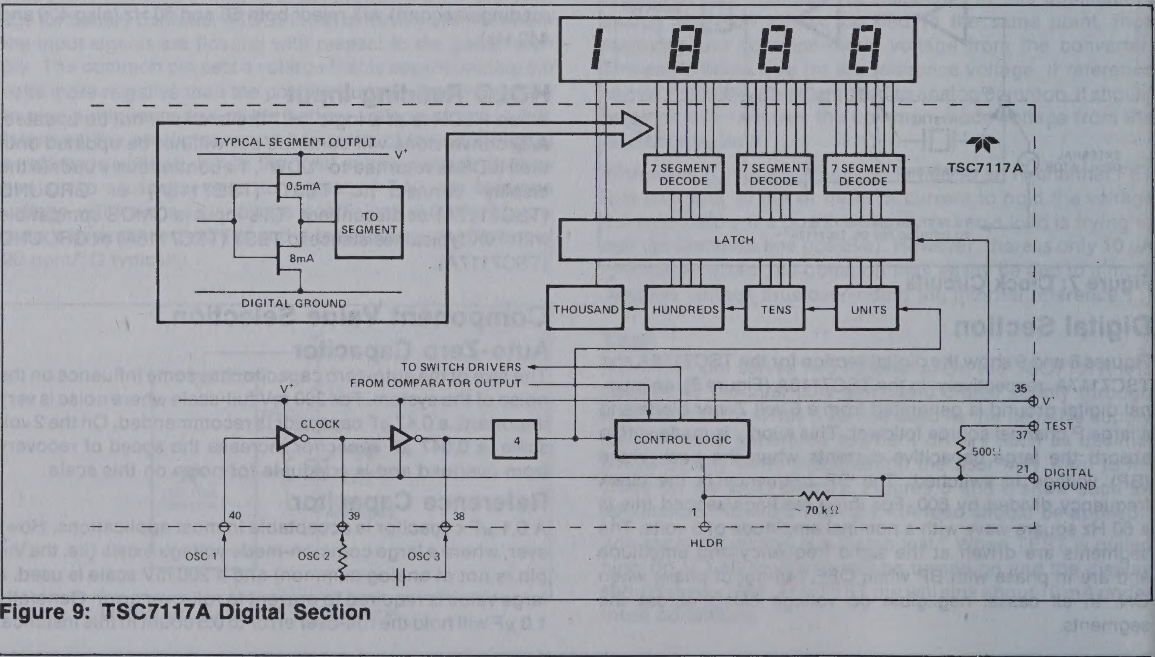

TYPICAL SEGMENT OUTPUT
V+
0.5mA
TO SEGMENT
8mA
DIGITAL GROUND
7 SEGMENT DECODE
7 SEGMENT DECODE
7 SEGMENT DECODE
TSC7117A
LATCH
THOUSAND
HUNDREDS
TENS
UNITS
TO SWITCH DRIVERS
FROM COMPARATOR OUTPUT
V+
CLOCK
4
CONTROL LOGIC
35
V+
TEST
37
500Ω
21
DIGITAL GROUND
~ 70 kΩ
1
40
39
38
OSC 1
OSC 2
OSC 3
HLDR

Figure 9: TSC7117A Digital Section

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the TSC7116A or the TSC7117A, when the analog common is used as a reference, a nominal ±2 volt full-scale integrator swing is acceptable. For the TSC7117A with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48 kHz clock) nominal values for C_{INT} are 0.22 μF and 0.10 μF, respectively. If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. They can supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full-scale, 470 kΩ is near optimum and similarly a 47 kΩ for a 200.0 mV scale.

Oscillator Components

For all ranges of frequency a 100 kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$. For 48 kHz clock (3 readings/second), C = 100 pF.

Reference Voltage

To generate full-scale output (2000 counts) the analog input required is: $V_{IN} = 2 V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.00 volt respectively. In many applications where the A/D is connected to a transducer, there will exist a scale factor between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage from the transducer is 700 mV. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select V_{REF} = 350 mV. Suitable values for integrating resistor and capacitor would be 120 kΩ and 0.22 μF. This makes the system slightly quieter and also avoids a divider network on the input. The TSC7117A with ±5 V supplies can accept input signals up to ±4 V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between V_{IN}^{+} and common and the variable (or fixed) offset voltage between common and V_{IN}^{-}.

TSC7117A Power Supplies

The TSC7117A is designed to work from ±5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors and an inexpensive IC. Figure 10 shows this application.

In selected applications no negative supply is required. The conditions to use a single +5 V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5 volts.
- An external reference is used.

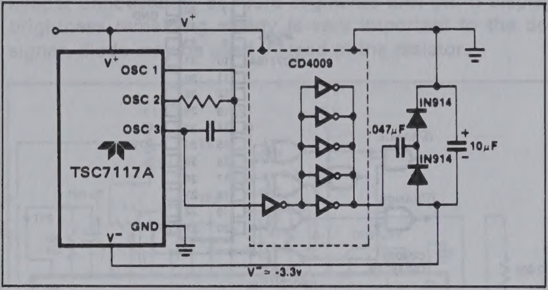


Figure 10: Generating Negative Supply From + 5V

Typical Applications

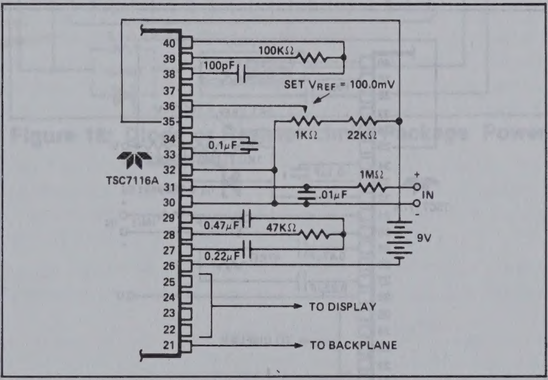


Figure 11: TSC7116A Using the Internal Reference (200 mV Full-Scale, 3 RPS)

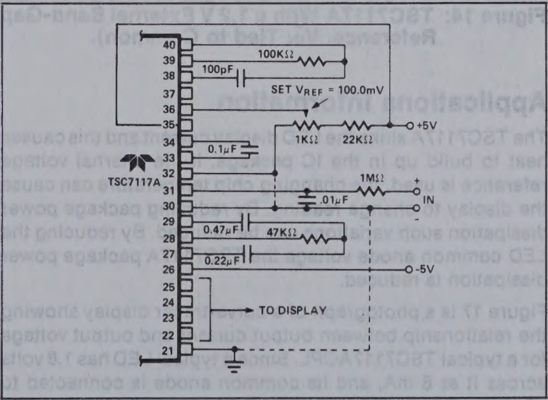


Figure 12: TSC7117A Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN}^{-} Tied to GND for Single Ended Inputs).

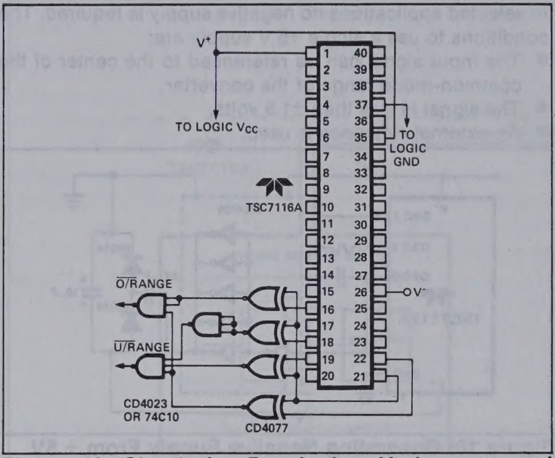

V+
TO LOGIC VCC
TO LOGIC GND
TSC7116A
O/RANGE
U/RANGE
V-
CD4023 OR 74C10
CD4077

Figure 13: Circuit for Developing Underrange and Overrange Signals from TSC7116A Outputs.

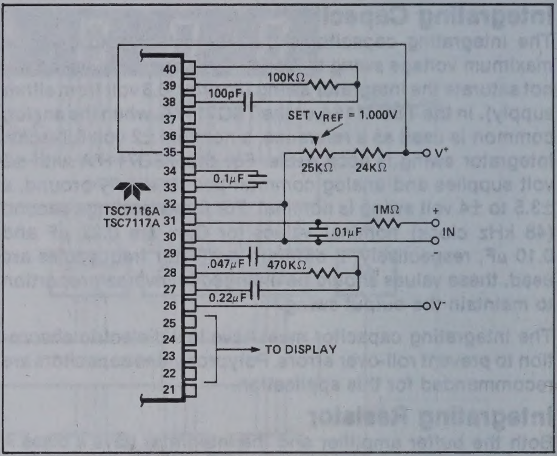

100KΩ
100pF
SET VREF = 1.000V
25KΩ
24KΩ
V+
0.1μF
TSC7116A
TSC7117A
1MΩ
.01μF
IN
.047μF
470KΩ
0.22μF
V-
TO DISPLAY

Figure 15: TSC7116A/TSC7117A: Recommended Component Values for 2.00 V Full-Scale.

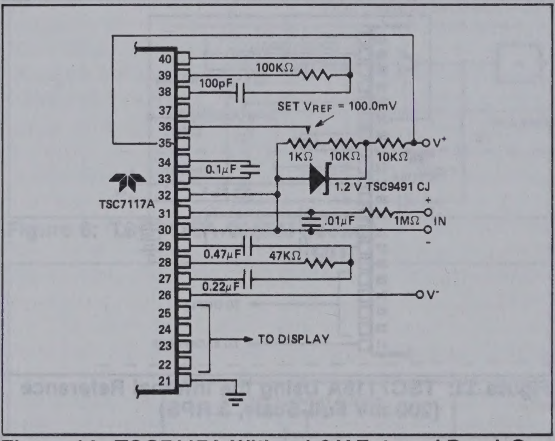

100KΩ
100pF
SET VREF = 100.0mV
1KΩ
10KΩ
10KΩ
V+
0.1μF
1.2 V TSC9491 CJ
TSC7117A
.01μF
1MΩ
IN
0.47μF
47KΩ
0.22μF
V-
TO DISPLAY

Figure 14: TSC7117A With a 1.2 V External Band-Gap Reference. VIN Tied to Common).

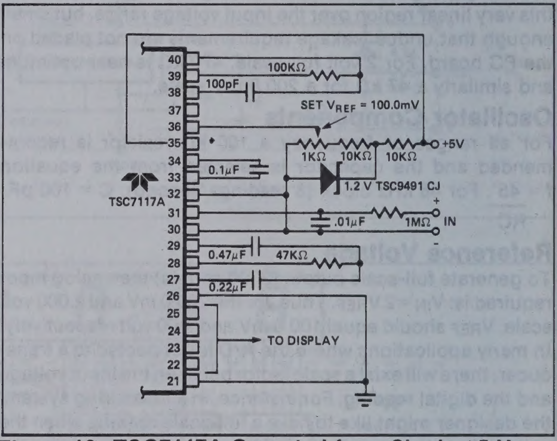

100KΩ
100pF
SET VREF = 100.0mV
1KΩ
10KΩ
10KΩ
+5V
0.1μF
1.2 V TSC9491 CJ
TSC7117A
.01μF
1MΩ
IN
0.47μF
47KΩ
0.22μF
TO DISPLAY

Figure 16: TSC7117A Operated from Single +5 V Supply. An External Reference Must Be Used in This Application.

Applications Information

The TSC7117A sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TSC7117A package power dissipation is reduced.

Figure 17 is a photograph of a curve-tracer display showing the relationship between output current and output voltage for a typical TSC7117ACPL. Since a typical LED has 1.8 volts across it at 8 mA, and its common anode is connected to +5 V, the TSC7117A output is at 3.2 V (point A on Fig. 17). Maximum power dissipation is 8.1 mA X 3.2 V X 24 segments = 622 mW.

Notice, however, that once the TSC7117A output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B of Figure 17) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is now only 7.7 mA X 2.5 V X 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA X 2.2 V X 24 = 385 mW).

Reduced power dissipation is very easy to obtain. Fig. 18 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TSC7117). The resistor will reduce the TSC7117A output voltage, when all 24 segments are "ON," to point "C" of Fig.

17. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor circuit will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, diode may be used instead of the resistor.

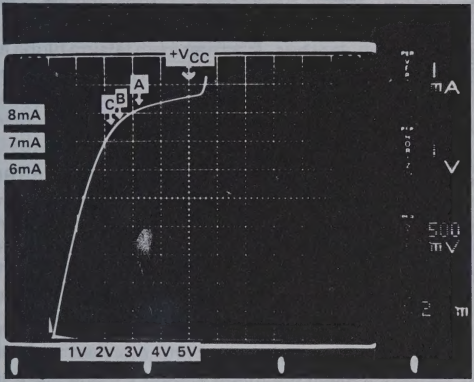


Figure 17: TSC7117A Output Current vs. Output Voltage

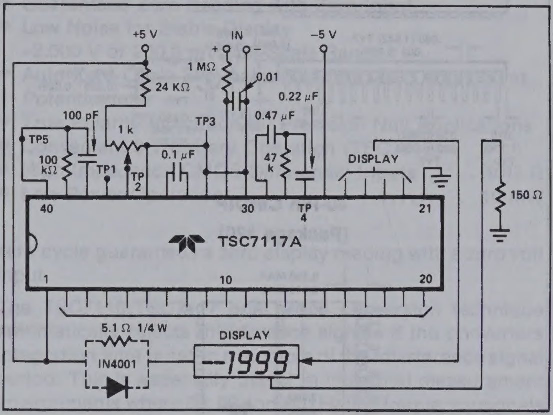
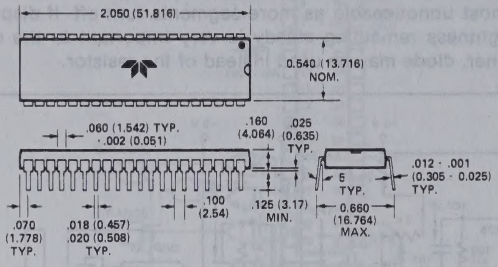

+5 V
IN
+
−
−5 V
1 MΩ
24 KΩ
0.01
0.22 μF
100 pF
0.47 μF
TP3
1 k
TP5
100 kΩ
TP1
TP 2
0.1 μF
47 k
DISPLAY
150 Ω
40
30
TP 4
21
TSC7117A
1
10
20
5.1 Ω 1/4 W
DISPLAY
IN4001
−1999

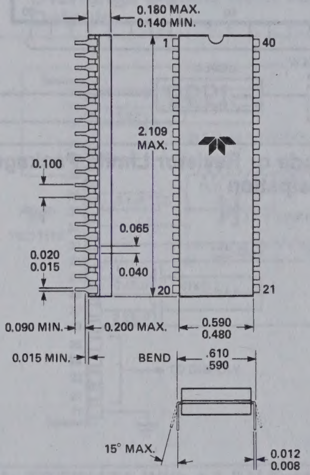
Figure 18: Diode or Resistor Limits Package Power Dissipation

Package Information

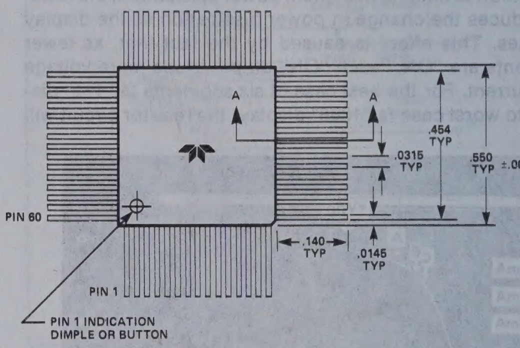
40-Pin Plastic Dual-In-Line Package
(Package #17)


2.050 (51.816)
0.540 (13.716)
NOM.
.060 (1.542) TYP.
.002 (0.051)
.160
(4.064)
.025
(0.635)
TYP.
.012 - .001
(0.305 - 0.025)
TYP.
5
TYP.
.100
(2.54)
.125 (3.17)
MIN.
0.660
(16.764)
MAX.
.070
(1.778)
TYP.
.018 (0.457)
.020 (0.508)
TYP.

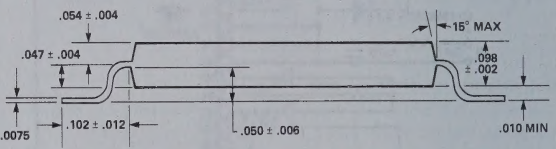
40-Pin CerDIP
(Package #20)


0.180 MAX.
0.140 MIN.
1
40
2.109
MAX.
0.100
0.065
0.020
0.015
0.040
20
21
0.090 MIN.
0.200 MAX.
0.590
0.480
0.015 MIN.
BEND
.610
.590
15° MAX.
0.012
0.008

60-Pin Plastic Flat Package


A
A
.454
TYP
.0315
TYP
.550
TYP ±.005
PIN 60
.140
TYP
.0145
TYP
PIN 1
PIN 1 INDICATION
DIMPLE OR BUTTON

"SQ" Package — Unformed Leads
(Package #22)


.054 ± .004
15° MAX
.047 ± .004
.098
± .002
.0075
.102 ± .012
.050 ± .006
.010 MIN

"BQ" Package — Formed Leads
(Package #21)

TELEDYNE
SEMICONDUCTOR

TSC7116 (LCD Drive)
TSC7117 (LED Drive)
3 1/2 Digit A/D Converter

- **Direct Display Drive**
- **Display Hold Function**

General Description

The TSC7116 and TSC7117 3-1/2 digit CMOS analog-to-digital converters contain all the active components necessary to construct a 0.05% resolution measurement system. Seven segment decoders, polarity and digit drivers, voltage reference and clock circuit are integrated on chip. The TSC7116 drives liquid crystal displays (LCD) and includes a backplane driver. The TSC7117 drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment.

The TSC7116/TSC7117 incorporates the display hold (HLDR) function. the displayed reading will remain indefinitely as long as HLDR is held high. Conversions continue but the output data display latches are not updated. The V_{REF}^- or reference low input is not available as it is with the TSC7106/TSC7107. V_{REF}^- is tied internally to analog common in the TSC7116/TSC7117 devices.

A low cost, high resolution indicating meter requires only a display, four resistors, and four capicitors. The TSC7116 low power drain and 9 V battery operation make it ideal for portable applications.

The TSC7116/TSC7117 reduce linearity error to less than 1 count. Rollover error — the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High impedance differential inputs offer 1 pA leakage current and a 10^{12} Ω input impedance. The 15 μVp-p noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

The TSC7116/TSC7117 dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The TSC7116/TSC7117 are available in a small 60-pin flat package for compact designs. Standard devices are offered in an industrial temperature range and with burn-in lasting for 160 hours at +125°C.

For applications requiring a more temperature stable internal reference voltage refer to the TSC7116A/7107A data sheets.

Features

- Display Hold Function
- Drives LCD or LED Displays Directly
- Guaranteed Zero Reading with Zero Input
- Low Noise for Stable Display
  -2.000 V or 200.0 mV Full-Scale Range
- Auto-Zero Cycle Eliminates Need for Zero Adjustment Potentiometer
- True Polarity Indication for Precision Null Applications
- Convenient 9 V Battery Operation (TSC7116)
- High Impedance CMOS Differential Inputs ..... 10^{12} Ω
- Low Power Operation .... 10 mW

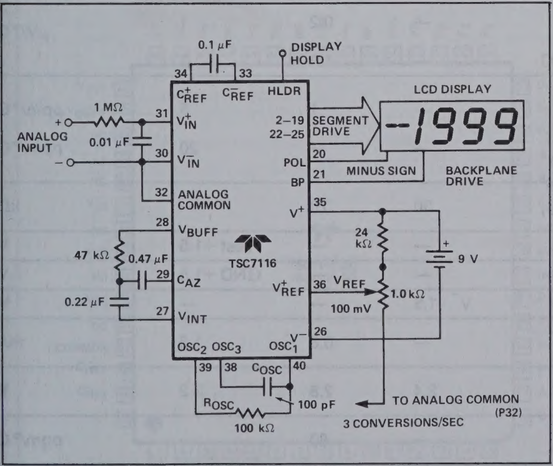

0.1 μF
DISPLAY HOLD
34
33
C_{REF}^+
C_{REF}^-
HLDR
LCD DISPLAY
1 MΩ
+
ANALOG INPUT
0.01 μF
−
31
V_{IN}^+
30
V_{IN}^-
2–19
22–25
SEGMENT DRIVE
-1999
20
POL
21
BP
MINUS SIGN
BACKPLANE DRIVE
32
ANALOG COMMON
35
V^+
28
V_{BUFF}
24 kΩ
+
9 V
47 kΩ
0.47 μF
29
C_{AZ}
TSC7116
0.22 μF
27
V_{INT}
36
V_{REF}^+
V_{REF}
1.0 kΩ
100 mV
26
V^-
OSC_2
OSC_3
OSC_1
39
38
C_{OSC}
40
R_{OSC}
100 kΩ
100 pF
TO ANALOG COMMON (P32)
3 CONVERSIONS/SEC

Figure 1: Typical TSC7116 Operating Circuit

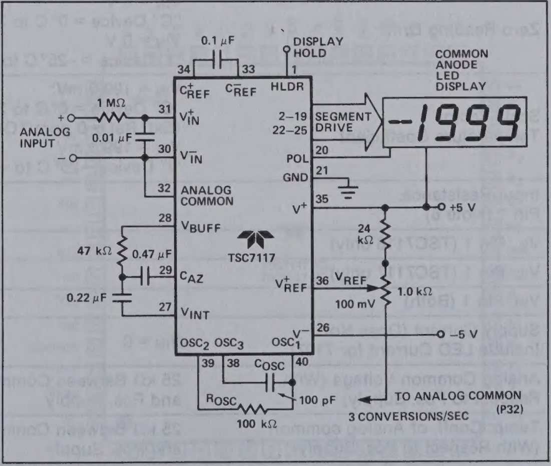

0.1 μF
DISPLAY HOLD
34
33
1
C_{REF}^+
C_{REF}^-
HLDR
COMMON ANODE LED DISPLAY
1 MΩ
+
ANALOG INPUT
0.01 μF
−
31
V_{IN}^+
30
V_{IN}^-
2–19
22–25
SEGMENT DRIVE
-1999
20
POL
21
GND
32
ANALOG COMMON
35
V^+
+5 V
28
V_{BUFF}
24 kΩ
47 kΩ
0.47 μF
29
C_{AZ}
TSC7117
0.22 μF
27
V_{INT}
36
V_{REF}^+
V_{REF}
1.0 kΩ
100 mV
26
V^-
−5 V
OSC_2
OSC_3
OSC_1
39
38
C_{OSC}
40
R_{OSC}
100 kΩ
100 pF
TO ANALOG COMMON (P32)
3 CONVERSIONS/SEC

Figure 2: Typical TSC7117 Operating Circuit

Absolute Maximum Ratings

TSC7116

Supply Voltage (V^+ to V^-)	15 V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	Test to V^+
Power Dissipation (Note 2)	
CerDIP Package	1000 mW
Plastic Package	800 mW
Operating Temperature	
"C" Devices	0° C to +70° C
"I" Devices	-25° C to +85° C
Storage Temperature	-65° C to +160° C
Lead Temperature (Soldering, 60 sec)	300° C

TSC7117

Supply Voltage	
V^+	+6 V
V^-	-9 V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	GND to V^+
Power Dissipation (Note 1)	
CerDIP Package	1000 mW
Plastic Package	800 mW
Operating Temperature	
"C" Devices	0° C to +70° C
"I" Devices	-25° C to +85° C
Storage Temperature	-65° C to +160° C
Lead Temperature (Soldering, 60 sec)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

Electrical Characteristics (Note 3)

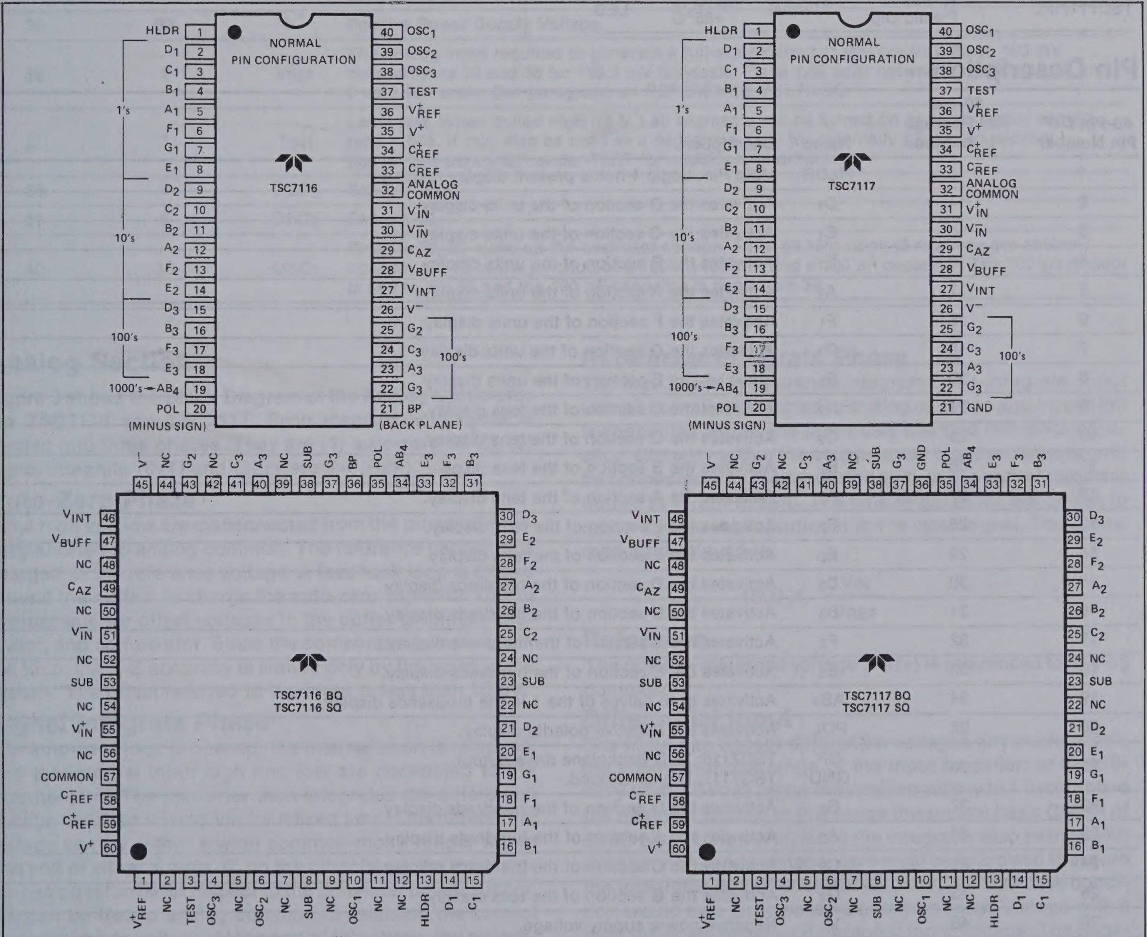
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	$V_{IN} = 0.0$ V Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ $V_{REF} = 100$ mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \simeq 200.0$ mV	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	$V_{CM} = \pm 1$ V, $V_{IN} = 0$ V. Full-Scale = 200.0 mV	—	50	—	μV/V
Noise (Pk - Pk Value Not Exceeded 95% of Time)	$V_{IN} = 0$ V Full-Scale = 200.0 mV	—	15	—	μV
Leakage Current @ Input	$V_{IN} = 0$ V	—	1	10	pA
Zero Reading Drift	$V_{IN} = 0$ V "C" Device = 0° C to 70° C	—	0.2	1	μV/° C
	$V_{IN} = 0$ V "I" Device = -25° C to +85° C	—	1.0	2	
Scale Factor Temperature Coefficient	$V_{IN} = 199.0$ mV, "C" Device = 0° C to 70° C (Ext. Ref = 0 ppm/° C)	—	1	5	ppm/° C
	$V_{IN} = 199.0$ mV "I" Device: -25° C to +85° C	—	—	20	ppm/° C
Input Resistance, Pin 1 (Note 6)		30	70	—	kΩ
V_{IL}, Pin 1 (TSC7116 only)		—	—	Test +1.5	V
V_{IL}, Pin 1 (TSC7117 only)		—	—	GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ -1.5	—	—	V
Supply Current (Does Not Include LED Current for 7107)	$V_{IN} = 0$	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog common (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	—	80	—	ppm/° C
TSC7116 ONLY Pk - Pk Segment Drive Voltage (Note 5)	V^+ to $V^- = 9$ V	4	5	6	V

Electrical Characteristics (Cont.)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
TSC7116 ONLY Pk - Pk Backplane Drive Voltage (Note 5)	V^+ to $V^- = 9$ V	4	5	6	V
TSC7117 ONLY Segment Sinking Current (Except Pin 19)	$V^+ = 5.0$ V Segment Voltage = 3 V	5	8.0	—	mA
TSC7117 ONLY Segment Sinking Current (Pin 19 Only)	$V^+ = 5.0$ V Segment Voltage = 3 V	10	16	—	mA

NOTES:
1. Input voltages may exceed the supply voltages provided the input current is limited to ± 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless other wise noted, specifications apply to both the TSC7116 and TSC7117 at $T_A = 25°C$, $f_{CLOCK} = 48$ kHz. TSC7116 is tested in the circuit of Figure 1. TSC7117 is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average dc component is less than 50 mV.
6. The TSC7116 logic input has an internal pull-down resistor connected from HLDR, Pin 1, to TEST, Pin 37. The TSC7117 logic input has an internal pull-down resistor connected from HLDR, Pin 1 to GROUND, Pin 21.

Pin Configuration


NORMAL PIN CONFIGURATION
TSC7116
HLDR 1
D1 2
C1 3
B1 4
A1 5
F1 6
G1 7
E1 8
D2 9
C2 10
B2 11
A2 12
F2 13
E2 14
D3 15
B3 16
F3 17
E3 18
1000's→AB4 19
POL 20
(MINUS SIGN)
1's
10's
100's
40 OSC1
39 OSC2
38 OSC3
37 TEST
36 V+REF
35 V+
34 C+REF
33 C−REF
32 ANALOG COMMON
31 V+IN
30 V−IN
29 CAZ
28 VBUFF
27 VINT
26 V−
25 G2
24 C3
23 A3
22 G3
21 BP
(BACK PLANE)
100's
NORMAL PIN CONFIGURATION
TSC7117
HLDR 1
D1 2
C1 3
B1 4
A1 5
F1 6
G1 7
E1 8
D2 9
C2 10
B2 11
A2 12
F2 13
E2 14
D3 15
B3 16
F3 17
E3 18
1000's→AB4 19
POL 20
(MINUS SIGN)
1's
10's
100's
40 OSC1
39 OSC2
38 OSC3
37 TEST
36 V+REF
35 V+
34 C+REF
33 C−REF
32 ANALOG COMMON
31 V+IN
30 V−IN
29 CAZ
28 VBUFF
27 VINT
26 V−
25 G2
24 C3
23 A3
22 G3
21 GND
100's
TSC7116 BQ
TSC7116 SQ
V− 45
NC 44
G2 43
NC 42
C3 41
A3 40
NC 39
SUB 38
G3 37
BP 36
POL 35
AB4 34
E3 33
F3 32
B3 31
VINT 46
VBUFF 47
NC 48
CAZ 49
NC 50
V−IN 51
NC 52
SUB 53
NC 54
V+IN 55
NC 56
COMMON 57
C−REF 58
C+REF 59
V+ 60
30 D3
29 E2
28 F2
27 A2
26 B2
25 C2
24 NC
23 SUB
22 NC
21 D2
20 E1
19 G1
18 F1
17 A1
16 B1
1 V+REF
2 NC
3 TEST
4 OSC3
5 NC
6 OSC2
7 NC
8 SUB
9 NC
10 OSC1
11 NC
12 NC
13 HLDR
14 D1
15 C1
TSC7117 BQ
TSC7117 SQ
V− 45
NC 44
G2 43
NC 42
C3 41
A3 40
NC 39
SUB 38
G3 37
GND 36
POL 35
AB4 34
E3 33
F3 32
B3 31
VINT 46
VBUFF 47
NC 48
CAZ 49
NC 50
V−IN 51
NC 52
SUB 53
NC 54
V+IN 55
NC 56
COMMON 57
C−REF 58
C+REF 59
V+ 60
30 D3
29 E2
28 F2
27 A2
26 B2
25 C2
24 NC
23 SUB
22 NC
21 D2
20 E1
19 G1
18 F1
17 A1
16 B1
1 V+REF
2 NC
3 TEST
4 OSC3
5 NC
6 OSC2
7 NC
8 SUB
9 NC
10 OSC1
11 NC
12 NC
13 HLDR
14 D1
15 C1

Notes:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7116CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7116IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LCD
TSC7116CJL	40-Pin CerDIP	Normal	0°C to +70°C	LCD
TSC7116IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7116CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TSC7116CSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LCD
TSC7117CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7117IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LED

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7117CJL	40-Pin CerDIP	Normal	0°C to +70°C	LED
TSC7117IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LED
TSC7117CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TSC7117CSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LED
Devices with Burn-In (160 Hours at +125°C)				
TSC7116CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7117CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LED

Pin Description

40-Pin DIP Pin Number	60-Pin Flat Package Pin Number	Name	Description
1	13	HLDR	Hold Pin, Logic 1 holds present display reading.
2	14	D_1	Activates the D section of the units display.
3	15	C_1	Activates the C section of the units display.
4	16	B_1	Activates the B section of the units display.
5	17	A_1	Activates the A section of the units display.
6	18	F_1	Activates the F section of the units display.
7	19	G_1	Activates the G section of the units display.
8	20	E_1	Activates the E section of the units display.
9	21	D_2	Activates the D section of the tens display.
10	25	C_2	Activates the C section of the tens display.
11	26	B_2	Activates the B section of the tens display.
12	27	A_2	Activates the A section of the tens display.
13	28	F_2	Activates the F section of the tens display.
14	29	E_2	Activates the E section of the tens display.
15	30	D_3	Activates the D section of the hundreds display.
16	31	B_3	Activates the B section of the hundreds display.
17	32	F_3	Activates the F section of the hundreds display.
18	33	E_3	Activates the E section of the hundreds display.
19	34	AB_4	Activates both halves of the 1 in the thousands display.
20	35	POL	Activates the negative polarity display.
21	36	BP GND	TSC7116: LCD Backplane drive output. TSC7117: Digital Ground.
22	37	G_3	Activates the G section of the hundreds display.
23	40	A_3	Activates the A section of the hundreds display.
24	41	C_3	Activates the C section of the hundreds display.
25	43	G_2	Activates the G section of the tens display.
26	45	V^-	Negative power supply voltage.
27	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for additional details.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	60-Pin Flat Package Pin Number	Name	Description
28	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ for a 200 mV full-scale range and a 470 kΩ for 2 V full-scale range.
29	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for a 200 mV full-scale, and a 0.047 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	51	V_{IN}^-	The analog low input is connected to this pin.
31	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	58	C_{REF}^-	See pin 34.
34	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	60	V^+	Positive Power Supply Voltage.
36	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 32 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 32 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read −1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	4	OSC_3	See pin 40.
39	6	OSC_2	See pin 40.
40	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the TSC7116 and TSC7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) reference (REF).

Auto-Zero Phase

Input high and low are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

Signal Integrate Phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between V_{IN}^+ and V_{IN}^- for a fixed time. This differential voltage can be within a wide common-mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, V_{IN}^- can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Reference Integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is:

$$1000\ X\ \frac{V_{IN}}{V_{REF}}$$

Reference

The positive reference voltage (V_{REF}^+) is referenced to analog common.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of

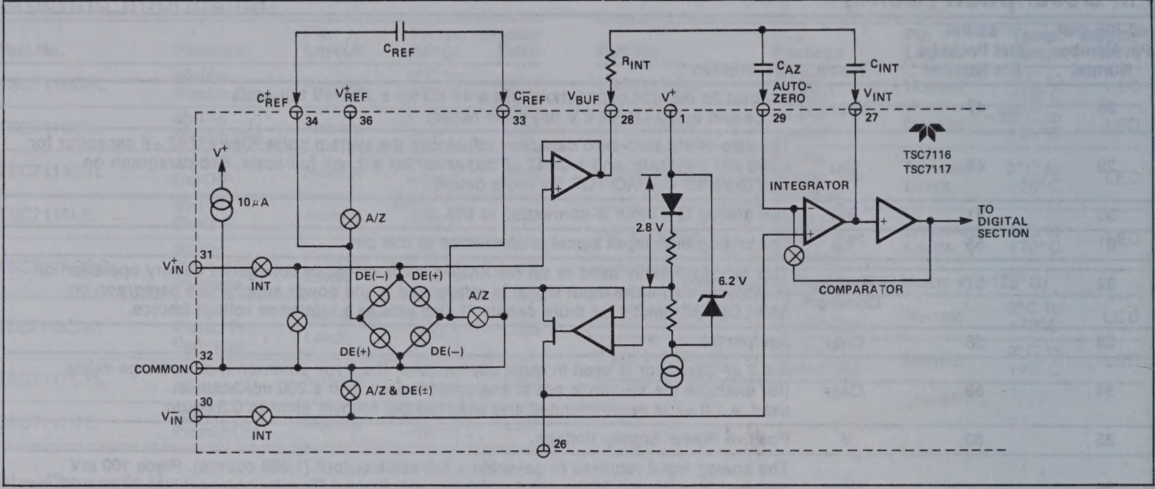


Figure 3: Analog Section of TSC7116/TSC7117

its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2 V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation (TSC7116) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6 V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7 V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈15 Ω), and a temperature coefficient of 80 ppm/° C typically.

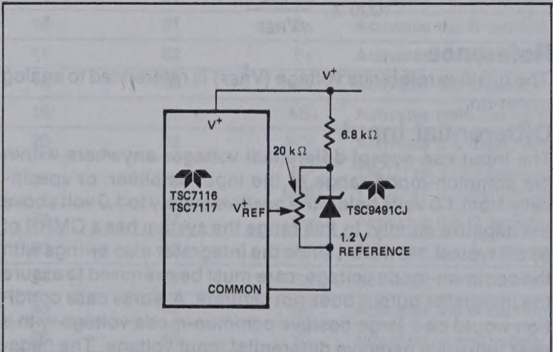


Figure 4: Using an External Reference

An external reference may be added to improve temperature stability or the TSC7116A/TSC7117A devices with lower analog common temperature drift may be used. The circuit is shown in Figure 4.

Analog common is also used as the V_{IN}^- return during auto-zero and deintegrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications V_{IN}^- will be set at a fixed known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog common, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET that can sink 30 mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10 µA of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. On the TSC7117 it is coupled to the internally generated digital supply through a 500 Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read −1888. The TEST pin will sink about 10 mA under these conditions.

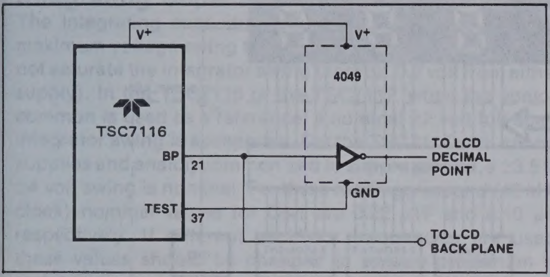


Figure 5: Simple Inverter for Fixed Decimal Point

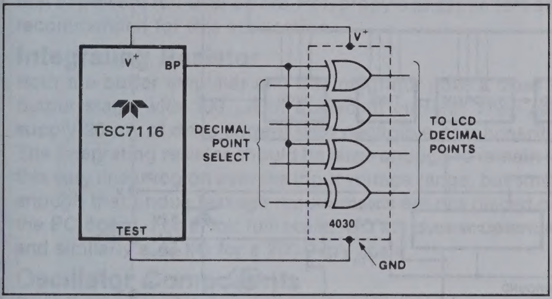


Figure 6: Exclusive "OR" Gate for Decimal Point Drive

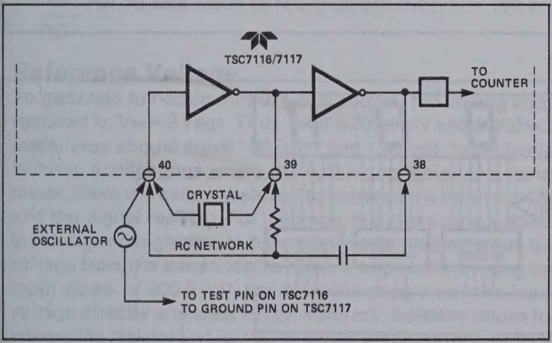


Figure 7: Clock Circuits

Digital Section

Figures 8 and 9 show the digital section for the TSC7116 and TSC7117, respectively. In the TSC7116 (Figure 8), an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible dc voltage exists across the segments.

Figure 9 is the Digital Section of the TSC7117. It is identical to the TSC7116 except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TSC7117 is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

System Timing

Figure 9 shows the clocking method used in the TSC7116 and TSC7117. Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full-scale auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

HOLD Reading Input

When HLDR is at a logic "HI" the latch will not be updated. A/D conversions will continue but will not be updated until the HLDR is returned to "LOW". To continuously update the display connect to TEST (TSC7116) or GROUND (TSC7117) or disconnect. This input is CMOS compatible with 70K typical resistance to TEST (TSC7116) or GROUND (TSC7117).

Component Value Selection

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full-scale where noise is very important, a 0.47 μF capacitor is recommended. On the 2 volt scale, a 0.047 μF capacitor increase the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common-mode voltage exists (i.e. the V_{IN}^- pin is not at analog common) and a 200 mV scale is used, a large value is required to prevent to roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

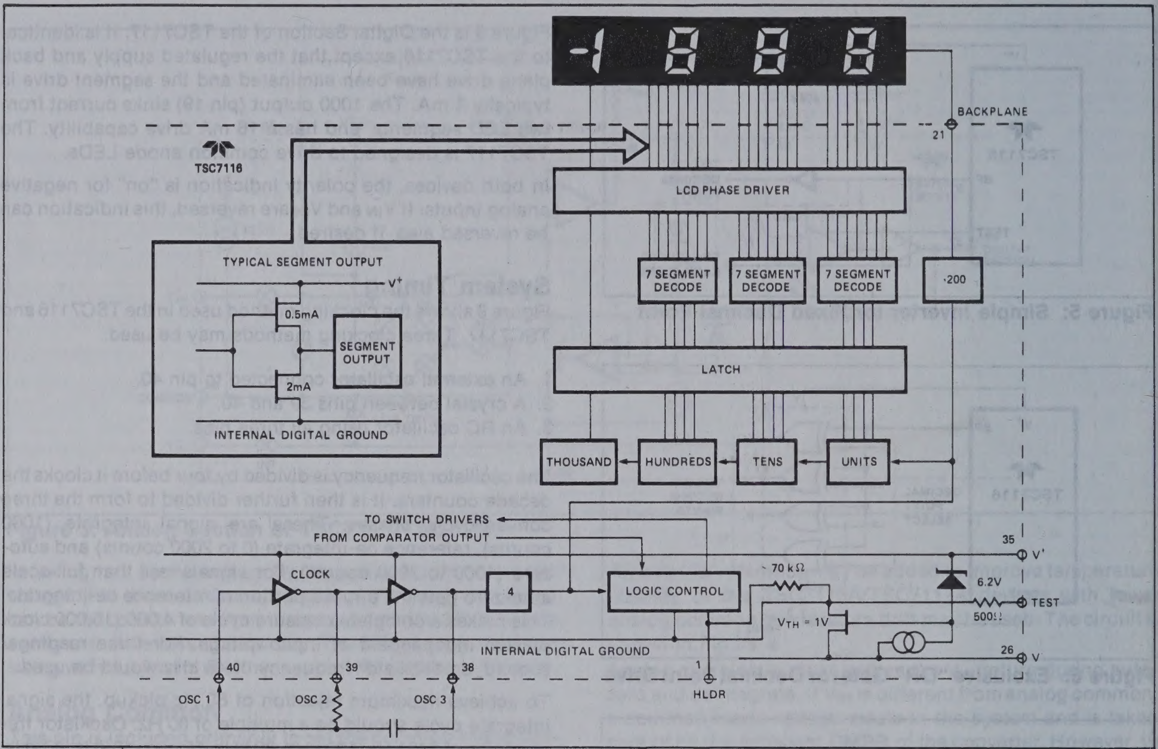

TSC7116
BACKPLANE
21
LCD PHASE DRIVER
TYPICAL SEGMENT OUTPUT
V+
0.5mA
SEGMENT OUTPUT
2mA
INTERNAL DIGITAL GROUND
7 SEGMENT DECODE
7 SEGMENT DECODE
7 SEGMENT DECODE
÷200
LATCH
THOUSAND
HUNDREDS
TENS
UNITS
TO SWITCH DRIVERS
FROM COMPARATOR OUTPUT
CLOCK
4
LOGIC CONTROL
70 kΩ
35
V+
6.2V
500Ω
TEST
VTH = 1V
26
V-
INTERNAL DIGITAL GROUND
40
39
38
1
OSC 1
OSC 2
OSC 3
HLDR

Figure 8: TSC7116 Digital Section

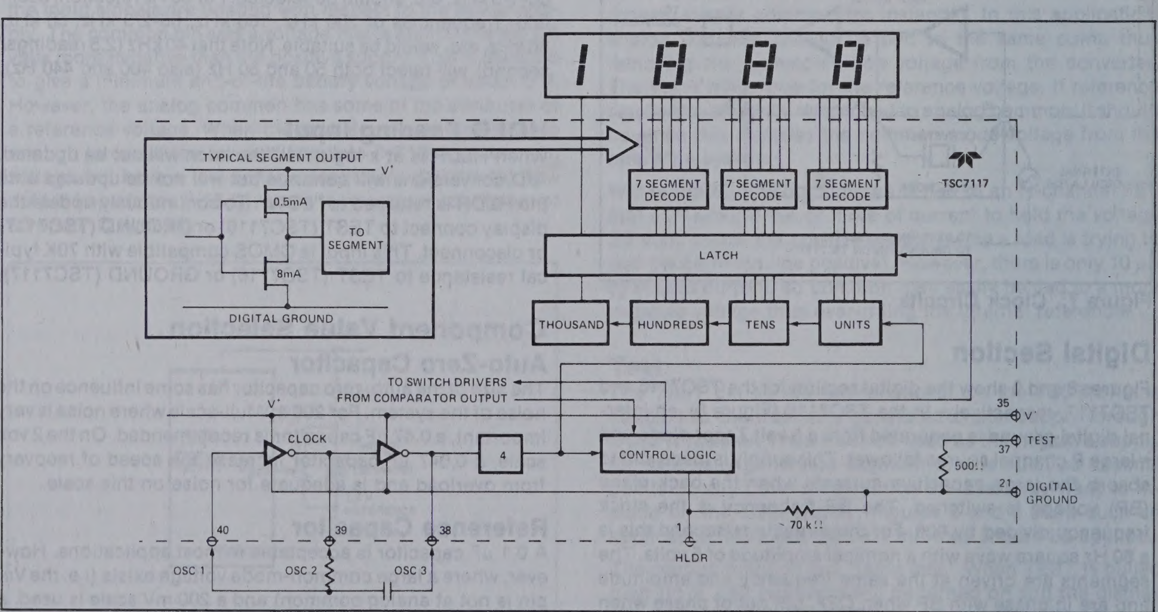

TYPICAL SEGMENT OUTPUT
V+
0.5mA
TO SEGMENT
8mA
DIGITAL GROUND
7 SEGMENT DECODE
7 SEGMENT DECODE
7 SEGMENT DECODE
TSC7117
LATCH
THOUSAND
HUNDREDS
TENS
UNITS
TO SWITCH DRIVERS
FROM COMPARATOR OUTPUT
V+
CLOCK
4
CONTROL LOGIC
35
V+
37
TEST
500Ω
21
DIGITAL GROUND
~70 kΩ
1
HLDR
40
39
38
OSC 1
OSC 2
OSC 3

Figure 9: TSC7117 Digital Section

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the TSC7116 or the TSC7117, when the analog common is used as a reference, a nominal ±2 volt full-scale integrator swing is acceptable. For the TSC7117 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48 kHz clock) nominal values for C_{INT} are 0.22 μ1F and 0.10 μF, respectively. If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. They can supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full-scale, 470 kΩ is near optimum and similarly a 47 kΩ for a 200.0 mV scale.

Oscillator Components

For all ranges of frequency a 100 kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$. For 48 kHz clock (3 readings/second), C = 100 pF.

Reference Voltage

To generate full-scale output (2000 counts) the analog input required is: $V_{IN} = 2 V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.00 volt respectively. In many applications where the A/D is connected to a transducer, there will exist a scale factor between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage from the transducer is 700 mV. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select $V_{REF} = 350$ mV. Suitable values for integrating resistor and capacitor would be 120 kΩ and 0.22 μF. This makes the system slightly quieter and also avoids a divider network on the input. The TSC7117 with ±5 V supplies can accept input signals up to ±4 V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between V_{IN}^{+} and common and the variable (or fixed) offset voltage between common and V_{IN}^{-}.

TSC7117 Power Supplies

The TSC7117 is designed to work from ±5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors and an inexpensive IC. Figure 10 shows this application.

In selected applications no negative supply is required. The conditions to use a single +5 V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5 volts.
- An external reference is used.

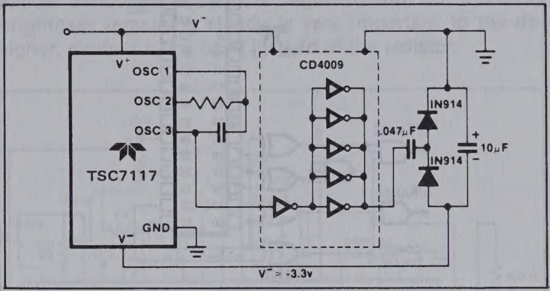


Figure 10: Generating Negative Supply From + 5V

Typical Applications

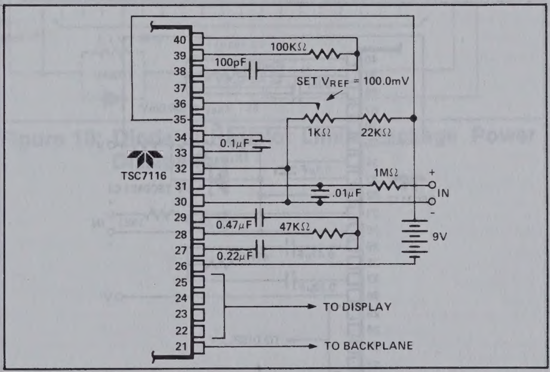


Figure 11: TSC7116 Using the Internal Reference (200 mV Full-Scale, 3 RPS)

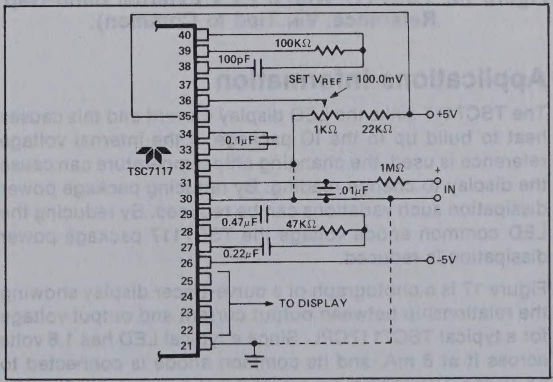


Figure 12: TSC7117 Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN}^{-} Tied to GND for Single Ended Inputs).

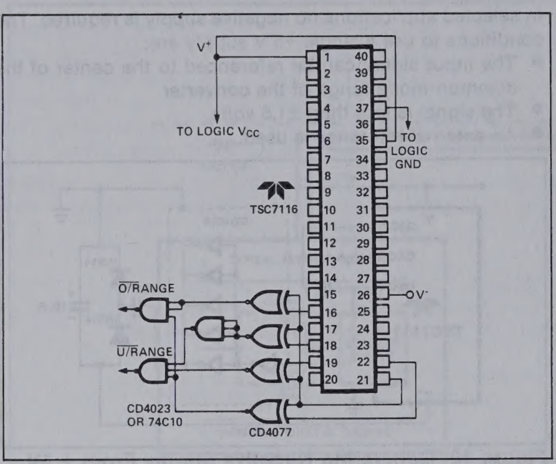

V+
TO LOGIC VCC
TO LOGIC GND
TSC7116
O/RANGE
U/RANGE
V-
CD4023 OR 74C10
CD4077

Figure 13: Circuit for Developing Underrange and Overrange Signals from TSC7116 Outputs.

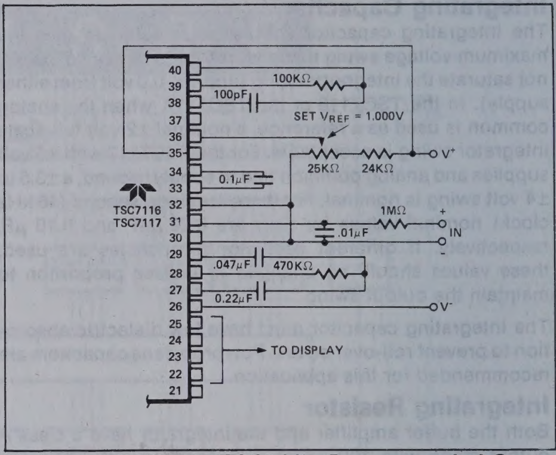

100KΩ
100pF
SET V_{REF} = 1.000V
25KΩ
24KΩ
V+
0.1µF
TSC7116
TSC7117
1MΩ
+
IN
-
.01µF
.047µF
470KΩ
0.22µF
V-
TO DISPLAY

Figure 15: TSC7116/TSC7117: Recommended Component Values for 2.00 V Full-Scale.

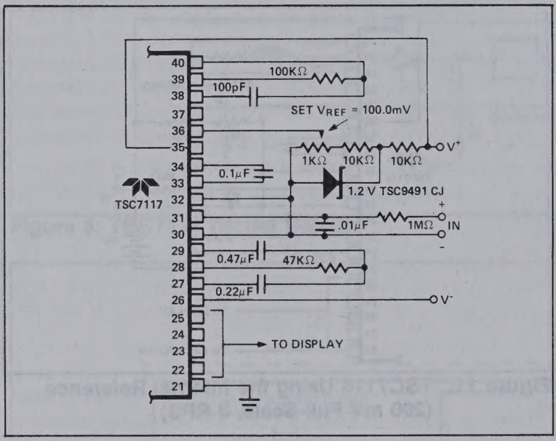

100KΩ
100pF
SET V_{REF} = 100.0mV
1KΩ
10KΩ
10KΩ
V+
0.1µF
1.2 V TSC9491 CJ
TSC7117
.01µF
1MΩ
+
IN
-
0.47µF
47KΩ
0.22µF
V-
TO DISPLAY

Figure 14: TSC7117 With a 1.2 V External Band-Gap Reference. V_{IN} Tied to Common).

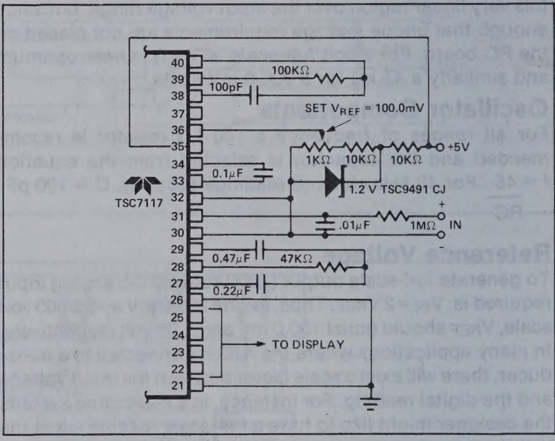

100KΩ
100pF
SET V_{REF} = 100.0mV
1KΩ
10KΩ
10KΩ
+5V
0.1µF
1.2 V TSC9491 CJ
TSC7117
.01µF
1MΩ
+
IN
-
0.47µF
47KΩ
0.22µF
TO DISPLAY

Figure 16: TSC7117 Operated from Single +5 V Supply. An External Reference Must Be Used in This Application.

Applications Information

The TSC7117 sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TSC7117 package power dissipation is reduced.

Figure 17 is a photograph of a curve-tracer display showing the relationship between output current and output voltage for a typical TSC7117CPL. Since a typical LED has 1.8 volts across it at 8 mA, and its common anode is connected to +5 V, the TSC7117 output is at 3.2 V (point A on Fig. 17). Maximum power dissipation is 8.1 mA X 3.2 V X 24 segments = 622 mW.

Notice, however, that once the TSC7117 output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B of Figure 17) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is now only 7.7 mA X 2.5 V X 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA X 2.2 V X 24 = 385 mW).

Reduced power dissipation is very easy to obtain. Fig. 18 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TSC7117). The resistor will reduce the TSC7117 output voltage, when all 24 segments are "ON," to point "C" of Fig.

17. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor circuit will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, diode may be used instead of the resistor.

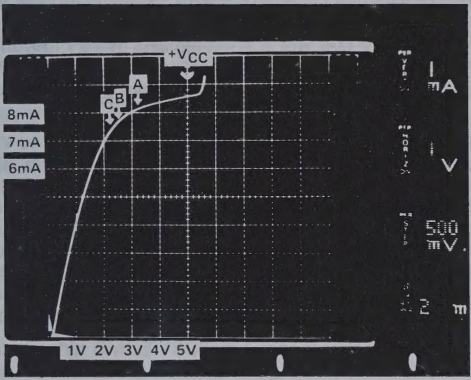


Figure 17: TSC7117 Output Current vs Output Voltage

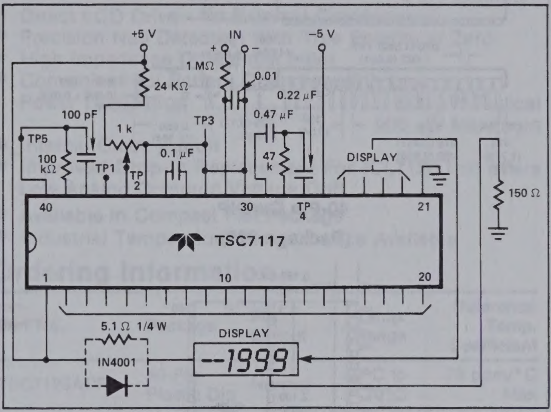
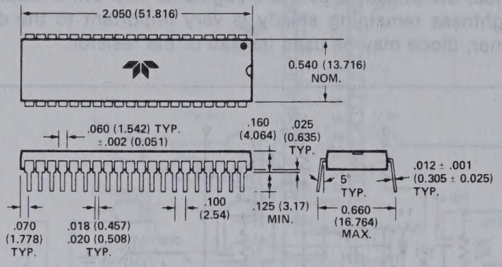

+5 V
IN
+
−
−5 V
1 MΩ
24 KΩ
0.01
0.22 μF
100 pF
0.47 μF
TP3
1 k
TP5
100 kΩ
TP1
TP 2
0.1 μF
47 k
DISPLAY
150 Ω
40
30
TP 4
21
TSC7117
1
10
20
5.1 Ω 1/4 W
IN4001
DISPLAY
--1999

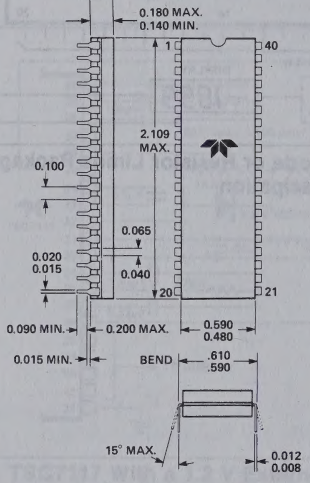
Figure 18: Diode or Resistor Limits Package Power Dissipation

Package Information

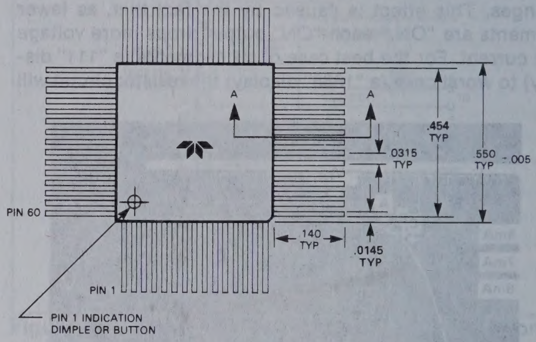
40-Pin Plastic Dual-In-Line Package
(Package #17)


2.050 (51.816)
0.540 (13.716) NOM.
.060 (1.542) TYP. ±.002 (0.051)
.160 (4.064)
.025 (0.635) TYP.
5° TYP.
.012 ± .001 (0.305 ± 0.025) TYP.
.070 (1.778) TYP.
.018 (0.457) .020 (0.508) TYP.
.100 (2.54)
.125 (3.17) MIN.
0.660 (16.764) MAX.

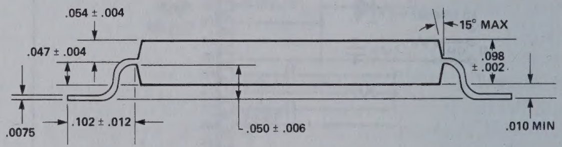
40-Pin CerDIP
(Package #20)


0.180 MAX.
0.140 MIN.
1
40
2.109 MAX.
0.100
0.065
0.020
0.015
0.040
20
21
0.090 MIN.
0.200 MAX.
0.590
0.480
0.015 MIN.
BEND
.610
.590
15° MAX.
0.012
0.008

60-Pin Plastic Flat Package


A
A
.454 TYP
.0315 TYP
.550 TYP ± .005
PIN 60
.140 TYP
.0145 TYP
PIN 1
PIN 1 INDICATION DIMPLE OR BUTTON

"SQ" Package — Unformed Leads
(Package #22)


.054 ± .004
15° MAX
.047 ± .004
.098 ± .002
.0075
.102 ± .012
.050 ± .006
.010 MIN

"BQ" Package — Formed Leads
(Package #21)

TELEDYNE SEMICONDUCTOR

TSC7126A

3 1/2 Digit A/D Converter

- **Low Power Dissipation - 900 μW Max.**
- **35 ppm/°C Internal Reference**

General Description

The TSC7126A is a low power 3 1/2 Digit LCD display analog to digital converter that allows existing 7126 based systems to be upgraded. An improved internal zener reference voltage circuit maintains the analog common temperature drift to 35 ppm/°C typically. A 75 ppm/°C maximum limit is guaranteed. This represents a 2 to 4 times improvement over similar 3 1/2 digit converters.

Existing TSC7126 or ICL7126 based systems may be upgraded without changing external passive component values. The costly, space consuming external reference source may be removed. Power dissipation is a low 900 μW maximum. Long battery life is guaranteed; a key design consideration in portable or battery back-up systems.

The TSC7126A limits linearity error to less than 1 count on 200 mV or 2.00 V full-scale ranges. Rollover error - the difference in readings for equal magnitude but opposite polarity input signals - is below ±1 count. High impedance differential inputs offer 1 pA leakage currents and a 10^{12} Ω input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μV_{p-p} noise performance guarantees a "rock solid" reading. The auto zero cycle guarantees a zero display readout for a zero volt input.

The single chip CMOS TSC7126A incorporates all the active devices for a 3 1/2 digit analog to digital converter to directly drive an LCD display. The internal oscillator, precision voltage reference and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution -0.05% - indicating meter requires only a display, four resistors, four capacitors and a 9 V battery. The flat package option eases the mechanical design of low cost, hand held multimeters.

The TSC7126A dual slope conversion technique rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

Typical Applications

- Thermometry
- Bridge Readouts (Strain Gauges, Load Cells, Null Detectors)
- Digital Meters
  - Voltage/Current/Ohms/Power
  - pH
  - Capacitance/Inductance
  - Fluid Flow Rate/Viscosity/Level
  - Humidity
  - Position
- Digital Scales
- Panel Meters
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Gaussometers
- Photometers

Features

- Internal Reference With Low Temperature Drift .... 35 ppm/°C Typical
75 ppm/°C Maximum
- Guaranteed Zero Reading With Zero Input
- Low Noise .... 15 μV_{p-p}
- High Resolution (0.05%) and Wide Dynamic Range (72 dB)
- Low Input Leakage Current .... 1 pA Typical
10 pA Maximum
- Direct LCD Drive - No External Components.
- Precision Null Detection With True Polarity at Zero
- High Impedance Differential Input
- Convenient 9 V Battery Operation With Low Power Dissipation .... 500 μW Typical
900 μW Maximum
- Internal Clock Circuit
- Improved Drop-In Replacement For ICL7126 that offers Low Analog Common Voltage Drift
- Available in Compact Flat Package
- Industrial Temperature Range Device Available

Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Reference Temp. Coefficient
TSC7126ACPL	40-Pin Plastic Dip	Normal	0°C to 70°C	75 ppm/°C Max
TSC7126ARCPL	40-Pin Plastic Dip	Reversed	0°C to 70°C	75 ppm/°C Max
TSC7126AIJL	40-Pin CerDIP	Normal	-25°C to +85°C	100 ppm/°C Max
TSC7126ACBQ	60-Pin Plastic Flat	Formed Leads	0°C to 70°C	75 ppm/°C Max
TSC7126ACSQ	60-Pin Plastic Flat	Unformed Leads	0°C to 70°C	75 ppm/°C Max
Devices with 160 Hour, +125°C Burn-In				
TSC7126ACPL/BI	40-Pin Plastic Dip	Normal	0°C to 70°C	75 ppm/°C Max
TSC7126AIJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C	100 ppm/°C Max

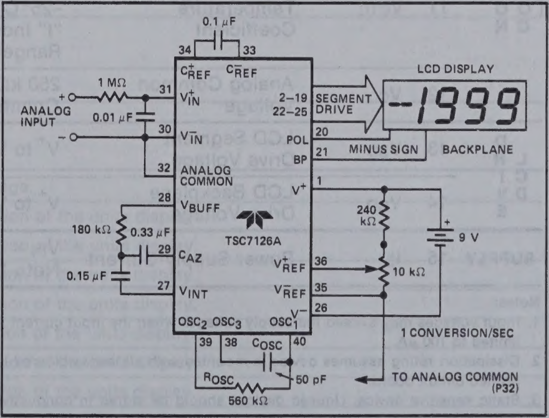


Figure 1: Typical Operating Circuit

© 1983

3 1/2 Digit A/D Converter

• Low Power Dissipation - 900 μW Max.
• 35 ppm/°C Internal Reference

TSC7126A

Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) .... 15 V
Analog Input Voltage (either input)$^{(1)}$ .... V^+ to V^-
Reference Input Voltage (either input) .... V^+ to V^-
Clock Input .... Test to V^+
Power Dissipation $^{(2)}$
CerDIP Package (J) .... 1000 mW
Plastic Package (P) .... 800 mW
Epoxy Flat Package (B, S) .... 500 mW
Operating Temperature
("C" Devices) .... 0°C to +70°C
("I" Devices) .... -25°C to +85°C
Storage Temperature .... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) .... 300°C

Electrical Characteristics: V_S = 9 V, f_{clock} = 16 kHz and T_A = 25°C unless otherwise noted.

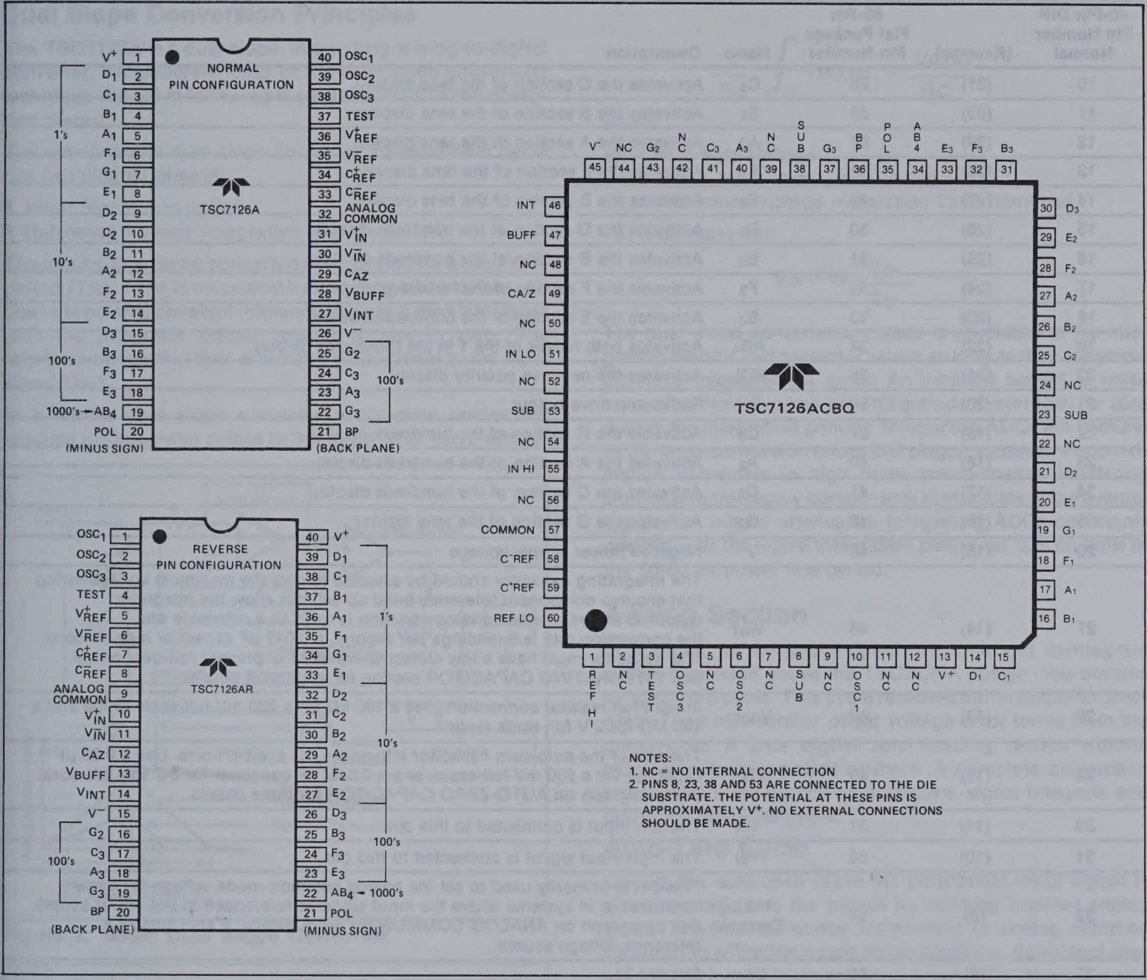
TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7126A MIN	TSC7126A TYP	TSC7126A MAX	UNIT
INPUT	1	—	Zero Input Reading	V_{IN} = 0.0 V, Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
	2	—	Zero Reading Drift	V_{IN} = 0.0 V, 0°C ≤ T_A ≤ 70°C	—	0.2	1	μV/°C
	3	—	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100 mV	999	999 1000	1000	Digital Reading
	4	NL	Linearity Error	Full-Scale = 200 mV or 2.000 V. Max. Deviation from Best Straight Line.	-1	±0.2	+1	Counts
	5	—	Rollover Error	$-V_{IN}$ = $+V_{IN}$ ≈ 200.0 mV	-1	±0.2	+1	Counts
	6	E_N	Noise	V_{IN} = 0 V, Full-Scale = 200.0 mV	—	15	—	μV_{p-p}
	7	I_L	Input Leakage Current	V_{IN} = 0 V	—	1	10	pA
	8	CMRR	Common-Mode Rejection Ratio	V_{CM} = ±1 V, V_{IN} = 0 V Full-Scale = 200.0 mV	—	50	—	μV/V
	9	—	Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, 0°C ≤ T_A ≤ 70°C Ext. Ref. Temp. Coeff. = 0 ppm/°C	—	1	5	ppm/°C
ANALOG COMMON	10	V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Commom and V^+ 0°C ≤ T_A ≤ 70°C "C" Commercial Temp. Range Devices	—	35	75	ppm/°C
	11	V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ -25°C ≤ T_A ≤ 85°C "I" Industrial Temp. Range Devices	—	35	100	ppm/°C
	12	V_C	Analog Common Voltage	250 kΩ Between Common and V^+	2.7	3.05	3.35	V
LCD DRIVE	13	V_{SD}	LCD Segment Drive Voltage	V^+ to V^- = 9 V	4	5	6	V_{p-p}
	14	V_{BD}	LCD Backplane Drive Voltage	V^+ to V^- = 9 V	4	5	6	V_{p-p}
SUPPLY	15	I_S	Power Supply Current	V_{IN} = 0 V, V^+ to V^- = 9 V, Note 7	—	55	100	μA

Notes:

1. Input voltages may exceed the supply voltages when the input current is limited to 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Static sensitive device. Unused devices should be stored in conductive material to protect devices from static discharge and static fields.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment and 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
6. See Figure 1.
7. During auto-zero phase, current is 10-20 μA higher. A 48 kHz oscillator increases current by 8 μA (typ.). Common current not included.

3 1/2 Digit A/D Converter
- **Low Power Dissipation - 900 μW Max.**
- **35 ppm/°C Internal Reference**

Pin Configuration


NORMAL PIN CONFIGURATION
TSC7126A
V^+ 1, D_1 2, C_1 3, B_1 4, A_1 5, F_1 6, G_1 7, E_1 8, D_2 9, C_2 10, B_2 11, A_2 12, F_2 13, E_2 14, D_3 15, B_3 16, F_3 17, E_3 18, AB_4 19, POL 20
40 OSC_1, 39 OSC_2, 38 OSC_3, 37 TEST, 36 V^+_{REF}, 35 V^-_{REF}, 34 C^+_{REF}, 33 C^-_{REF}, 32 ANALOG COMMON, 31 V^+_{IN}, 30 V^-_{IN}, 29 C_{AZ}, 28 V_{BUFF}, 27 V_{INT}, 26 V^-, 25 G_2, 24 C_3, 23 A_3, 22 G_3, 21 BP
1's
10's
100's
1000's
100's
(MINUS SIGN)
(BACK PLANE)
REVERSE PIN CONFIGURATION
TSC7126AR
OSC_1 1, OSC_2 2, OSC_3 3, TEST 4, V^+_{REF} 5, V^-_{REF} 6, C^+_{REF} 7, C^-_{REF} 8, ANALOG COMMON 9, V^+_{IN} 10, V^-_{IN} 11, C_{AZ} 12, V_{BUFF} 13, V_{INT} 14, V^- 15, G_2 16, C_3 17, A_3 18, G_3 19, BP 20
40 V^+, 39 D_1, 38 C_1, 37 B_1, 36 A_1, 35 F_1, 34 G_1, 33 E_1, 32 D_2, 31 C_2, 30 B_2, 29 A_2, 28 F_2, 27 E_2, 26 D_3, 25 B_3, 24 F_3, 23 E_3, 22 AB_4, 21 POL
1's
10's
100's
100's
1000's
(BACK PLANE)
(MINUS SIGN)
TSC7126ACBQ
45 V^-, 44 NC, 43 G_2, 42 NC, 41 C_3, 40 A_3, 39 NC, 38 SUB, 37 G_3, 36 BP, 35 POL, 34 AB4, 33 E_3, 32 F_3, 31 B_3
30 D_3, 29 E_2, 28 F_2, 27 A_2, 26 B_2, 25 C_2, 24 NC, 23 SUB, 22 NC, 21 D_2, 20 E_1, 19 G_1, 18 F_1, 17 A_1, 16 B_1
1 REF H, 2 NC, 3 TEST, 4 OSC3, 5 NC, 6 OSC2, 7 NC, 8 SUB, 9 NC, 10 OSC1, 11 NC, 12 NC, 13 V^+, 14 D_1, 15 C_1
46 INT, 47 BUFF, 48 NC, 49 CA/Z, 50 NC, 51 IN LO, 52 NC, 53 SUB, 54 NC, 55 IN HI, 56 NC, 57 COMMON, 58 C^-REF, 59 C^+REF, 60 REF LO

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.
9	(32)	21	D_2	Activates the D section of the tens display.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP	Backplane drive output.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 μF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See INTEGRATING CAPACITOR section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 180 kΩ for a 200 mV full-scale range and a 180 MΩ for 2 V full scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.33 μF capacitor for a 200 mV full-scale, and a 0.033 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The low input is connected to this pin.
31	(10)	55	V_{IN}^+	The high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.
34	(7)	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common mode voltage exists (for example the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.
36	(5)	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38.

General Theory of Operation

Dual Slope Conversion Principles

The TSC7126A is a dual slope, integrating analog-to-digital converter. An understanding of the dual slope conversion technique will aid in following the detailed TSC7126A operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}).

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

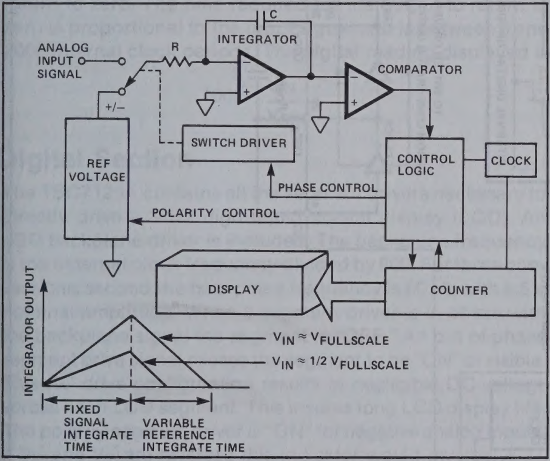


Figure 2: Basic Dual Slope Converter

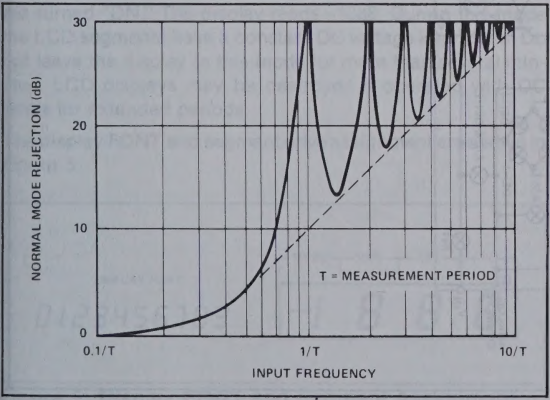


Figure 3: Normal-Mode Rejection of Dual Slope Converter

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_{0}^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage
T_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period.

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed above the TSC7126A design incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference integrate cycle.

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero cycle residual is typically 10 –15 μV.

The auto-zero cycle length is 1000 to 3000 clock periods.

Signal Integration Cycle

The auto-zero loop is opened and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is integrated for a fixed time period. The TSC7126A signal integration period is 1000 clock periods or counts. The externally set clock frequency is divided by four before clocking the internal counters. The intergration time period is:

$$T_{SI} = \frac{4}{f_{OSC}} \times 1000$$

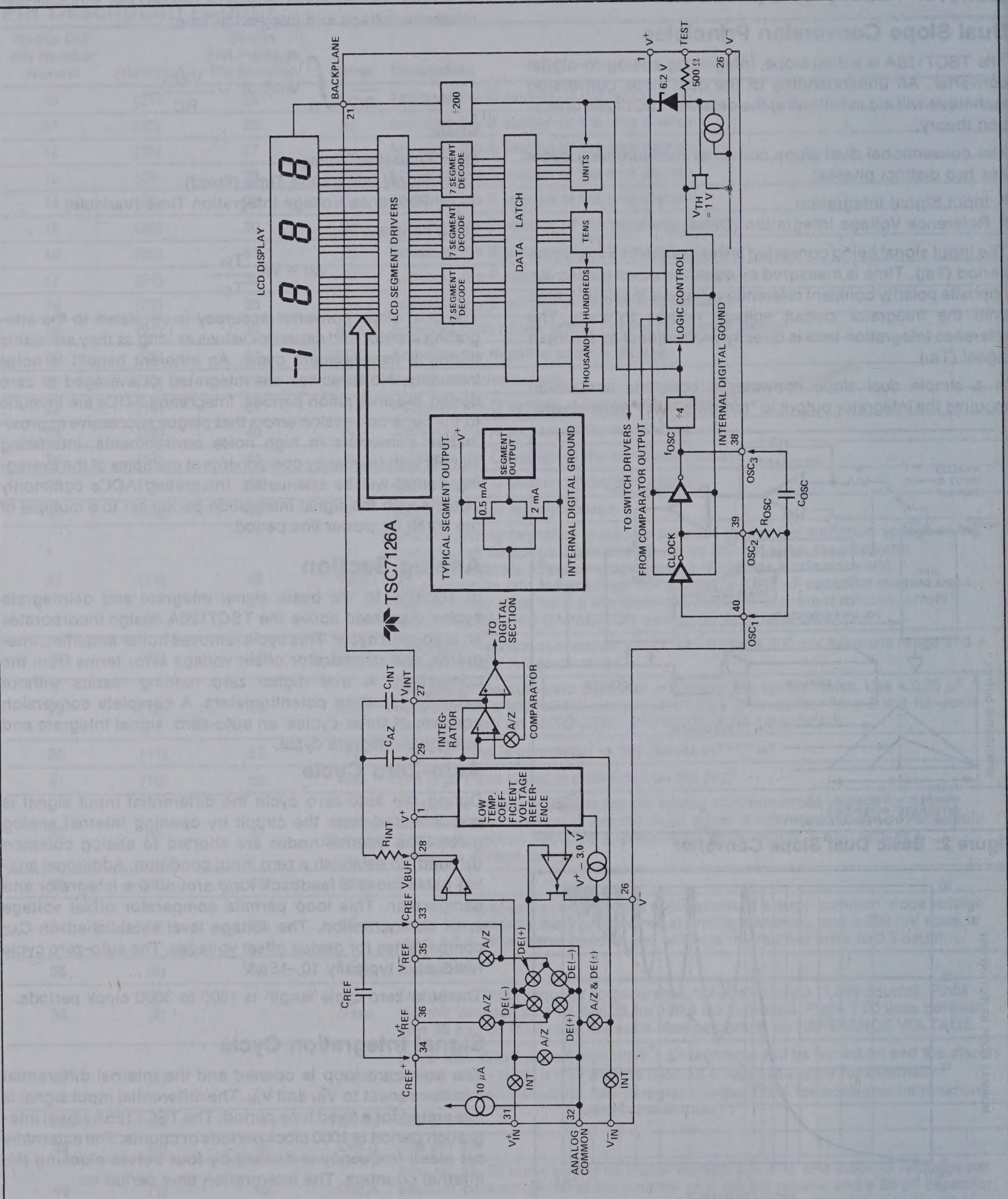

LCD DISPLAY
BACKPLANE
21
LCD SEGMENT DRIVERS
7 SEGMENT DECODE
7 SEGMENT DECODE
7 SEGMENT DECODE
÷200
DATA LATCH
THOUSAND
HUNDREDS
TENS
UNITS
LOGIC CONTROL
TO SWITCH DRIVERS FROM COMPARATOR OUTPUT
CLOCK
f_{OSC}
÷4
INTERNAL DIGITAL GOUND
38
OSC_3
C_{OSC}
39
R_{OSC}
OSC_2
40
OSC_1
V^+
1
TEST
V^-
26
6.2 V
500 Ω
V_{TH} = 1 V
TYPICAL SEGMENT OUTPUT
V^+
SEGMENT OUTPUT
0.5 mA
2 mA
INTERNAL DIGITAL GROUND
TSC7126A
TO DIGITAL SECTION
COMPARATOR
INTEG-RATOR
A/Z
C_{INT}
V_{INT}
27
C_{AZ}
29
LOW TEMP. COEF-FICIENT VOLTAGE REFER-ENCE
V^+
1
R_{INT}
28
V_{BUF}
V^+ – 3.0 V
V^-
26
C_{REF}^-
33
V_{REF}^-
35
A/Z
DE(+)
DE(–)
DE(–)
C_{REF}
V_{REF}^+
36
A/Z
DE(–)
A/Z
DE(+)
A/Z & DE(±)
34
C_{REF}^+
10 µA
INT
INT
31
V_{IN}^+
32
ANALOG COMMON
30
V_{IN}^-

Figure 4: TSC7126A Block Diagram

where:

f_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference Integrate Cycle:

The final phase is reference integrate or deintegrate. V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 internal clock periods. The digital reading displayed is

$$1000 \frac{V_{IN}}{V_{REF}}$$

Digital Section

The TSC7126A contains all the segment drivers necessary to directly drive a 3-1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60 Hz with a 5 V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF." An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^+ and V_{IN}^- are reversed this indicator would reverse.

On the TSC7126A when the test pin is pulled to V^+ all segments are turned "ON." The display reads -1888. During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and segment drive assignment are shown in Figure 5.

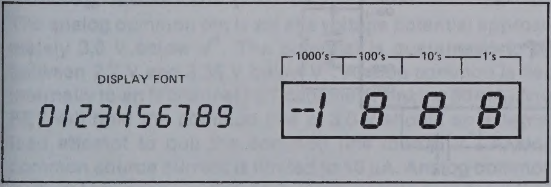


Figure 5: Display FONT and Segment Assignment.

System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The three phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 1000 to 3000 Counts
  (4000 to 12000 Clock Pulses)
  For signals less than full-scale the auto-zero phase is assigned the unused reference integrate time period.
- Signal Integrate: 1000 Counts
  (4000 Clock Pulses)
  This time period is fixed. The integration period is:

$$T_{SI} = 4000 \left[\frac{1}{f_{OSC}}\right]$$

  Where f_{OSC} is the externally set clock frequency.
- Reference Integrate: 0 to 2000 Counts
  (0 to 8000 Clock Pulses)

The TSC7126A is a drop in replacement for the TSC7126 and ICL7126 that offers a greatly improved internal reference temperature coefficient. No external component value changes are required to upgrade existing designs.

Component Value Selection

Auto-Zero Capacitor - C_{AZ}

The C_{AZ} capacitor size has some influence on system noise. A 0.33 μF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 μV. A 0.033 μF capacitor is adequate for 2.0 V full-scale applications. A mylar type dielectric capacitor is adequate.

Reference Voltage Capacitor - C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 μF capacitor is acceptable when V_{IN}^- is tied to analog common. If a large common-mode voltage exists ($V_{REF}^- \neq$ analog common) and the application requires a 200 mV full-scale increase C_{REF} to 1.0 μF. Rollover error will be held to less than 0.5 count. A mylar type dielectric capacitor is adequate.

Integrating Capacitor - C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Due to the TSC7126A superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case a ±2 V full-scale integrator output swing is satisfactory. For 3 readings/second (f_{OSC} = 48 kHz) a 0.047 value is suggested. For one reading per second 0.15 μF is recommended. If a different oscillator frequency is used C_{INT} must be changed in inverse proportion to maintain the nominal ±2 V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}}$$

Where:

f_{OSC} = Clock frequency at Pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

At three readings per seccond, a 750 Ω resistor should be placed in series with C_{INT}. This increases accuracy by compensating for comparator delay. C_{INT} must have low dielectric absorption to minimize roll-over error. An inexpensive polypropylene capacitor is recommended.

Integrating Resistor - R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 6 μA. The integrator and buffer can supply 1 μA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200 mV full-scale R_{INT} is 180 kΩ. A 2.0 V full-scale requires 1.8 mΩ.

Component	**Nominal Full-Scale Voltage**	
Value	200.0 mV	2.000 V
C_{AZ}	0.33 μF	0.033 μF
R_{INT}	180 kΩ	1.8 MΩ
C_{INT}	0.047 μF	0.047 μF

Note:
1. fosc = 48 kHz (3 readings/sec)

Oscillator Components

C_{OSC} should be 50 pF. R_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}$$

For a 48 kHz clock (3 conversions/sec) R = 180 kΩ.

Note that f_{OSC} is divided by four to generate the TSC7126A internal control clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, 33 1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66 2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage *	V_{REF}
200.0 mV	100.0 mV
2.000 V	1.000 V

* $V_{FS} = 2\ V_{REF}$

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400 mV for 2000 lb/in^2. Rather than dividing the input voltage by two the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

Device Pin Functional Description

Differential Signal Inputs

(V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30))

The TSC7126A is designed with true differential inputs and accepts input signals within the input stage common-mode

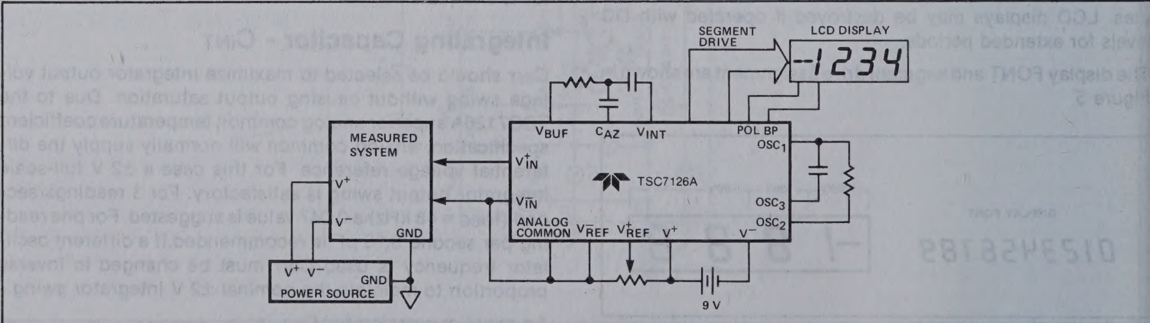


Figure 6: Common-Mode Voltage Removed in Battery Operation with V_{IN} = Analog Common

voltage range (V_{CM}). The typical range is $V^+ - 1.0$ to $V^- + 1$ V. Common-mode voltages are removed from the system when the TSC7126A operates from a battery or floating power source (Isolated from measured system) and V_{IN}^- is connected to analog common (V_{COM}): See Figure 6.

In systems where common-mode voltages exist the TSC7126A 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 7). For such applications the integrator output swing can be reduced below the recommended 2.0 V full-scale swing. The integrator output will swing within 0.3 V of V^+ or V^- without increased linearity error.

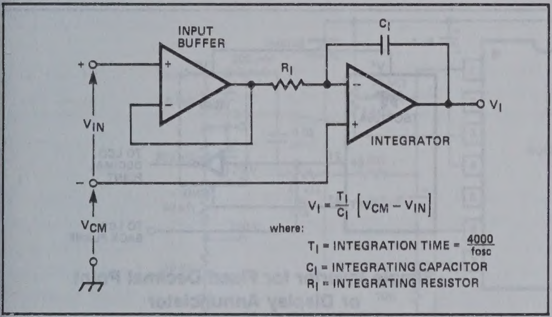

INPUT BUFFER
C_I
R_I
+
−
V_{IN}
V_{CM}
V_I
INTEGRATOR
$V_I = \frac{T_I}{C_I}\left[V_{CM} - V_{IN}\right]$
where:
T_I = INTEGRATION TIME = $\frac{4000}{f_{osc}}$
C_I = INTEGRATING CAPACITOR
R_I = INTEGRATING RESISTOR

Figure 7: Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

Differential Reference

(V_{REF}^+ (Pin 36), V_{REF}^-(Pin 39))

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent rollover type errors being induced by large common-mode voltages C_{REF} should be large compared to stray node capacitance.

The TSC7126A offers a significantly improved analog common temperature coefficient. This potential provides a very stable voltage suitable for use as a voltage reference. The temperature coefficient of analog common is 20 ppm/°C typically.

Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3.0 V below V^+. The potential is guaranteed to be between 2.7 V and 3.35 V below V^+. Analog common is tied internally to an N channel FET capable of sinking 30 mA. This FET will hold the common line at 3.0 V should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 10 μA. Analog common is therefore easily pulled to a more negative voltage (i.e., below V^+ -3.0 V).

The TSC7126A connects the internal V_{IN}^+ and V_{IN}^- inputs to analog common during the auto-zero cycle. During the reference integrate phase V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converters 86 dB common-mode rejection ratio. In battery operation analog common and V_{IN}^- are usually connected removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}^-.

The analog common pin serves to set the analog section reference or common point. The TSC7126A is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TSC7126A power source. The analog common potential of V^+ -3.0 V gives a 7 V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient and a 15 Ω output impedance.

With sufficiently high total supply voltage ($V^+ - V^- > 7.0$ V) analog common is a very stable potential with excellent temperature stability - typically 35 ppm/°C. This potential can be used to generate the TSC7126A reference voltage. An external voltage reference will be unnecessary in most cases because of the 35 ppm/°C temperature coefficient. See TSC7126A Internal Voltage Reference discussion.

Test (Pin 37)

The test pin potential is 5 V less than V^+. Test may be used as the negative power supply connection for external CMOS logic. The test pin is tied to the internally generated negative logic supply through a 500 Ω resistor. The test pin load should be no more than 1 mA. See the applications section for additional information on using test as a negative digital logic supply.

If test is pulled high to V^+ all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes. With Test = V^+ the LCD Segments are impressed with a DC voltage which will destroy the LCD.

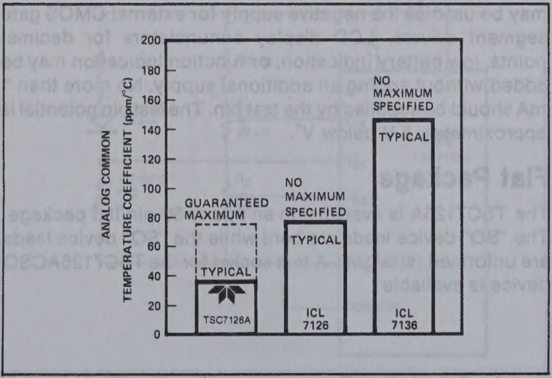


Figure 8: Analog Common Temperature Coefficient

TSC7126A Internal Voltage Reference

The TSC7126A analog common voltage temperature stability has been significantly improved (Figure 8). The "A" version of the industry standard 7126 device will allow users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 9 shows analog common supplying the necessary voltage reference for the TSC7126A.

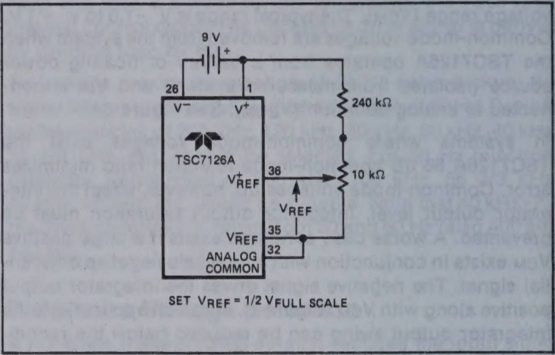


Figure 9: TSC7126A Internal Voltage Reference Connection

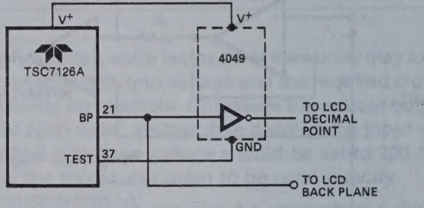
Applications Information

Liquid Crystal Display Sources

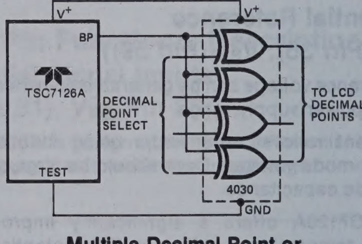
Several LCD manufacturers supply standard LCD displays to interface with the TSC7126A 3 1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers[1]
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216/655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415/347-9916	FE 0801 FE 0203
EPSON	3415 Kashikawa St., Torrance, CA 90505 213/534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414/648-2361	3902, 3933, 3903

Note:
1. Contact LCD manufacturer for full product listing/specifications.



Simple Inverter for Fixed Decimal Point or Display Annunciator



Multiple Decimal Point or Annunciator Driver

Decimal Point and Annunciator Drive

The test pin is connected to the internally-generated digital logic supply ground through a 500 Ω resistor. The test pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the test pin. The test pin potential is approximately 5 V below V⁺.

Flat Package

The TSC7126A is available in an epoxy 60-pin flat package. The "BQ" device leads are bent while the "SQ" device leads are unformed (straight). A test socket for the TSC7126ACSQ device is available:

Part No.: IC 51-42
Manufacturer: Yamaichi
Distribution: Nepenthe Distribution
2471 East Bayshore
Suite 520
Palo Alto, CA 94043
(415) 856-9332

Ratiometric Resistance Measurements

The TSC7126A true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{\text{R Unknown}}{\text{R Standard}} \times 1000$$

The display will overrange for R Unknown ≥ 2 x R Standard.

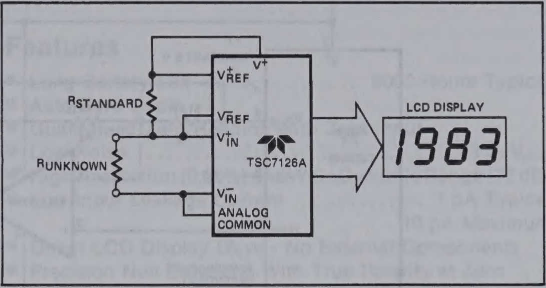
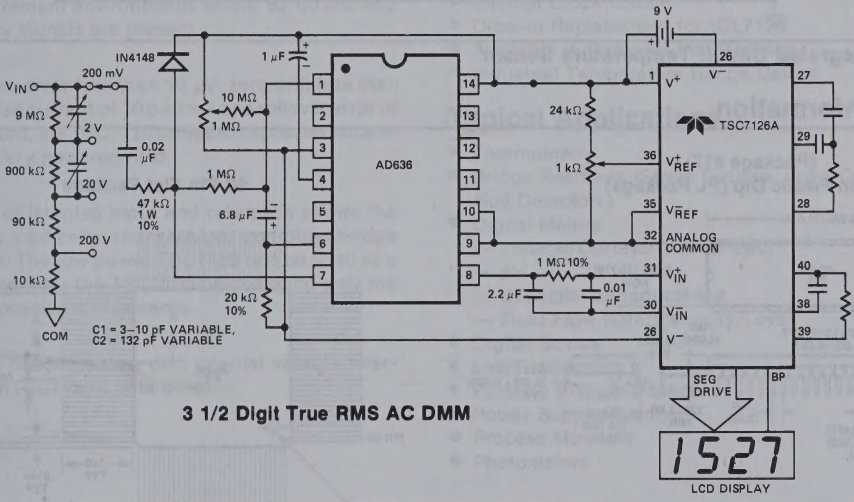

V+
V^+_{REF}
$R_{STANDARD}$
V^-_{REF}
V^+_{IN}
TSC7126A
$R_{UNKNOWN}$
V^-_{IN}
ANALOG COMMON
LCD DISPLAY
1983

Figure 10: Low Parts Count Ratiometric Resistance Measurement


IN4148
1 μF
200 mV
V_{IN}
10 MΩ
1 MΩ
9 MΩ
2 V
0.02 μF
900 kΩ
20 V
1 MΩ
47 kΩ 1 W 10%
6.8 μF
90 kΩ
200 V
10 kΩ
20 kΩ 10%
COM
C1 = 3–10 pF VARIABLE, C2 = 132 pF VARIABLE
AD636
1
2
3
4
5
6
7
8
9
10
11
12
13
14
9 V
26
27
1
V+
V−
24 kΩ
TSC7126A
29
36
1 kΩ
V^+_{REF}
35
28
V^-_{REF}
32
ANALOG COMMON
1 MΩ 10%
31
V^+_{IN}
40
2.2 μF
0.01 μF
30
V^-_{IN}
38
26
V−
39
SEG DRIVE
BP
1527
LCD DISPLAY

3 1/2 Digit True RMS AC DMM

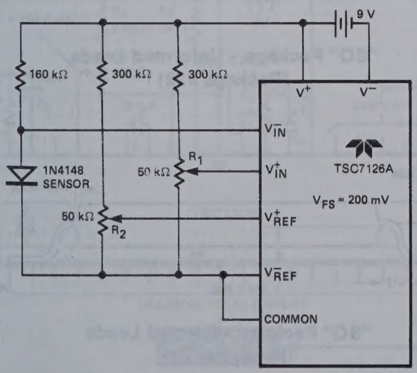

9 V
160 kΩ
300 kΩ
300 kΩ
V+
V−
V^-_{IN}
1N4148 SENSOR
R_1
50 kΩ
V^+_{IN}
TSC7126A
V_{FS} = 200 mV
50 kΩ
R_2
V^+_{REF}
V^-_{REF}
COMMON

Figure 11: Temperature Sensor

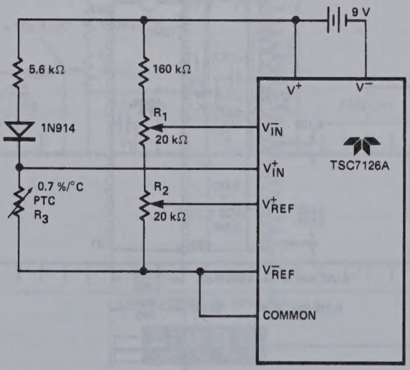

9 V
5.6 kΩ
160 kΩ
V+
V−
1N914
R_1
20 kΩ
V^-_{IN}
V^+_{IN}
TSC7126A
0.7 %/°C PTC R_3
R_2
20 kΩ
V^+_{REF}
V^-_{REF}
COMMON

Figure 12: Positive Temperature Coefficient Resistor Temperature Sensor

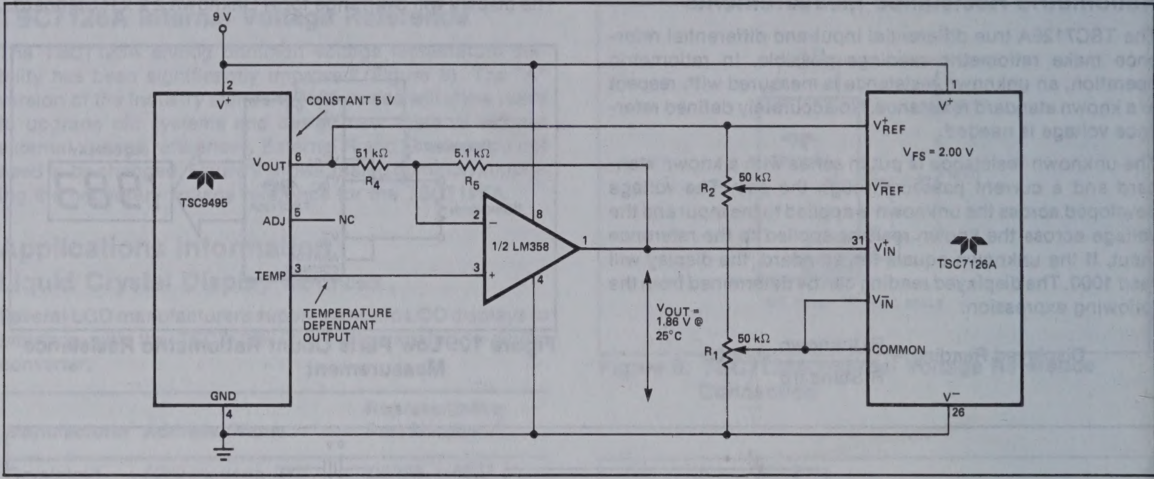
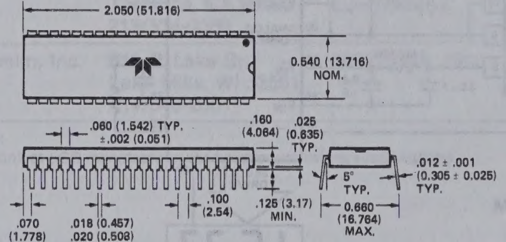

9 V
2
V+
CONSTANT 5 V
VOUT
6
51 kΩ
R4
5.1 kΩ
R5
TSC9495
ADJ
5
NC
TEMP
3
TEMPERATURE DEPENDANT OUTPUT
2
3
8
4
1
1/2 LM358
GND
4
1
V+
V+REF
VFS = 2.00 V
50 kΩ
R2
V−REF
31
V+IN
TSC7126A
V−IN
VOUT = 1.86 V @ 25°C
50 kΩ
R1
COMMON
V−
26

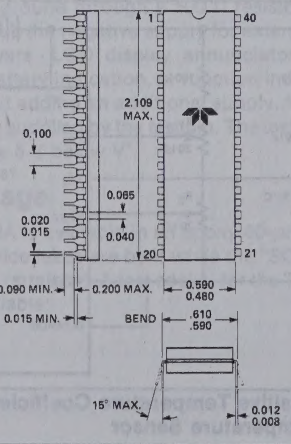
Figure 13: Integrated Circuit Temperature Sensor

Package Information

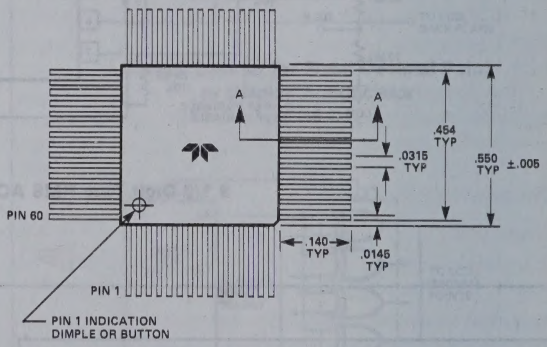
(Package #17)
40-Pin Plastic Dip (PL Package)


2.050 (51.816)
0.540 (13.716) NOM.
.060 (1.542) TYP. ±.002 (0.051)
.160 (4.064)
.025 (0.635) TYP.
5° TYP.
.012 ± .001 (0.305 ± 0.025) TYP.
.070 (1.778) TYP.
.018 (0.457) .020 (0.508) TYP.
.100 (2.54)
.125 (3.17) MIN.
0.660 (16.764) MAX.

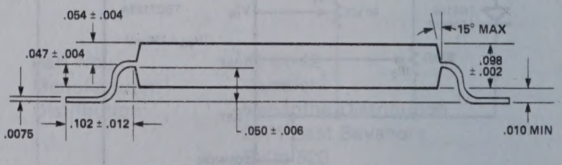
(Package #20)
40-Pin CerDIP


1
40
2.109 MAX.
0.100
0.065
0.020 0.015
0.040
20
21
0.090 MIN.
0.200 MAX.
0.590 0.480
0.015 MIN.
BEND
.610 .590
15° MAX.
0.012 0.008

60-Pin Flat Package


A
A
.454 TYP
.550 TYP ±.005
.0315 TYP
PIN 60
.140 TYP
.0145 TYP
PIN 1
PIN 1 INDICATION DIMPLE OR BUTTON

"SQ" Package - Unformed Leads
(Package #22)


.054 ± .004
.047 ± .004
15° MAX
.098 ±.002
.0075
.102 ± .012
.050 ± .006
.010 MIN

"BQ" Package - Formed Leads
(Package #21)

TELEDYNE SEMICONDUCTOR

TSC7126
3 1/2 Digit A/D Converter
• Low Power Dissipation - 900 μW Max.

General Description

The single chip CMOS TSC7126 incorporates all the active devices for a 3 1/2 digit analog-to-digital converter to directly drive an LCD display. The internal oscillator, voltage reference and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution -0.05% - indicating meter requires only a display, four resistors, four capacitors and a 9 V battery. The flat package option eases the mechanical design of low cost, hand held multimeters and systems.

The TSC7126 dual slope conversion technique rejects interference signals when the integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

With an auto-zero error less than 10 μV, zero drift less than 1 μV/° C, input bias current of 10 pA max and rollover error of less than one count, the TSC7126 brings exceptional value to the portable battery powered field.

In addition, the differential input and reference allows the measurement on load cells, strain gauges and other bridge type transducers. The low power TSC7126 can be used as a plug-in replacement for the TSC7106 by changing only the values of seven passive components.

For applications needing a low drift internal voltage reference refer to the TSC7126A data sheet.

Features

- Long Battery Life .... 8000 Hours Typical
- Auto-Zero Cycle
- Guaranteed Zero Reading With Zero Input
- Low Noise .... 15 μV_{p-p}
- High Resolution (0.05%) and Wide Dynamic Range (72 dB)
- Low Input Leakage Current .... 1 pA Typical
10 pA Maximum
- Direct LCD Display Drive - No External Components.
- Precision Null Detection With True Polarity at Zero
- High Impedance Differential Input
- Convenient 9 V Battery Operation With Low Power Dissipation .... 500 μW Typical
900 μW Maximum
- Internal Clock Circuit
- Drop-In Replacement for ICL7126
- Available in Compact Flat Package
- Industrial Temperature Range Device

Typical Applications

- Thermometry
- Bridge Readouts (Strain Gauges, Load Cells, Null Detectors)
- Digital Meters
  - — Voltage/Current/Ohms/Power
  - — pH
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity/Level
- Digital Scales
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Photometers

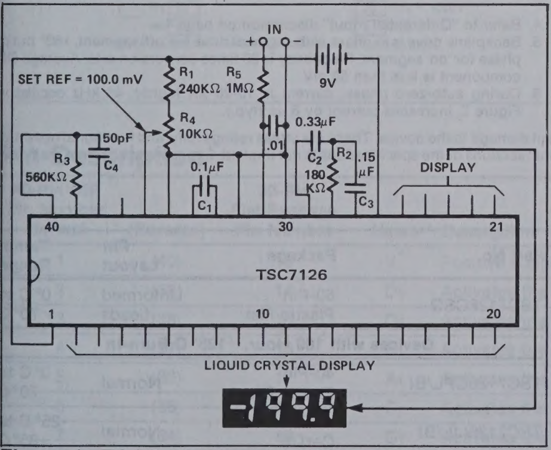

IN
+
−
9V
SET REF = 100.0 mV
R1
240KΩ
R5
1MΩ
R4
10KΩ
50pF
C4
R3
560KΩ
.01
0.33μF
C2
180
KΩ
R2
.15
μF
C3
0.1μF
C1
DISPLAY
40
30
21
TSC7126
1
10
20
LIQUID CRYSTAL DISPLAY
-1999

Figure 1: TSC7126 Clock Frequency 16 kHz (1 reading/sec.)

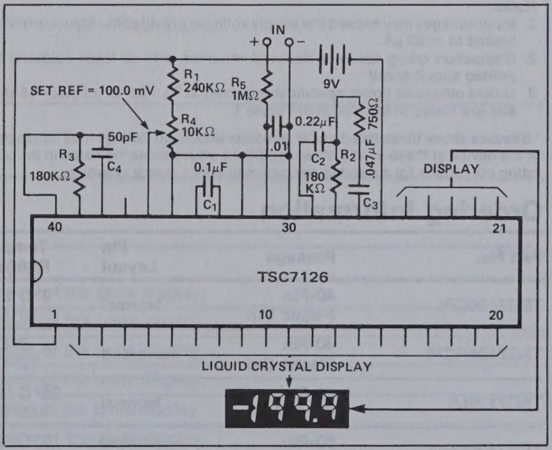

IN
+
−
9V
SET REF = 100.0 mV
R1
240KΩ
R5
1MΩ
R4
10KΩ
50pF
C4
R3
180KΩ
.01
0.22μF
C2
180
KΩ
R2
.047μF
750Ω
C3
0.1μF
C1
DISPLAY
40
30
21
TSC7126
1
10
20
LIQUID CRYSTAL DISPLAY
-1999

Figure 2: TSC7126 Clock Frequency 48 kHz (3 readings/sec.)

Absolute Maximum Ratings*

Supply voltage (V^+ to V^-) .... 15 V
Analog Input Voltage (either input) (1) .... V^+ to V^-
Reference Input Voltage (either input) .... V^+ to V^-
Clock Input .... Test to V^+
Power Dissipation (2)
Ceramic Package .... 1000 mW
Plastic Package .... 800 mW
Operating Temperature
(C Device) .... 0° C to +70° C
(I Device) .... -25° C to +85° C
Storage Temperature .... -65° C to +160° C
Lead Temperature (Soldering, 60 sec) .... 300° C

Electrical Characteristics [3]

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0 mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200 mV or Full Scale = 2.000 V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio[4]	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0 mV	—	50	—	μV/V
Noise (Pk - Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0 mV	—	15	—	μV
Leakage Current @ Input	V_{IN} = 0V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 $0° < T_A < 70°$C	—	0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV $0 < T_A < 70°$C (Ext. Ref. 0 ppm/°C)	—	1	5	ppm/°C
Supply Current (Does not include Common current)	V_{IN} = 0 Note 6	—	50	100	μA
Analog Common Voltage (with respect to positive supply)	250KΩ between Common and positive supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to positive supply)	250KΩ between Common and positive supply	—	80	—	ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs. Clock Frequency	—	40	—	pF

Notes:

1. Input voltages may exceed the supply voltages provided the input current is limited to ±100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless otherwise noted, specifications apply at T_A = 25° C. f_{CLOCK} = 16 kHz and are tested in the circuit of Figure 1.
4. Refer to "Differential Input" discussion on page 4.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
6. During auto-zero phase, current is 10-20 μA higher. 48 kHz oscillator Figure 2, increases current by 8 μa (typ.).

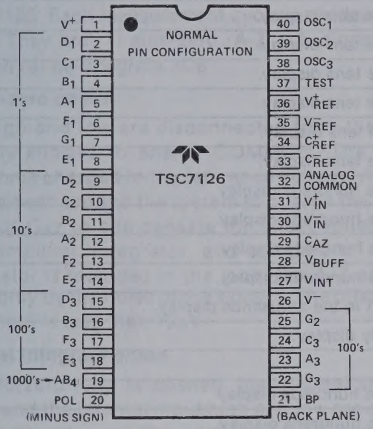
* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

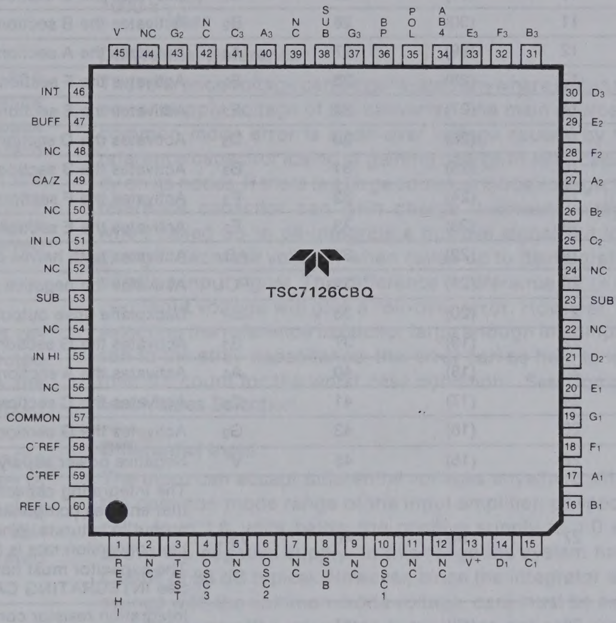
Ordering Information

Part No.	Package	Pin Layout	Temp. Range
TSC7126CPL	40-Pin Plastic Dip	Normal	0° C to 70° C
TSC7126RCPL	40-Pin Plastic Dip	Reversed	0° C 70° C
TSC7126IJL	40-Pin CerDIP	Normal	-25° C to +85° C
TSC7126CBQ	60-Pin Plastic Flat	Formed Leads	0° C to 70° C

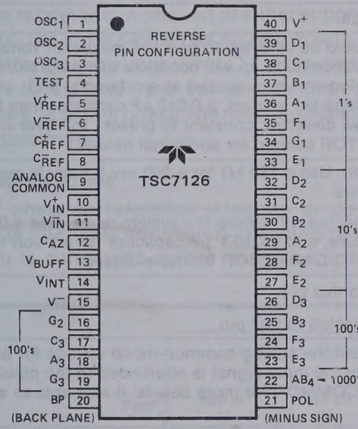
Part No.	Package	Pin Layout	Temp. Range
TSC7126CSQ	60-Pin Plastic Flat	Unformed Leads	0° C to 70° C
Devices with 160 Hour, +125° C Burn-In			
TSC7126CPL/BI	40-Pin Plastic Dip	Normal	0° C to 70° C
TSC7126IJL/BI	40-Pin CerDIP	Normal	-25° C to +85° C

Pin Configuration


NORMAL PIN CONFIGURATION
TSC7126
V+ 1, D1 2, C1 3, B1 4, A1 5, F1 6, G1 7, E1 8, D2 9, C2 10, B2 11, A2 12, F2 13, E2 14, D3 15, B3 16, F3 17, E3 18, AB4 19, POL 20
1's
10's
100's
1000's
(MINUS SIGN)
40 OSC1, 39 OSC2, 38 OSC3, 37 TEST, 36 V+REF, 35 V−REF, 34 C+REF, 33 C−REF, 32 ANALOG COMMON, 31 V+IN, 30 V−IN, 29 CAZ, 28 VBUFF, 27 VINT, 26 V−, 25 G2, 24 C3, 23 A3, 22 G3, 21 BP
(BACK PLANE)


TSC7126CBQ
45 V−, 44 NC, 43 G2, 42 NC, 41 C3, 40 A3, 39 NC, 38 SUB, 37 G3, 36 BP, 35 POL, 34 AB4, 33 E3, 32 F3, 31 B3
46 INT, 47 BUFF, 48 NC, 49 CA/Z, 50 NC, 51 IN LO, 52 NC, 53 SUB, 54 NC, 55 IN HI, 56 NC, 57 COMMON, 58 C−REF, 59 C+REF, 60 REF LO
30 D3, 29 E2, 28 F2, 27 A2, 26 B2, 25 C2, 24 NC, 23 SUB, 22 NC, 21 D2, 20 E1, 19 G1, 18 F1, 17 A1, 16 B1
1 REF HI, 2 NC, 3 TEST, 4 OSC3, 5 NC, 6 OSC2, 7 NC, 8 SUB, 9 NC, 10 OSC1, 11 NC, 12 NC, 13 V+, 14 D1, 15 C1

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.


REVERSE PIN CONFIGURATION
TSC7126
OSC1 1, OSC2 2, OSC3 3, TEST 4, V+REF 5, V−REF 6, C+REF 7, C−REF 8, ANALOG COMMON 9, V+IN 10, V−IN 11, CAZ 12, VBUFF 13, VINT 14, V− 15, G2 16, C3 17, A3 18, G3 19, BP 20
(BACK PLANE)
100's
40 V+, 39 D1, 38 C1, 37 B1, 36 A1, 35 F1, 34 G1, 33 E1, 32 D2, 31 C2, 30 B2, 29 A2, 28 F2, 27 E2, 26 D3, 25 B3, 24 F3, 23 E3, 22 AB4, 21 POL
1's
10's
100's
1000's
(MINUS SIGN)

Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
9	(32)	21	D_2	Activates the D section of the tens display.
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP	Backplane drive output.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 μF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See INTEGRATING CAPACITOR section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 180 kΩ for a 200 mV full-scale range and a 1.80 MΩ for 2 V full-scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.33 μF capacitor for a 200 mV full-scale, and a 0.033 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The low input is connected to this pin.
31	(10)	55	V_{IN}^+	The high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.
34	(7)	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common mode voltage exists (for example the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.
36	(5)	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read −1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38.

Detailed Description

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the 7126. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate, (DE).

1. Auto-zero phase

Input high and low are disconnected from the pins and internally shorted to analog COMMON. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10µV.

2. Signal Integrate phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (—) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. See Component Values Selection.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator

7

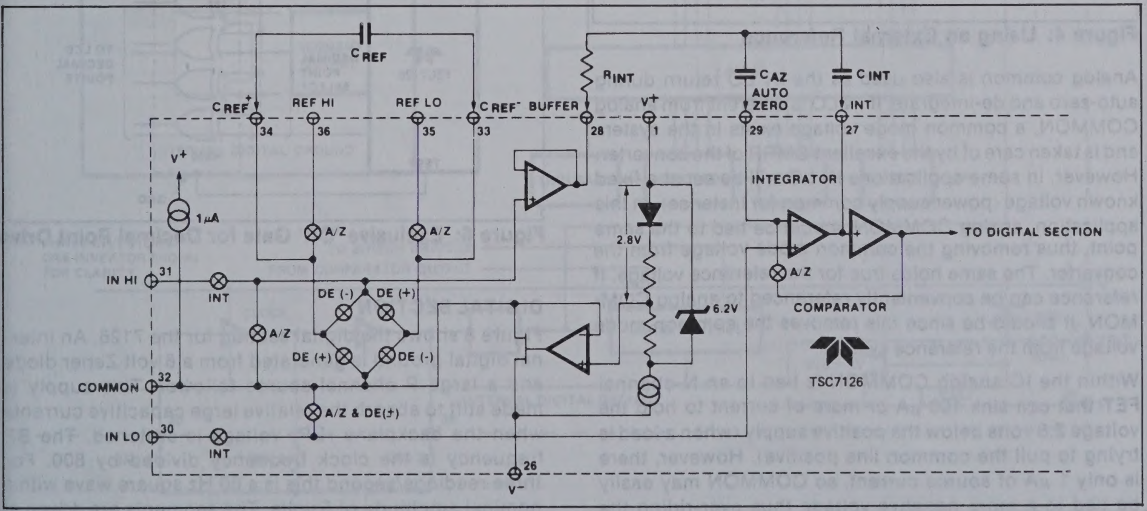


Figure 3: Analog Section of TSC7126.

positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≃15Ω), and a temperature coefficient typically less than 80 ppm/°C.

An external reference may be added to improve temperature stability. The circuit is shown in Figure 4.

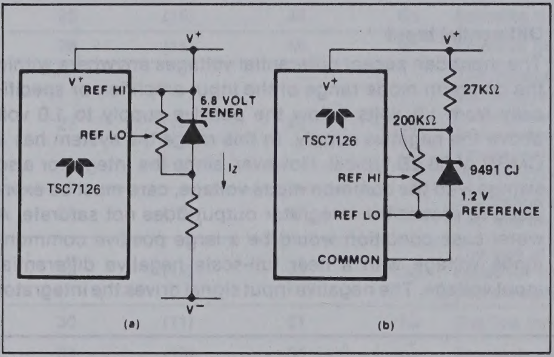


Figure 4: Using an External Reference

Analog common is also used as the IN LO return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC analog COMMON is tied to an N-channel FET that can sink 100 μA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 1 μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. No more than a 1 mA load should be applied. Figures 5 and 6 show such an application.

The second function is a "lamp test". When TEST is pulled high (to V⁺) all segments will be turned on and the display should read - 1888. The TEST pin will sink about 10 mA under these conditions.

Caution: In the lamp test mode, the segments have a constant d-c voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

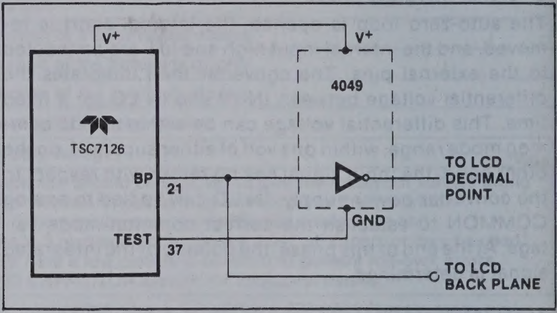


Figure 5: Simple Inverter for Fixed Decimal Point

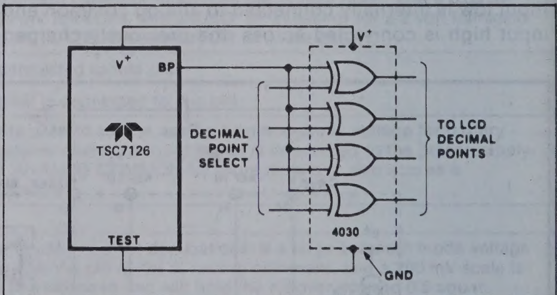


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

DIGITAL SECTION

Figure 8 shows the digital section for the 7126. An internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with

BP when OFF, but out of phase when ON. In all cases, negligible d-c voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

System Timing

Three clocking methods may be used: (Figure 7)

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, Oscillator frequencies of 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

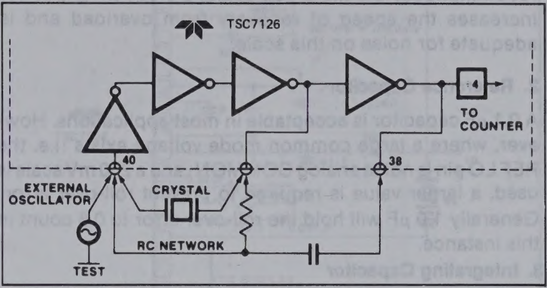

TSC7126
÷4
TO COUNTER
40
38
EXTERNAL OSCILLATOR
CRYSTAL
RC NETWORK
TEST

Figure 7: Clock Circuits

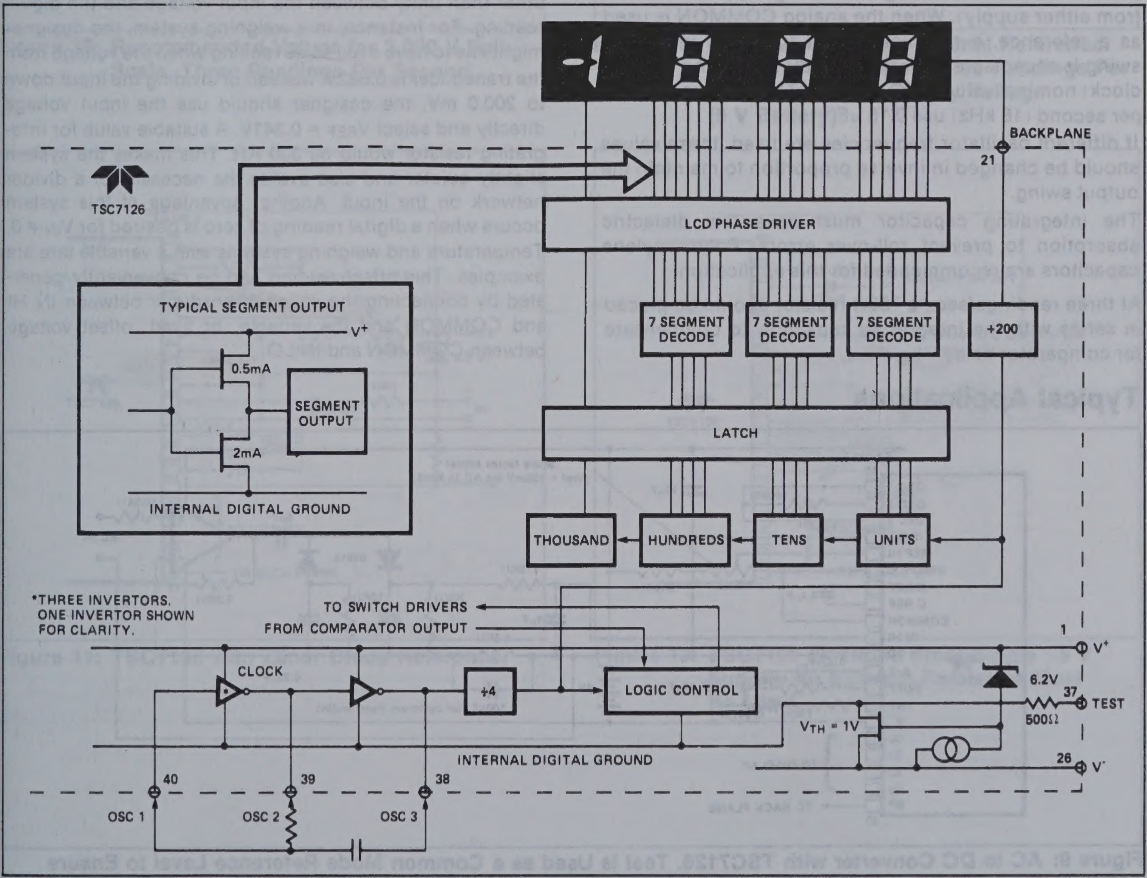

BACKPLANE
21
TSC7126
LCD PHASE DRIVER
TYPICAL SEGMENT OUTPUT
V+
0.5mA
SEGMENT OUTPUT
2mA
INTERNAL DIGITAL GROUND
7 SEGMENT DECODE
7 SEGMENT DECODE
7 SEGMENT DECODE
÷200
LATCH
THOUSAND
HUNDREDS
TENS
UNITS
*THREE INVERTORS. ONE INVERTOR SHOWN FOR CLARITY.
TO SWITCH DRIVERS
FROM COMPARATOR OUTPUT
CLOCK
÷4
LOGIC CONTROL
1
V+
6.2V
37
TEST
500Ω
V_{TH} = 1V
INTERNAL DIGITAL GROUND
26
V-
40
39
38
OSC 1
OSC 2
OSC 3

Figure 8: Digital Section

Component Value Selection

1. Auto-zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise is very important, a 0.33 μF capacitor is recommended. On the 2 volt scale, a 0.033 μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

2. Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200 mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

3. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 volt full scale integrator swing is acceptable). For three readings/second (48 kHz clock) nominal value for C_{INT} is 0.047 μF, for one reading per second (16 kHz) use 0.15 μF.

If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

At three readings/sec., a 750Ω resistor should be placed in series with the integrating capacitor, to compensate for comparator delay.

4. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6 μA of quiescent current. They can supply ~1 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 1.8 MΩ is near optimum and similarly 180 KΩ for a 200.0 mV scale.

5. Oscillator Components

For all ranges of frequency a 50 pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim \frac{45}{RC}$. For 48 kHz clock (3 readings/second), R = 180 KΩ.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2\,V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. A suitable value for integrating resistor would be 330 KΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

Typical Applications

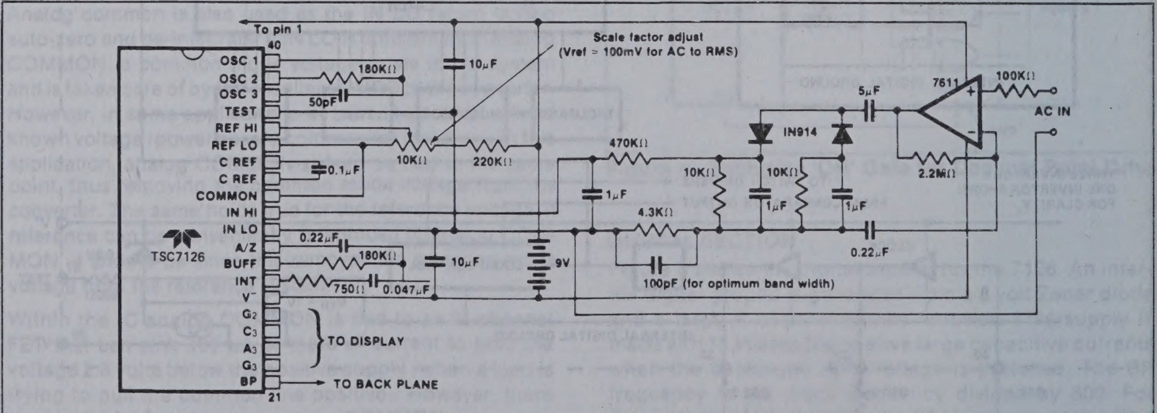


Figure 9: AC to DC Converter with TSC7126. Test is Used as a Common Mode Reference Level to Ensure Compatibility with Most Op-amps.

Typical Applications (Cont.)

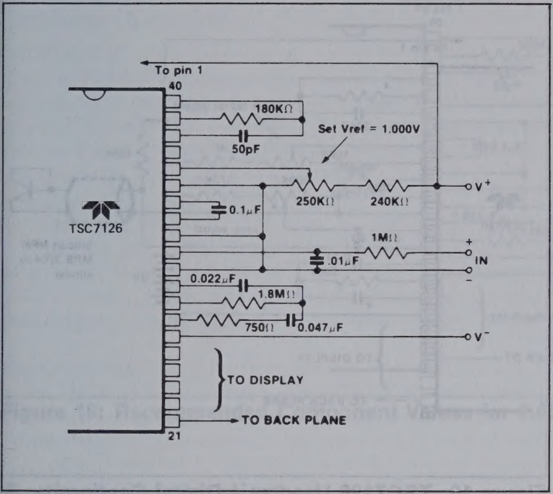

To pin 1
40
180KΩ
50pF
Set Vref = 1.000V
250KΩ
240KΩ
V+
0.1μF
TSC7126
1MΩ
.01μF
+
IN
-
0.022μF
1.8MΩ
750Ω
0.047μF
V-
TO DISPLAY
TO BACK PLANE
21

Figure 10: Recommended Values for 2.000 V Full-Scale, Three Readings Per Second.

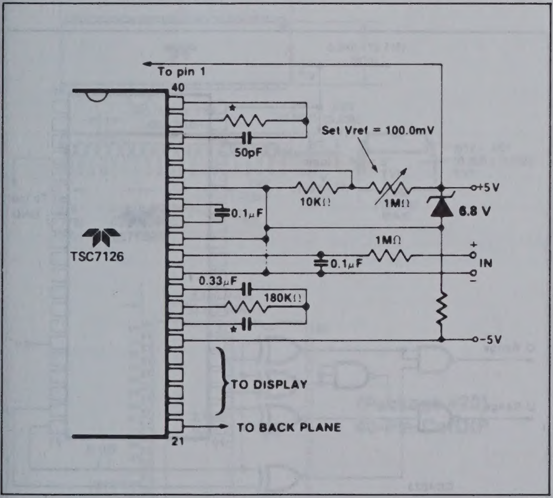

To pin 1
40
*
50pF
Set Vref = 100.0mV
+5V
10KΩ
1MΩ
6.8 V
0.1μF
TSC7126
1MΩ
0.1μF
+
IN
-
0.33μF
180KΩ
*
-5V
TO DISPLAY
TO BACK PLANE
21

Figure 11: TSC7126 with Zener Diode Reference.

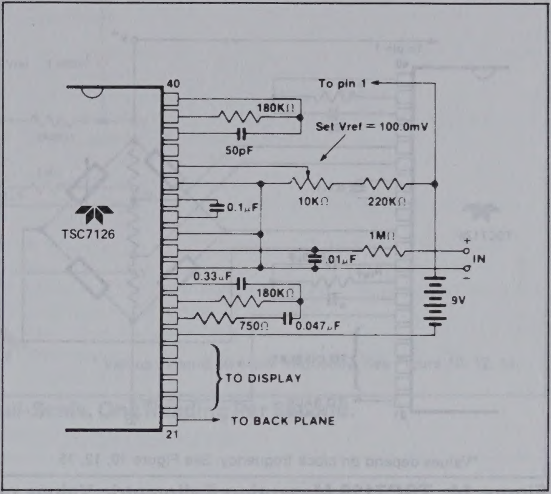

40
To pin 1
180KΩ
50pF
Set Vref = 100.0mV
10KΩ
220KΩ
0.1μF
TSC7126
1MΩ
.01μF
+
IN
-
0.33μF
180KΩ
9V
750Ω
0.047μF
TO DISPLAY
TO BACK PLANE
21

Figure 12: TSC7126 Using the Internal Reference. 200.0 mV Full-Scale, Three Readings Per Second, Floating Supply Voltage (9 V Battery).

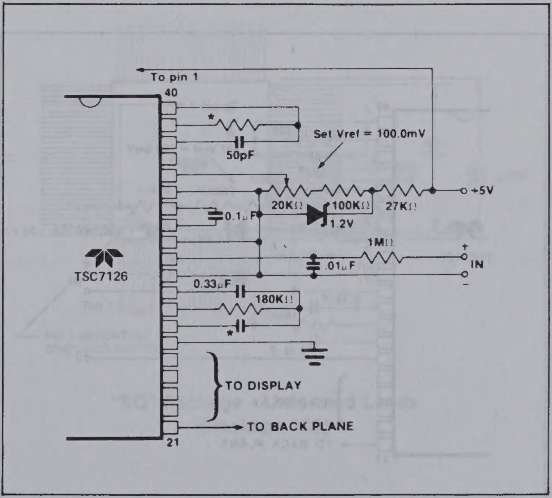
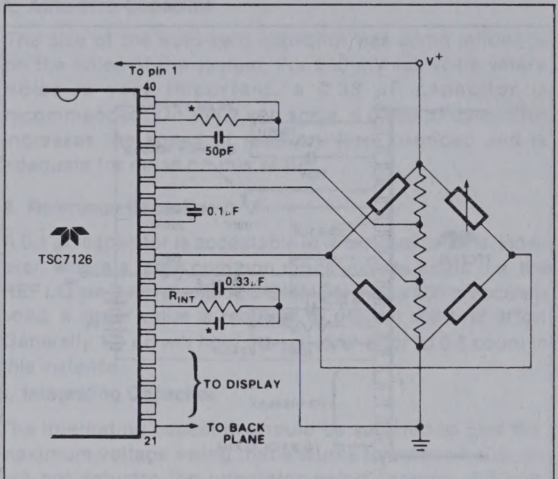

To pin 1
40
*
50pF
Set Vref = 100.0mV
+5V
20KΩ
100KΩ
27KΩ
1.2V
0.1μF
TSC7126
1MΩ
.01μF
+
IN
-
0.33μF
180KΩ
*
TO DISPLAY
TO BACK PLANE
21

Figure 13: TSC7126 Operated From Single +5 V Supply. An External Reference Must Be Used.

Typical Applications (Cont.)


To pin 1
V+
40
*
50pF
0.1μF
TSC7126
0.33μF
R_INT
*
TO DISPLAY
TO BACK PLANE
21

*Values depend on clock frequency. See Figure 10, 12, 15.

Figure 14: TSC7126 Measuring Ratiometric Values of Quad Load Cell. The Resistor Values Within the Bridge are Determined by the Desired Sensitivity.

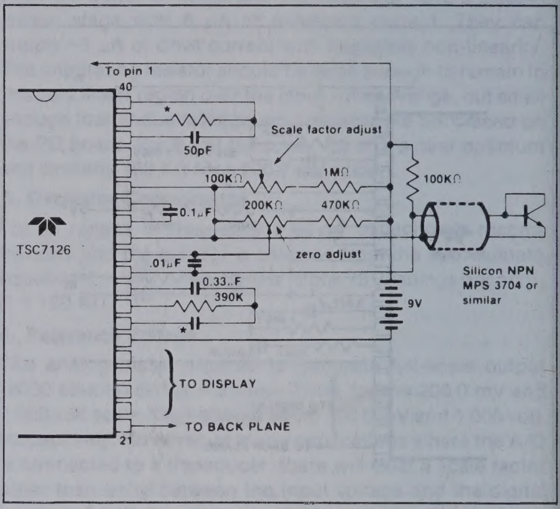

To pin 1
40
*
50pF
Scale factor adjust
100KΩ
1MΩ
100KΩ
0.1μF
200KΩ
470KΩ
TSC7126
zero adjust
.01μF
0.33μF
390K
9V
Silicon NPN
MPS 3704 or
similar
*
TO DISPLAY
TO BACK PLANE
21

Figure 16: TSC7126 Used as a Digital Centigrade Thermometer. A Silicon Diode-Connected Transistor Has a Temperature Coefficient of About 2 mV/°C.

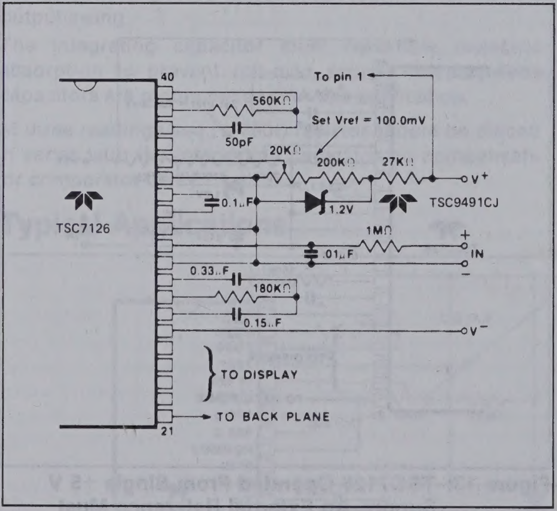

40
To pin 1
560KΩ
50pF
Set Vref = 100.0mV
20KΩ
200KΩ
27KΩ
V+
0.1μF
1.2V
TSC9491CJ
TSC7126
1MΩ
+
.01μF
IN
−
0.33μF
180KΩ
0.15μF
V−
TO DISPLAY
TO BACK PLANE
21

Figure 15: TSC7126 With an External Band-Gap Reference (1.2 V Typ) IN LO Is Tied to Common. Values Shown are for One Reading Per Second.

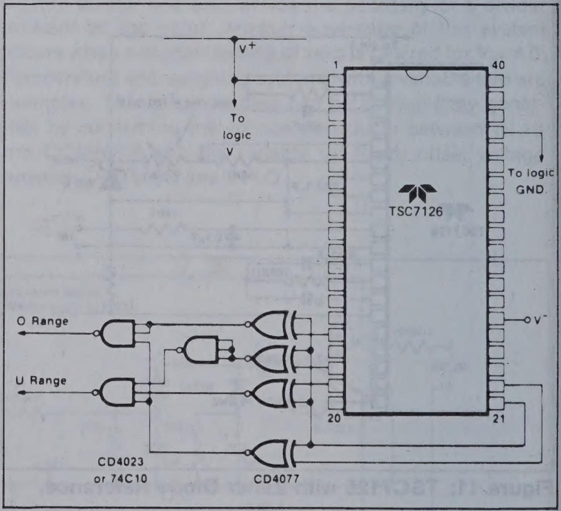

V+
1
40
To logic V
To logic GND.
TSC7126
O Range
V−
U Range
20
21
CD4023 or 74C10
CD4077

Figure 17: Circuit for Developing Underrange and Overrange Signals from TSC7126 Outputs.

Typical Applications (Cont.)

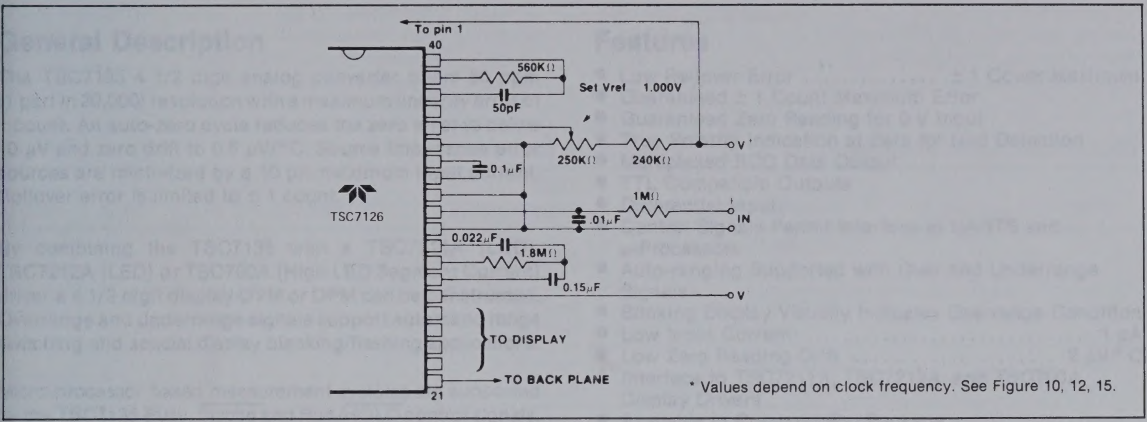
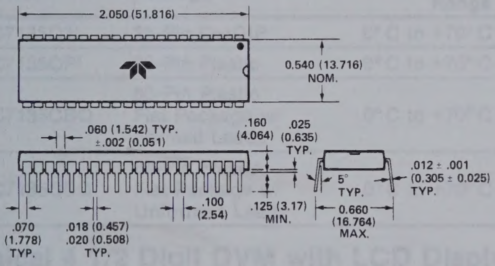

To pin 1
40
560KΩ
50pF
Set Vref 1.000V
250KΩ
240KΩ
0.1μF
TSC7126
1MΩ
.01μF
IN
0.022μF
1.8MΩ
0.15μF
V
TO DISPLAY
TO BACK PLANE
21
* Values depend on clock frequency. See Figure 10, 12, 15.

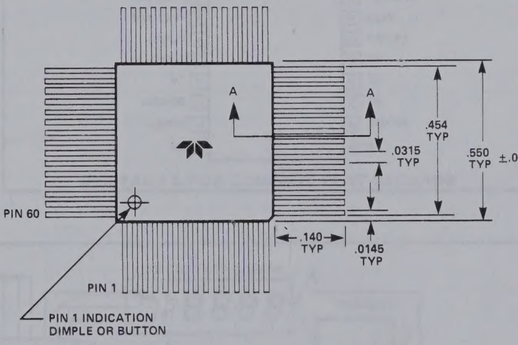
Figure 18: Recommended Component Values for 2.00 V Full-Scale, One Reading Per Second.

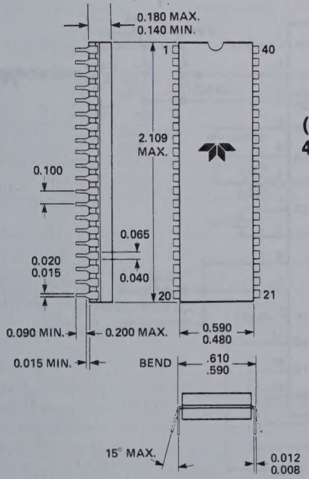
Package Information

(Package #17)
40-Pin Plastic Dip (PL Package)


2.050 (51.816)
0.540 (13.716) NOM.
.060 (1.542) TYP. ±.002 (0.051)
.160 (4.064)
.025 (0.635) TYP.
5° TYP.
.012 ± .001 (0.305 ± 0.025) TYP.
.100 (2.54)
.125 (3.17) MIN.
0.660 (16.764) MAX.
.070 (1.778) TYP.
.018 (0.457) .020 (0.508) TYP.

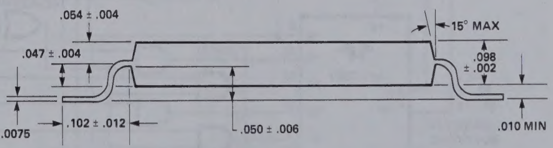
60-Pin Flat Package


A
A
.454 TYP
.0315 TYP
.550 TYP ±.005
PIN 60
.140 TYP
.0145 TYP
PIN 1
PIN 1 INDICATION DIMPLE OR BUTTON


0.180 MAX.
0.140 MIN.
1
40
2.109 MAX.
0.100
0.065
0.020
0.015
0.040
20
21
0.090 MIN.
0.200 MAX.
0.590
0.480
0.015 MIN.
BEND
.610
.590
15° MAX.
0.012
0.008

(Package #20)
40-Pin CerDIP

"SQ" Package - Unformed Leads
(Package #22)


.054 ± .004
15° MAX
.047 ± .004
.098 ± .002
.0075
.102 ± .012
.050 ± .006
.010 MIN

"BQ" Package - Formed Leads
(Package #21)

Notes

TELEDYNE SEMICONDUCTOR

TSC7135
4 1/2 Digit Precision Analog-to-Digital Converter

General Description

The TSC7135 4 1/2 digit analog converter offers 50 ppm (1 part in 20,000) resolution with a maximum linearity error of 1 count. An auto-zero cycle reduces the zero error to below 10 μV and zero drift to 0.5 μV/°C. Source impedance error sources are minimized by a 10 pA maximum input current. Rollover error is limited to ± 1 count.

By combining the TSC7135 with a TSC7211A (LCD), TSC7212A (LED) or TSC700A (High LED Segment Current) driver a 4 1/2 digit display DVM or DPM can be constructed. Overrange and underrange signals support automatic range switching and special display blanking/flashing applications.

Micro-processor based measurement systems are supported by the TSC7135 Busy, $\overline{\text{Strobe}}$ and Run/$\overline{\text{HOLD}}$ control signals. Remote data acquisition systems with data transfer via UARTs are also possible. The additional control pins and multiplexed BCD outputs make the TSC7135 the ideal converter for display or μ-processor based measurement systems.

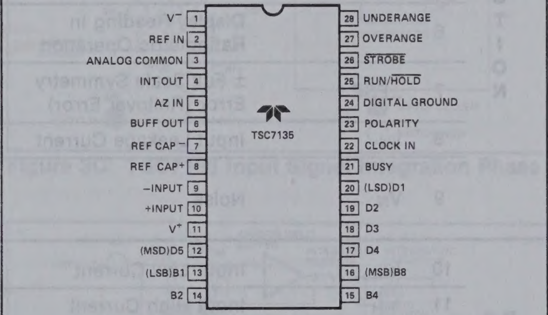
Ordering Information

Part No.	Package	Temperature Range
TSC7135CJI	28-Pin CerDIP	0°C to +70°C
TSC7135CPI	28-Pin Plastic	0°C to +70°C
TSC7135CBQ	60-Pin Plastic Flat Package w/ Formed Leads	0°C to +70°C
TSC7135CSQ	60-Pin Plastic Flat Package w/ Unformed Leads	0°C to +70°C

Features

- Low Rollover Error .... ± 1 Count Maximum
- Guaranteed ± 1 Count Maximum Error
- Guaranteed Zero Reading for 0 V Input
- True Polarity Indication at Zero for Null Detection
- Multiplexed BCD Data Output
- TTL Compatible Outputs
- Differential Input
- Control Signals Permit Interface to UARTS and μ-Processors
- Auto-ranging Supported with Over and Underrange Signals
- Blinking Display Visually Indicates Overrange Condition
- Low Input Current .... 1 pA
- Low Zero Reading Drift .... 2 μV/°C
- Interface to TSC7211A, TSC7212A, and TSC700A Display Drivers
- Available in Compact Flat Package

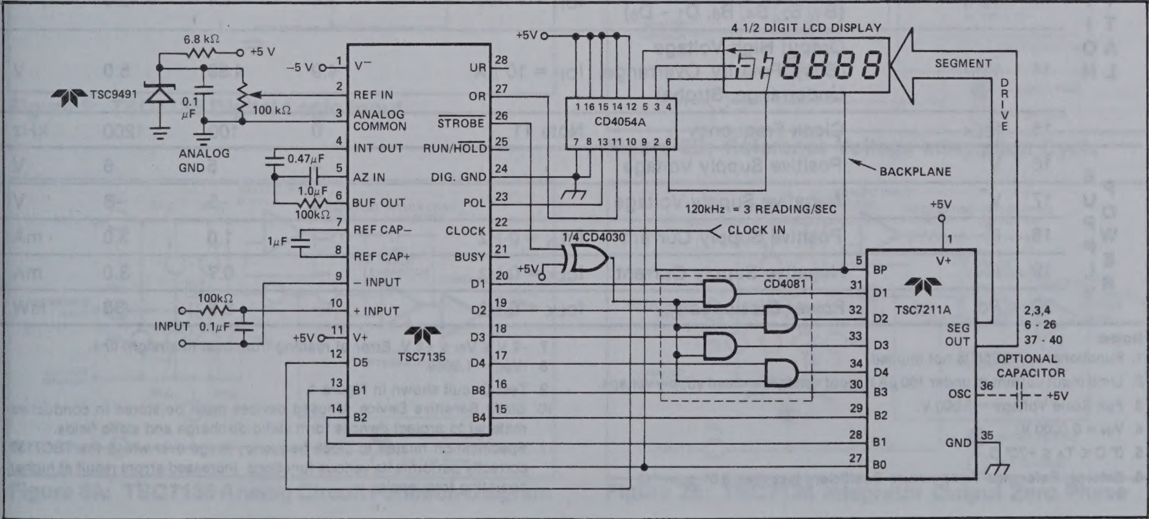
Pin Configuration



V− 1
REF IN 2
ANALOG COMMON 3
INT OUT 4
AZ IN 5
BUFF OUT 6
REF CAP − 7
REF CAP+ 8
−INPUT 9
+INPUT 10
V+ 11
(MSD)D5 12
(LSB)B1 13
B2 14
28 UNDERANGE
27 OVERANGE
26 STROBE
25 RUN/HOLD
24 DIGITAL GROUND
23 POLARITY
22 CLOCK IN
21 BUSY
20 (LSD)D1
19 D2
18 D3
17 D4
16 (MSB)B8
15 B4
TSC7135

SEE PAGE 5 FOR COMPACT FLAT PACKAGE

Typical 4 1/2 Digit DVM with LCD Display



6.8 kΩ
+5 V
TSC9491
0.1 μF
100 kΩ
ANALOG GND
−5 V
0.47μF
1.0μF
100kΩ
1μF
100kΩ
INPUT 0.1μF
+5V
1 V−
2 REF IN
3 ANALOG COMMON
4 INT OUT
5 AZ IN
6 BUF OUT
7 REF CAP−
8 REF CAP+
9 − INPUT
10 + INPUT
11 V+
12 D5
13 B1
14 B2
UR 28
OR 27
STROBE 26
RUN/HOLD 25
DIG. GND 24
POL 23
CLOCK 22
BUSY 21
D1 20
D2 19
D3 18
D4 17
B8 16
B4 15
TSC7135
+5V
1 16 15 14 12 5 3 4
CD4054A
7 8 13 11 10 9 2 6
1/4 CD4030
+5V
CD4081
4 1/2 DIGIT LCD DISPLAY
SEGMENT DRIVE
BACKPLANE
120kHz = 3 READING/SEC
CLOCK IN
+5V
1
V+
5 BP
31 D1
32 D2
33 D3
34 D4
30 B3
29 B2
28 B1
27 B0
TSC7211A
SEG OUT
2,3,4
6 - 26
37 - 40
OPTIONAL CAPACITOR
36 OSC
+5V
GND 35

© 1983

Absolute Maximum Ratings (Note 1)

Positive Supply Voltage	+6 V
Negative Supply voltage	-9 V
Analog Input Voltage (Pin 9 or 10)	V^+ to V^- (Note 2)
Reference Input Voltage (Pin 2)	V^+ to V^-
Clock Input Voltage	0 V to V^+
Operating Temperature Range	0° C to +70° C
Storage Temperature Range	-65° C to +160° C
Soldering Lead Temperature (10 Seconds)	300° C
CerDIP(J) Package Power Dissipation	1 W
Plastic(P) Package Power Dissipation	0.8 W

Electrical Specifications: T_A = 25° C, f_{CLOCK} = 120 kHz, V^+ = 5.0 V, V^- = −5 V

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7135 MIN	TSC7135 TYP	TSC7135 MAX	UNIT
ANALOG SECTION	1		Display Reading with Zero Volt Input	Note 3,4	-0.0000	±0.0000	+0.0000	Display Reading
	2	TC_Z	Zero Reading Temperature Coefficient	V_{IN} = 0 V Note 5	—	0.5	2	μV/°C
	3	TC_{FS}	Full Scale Temperature Coefficient	V_{IN} = 2 V Notes 5,6	—	—	5	ppm/°C
	4	NL	Nonlinearity Error	Note 7	—	0.5	1	count
	5	DNL	Differential Linearity Error	Note 7	—	0.01	—	LSB
	6		Display Reading In Ratiometric Operation	V_{IN} = V_{REF} Note 3	+0.9998	+0.9999	+1.0000	Display Reading
	7	±FSE	± Full Scale Symmetry Error (Rollover Error)	$-V_{IN} = +V_{IN}$ Note 8	—	0.5	1	count
	8	I_{IN}	Input Leakage Current	Note 4	—	1	10	pA
	9	V_N	Noise	Peak-to-Peak Value not exceed 95% of time	—	15	—	μV_{p-p}
DIGITAL SECTION	10	I_{NL}	Input Low Current	V_{IN} = 0 V	—	10	100	μA
	11	I_{NH}	Input High Current	V_{IN} = +5 V	—	0.08	10	μA
	12	V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	—	0.20	0.40	V
	13	V_{OH}	Output High Voltage (B_1, B_2, B_4, B_8, D_1 - D_5)	I_{OH} = 1 mA	2.4	4.4	5.0	V
	14	V_{OH}	Output High Voltage (Busy, Polarity, Overrange, Underrange, Strobe)	I_{OH} = 10 μA	4.9	4.99	5.0	V
	15	f_{CLK}	Clock Frequency	Note 11	0	100	1200	kHz
POWER SUPPLY	16	V^+	Positive Supply Voltage		4	5	6	V
	17	V^-	Negative Supply Voltage		-3	-5	-8	V
	18	I^+	Positive Supply Current	f_{CLK} = 0 Hz	—	1.0	3.0	mA
	19	I^-	Negative Supply Current	f_{CLK} = 0 Hz	—	0.7	3.0	mA
	20	Pd	Power Dissipation	f_{CLK} = 0 Hz	—	8.5	30	mW

Notes:

1. Functional operation is not implied.
2. Limit input current to under 100 μA if input voltages exceed supply voltage.
3. Full Scale Voltage = 2.000 V.
4. V_{IN} = 0.0000 V.
5. 0° C ≤ T_A ≤ +70° C.
6. External Reference Temperature Coefficient less than 0.01 ppm/° C.
7. -2 V ≤ V_{IN} ≤ +2 V. Error of reading from best fit straight line.
8. $|V_{IN}|$ = 1.9959.
9. Test Circuit shown in Figure 1.
10. Static Sensitive Device. Unused devices must be stored in conductive material to protect devices form static discharge and static fields.
11. Specification related to clock frequency range over which the TSC7135 correctly performs its various functions. Increased errors result at higher operating frequencies.

Test Circuits

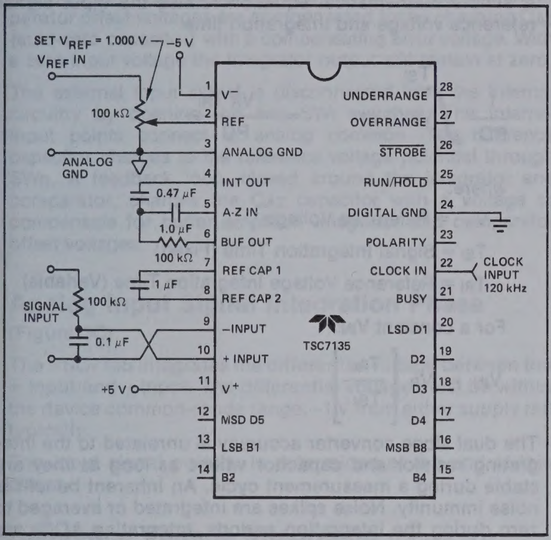

SET V_{REF} = 1.000 V
V_{REF} IN
−5 V
100 kΩ
ANALOG GND
0.47 µF
1.0 µF
100 kΩ
1 µF
SIGNAL INPUT
100 kΩ
0.1 µF
+5 V
1 V⁻
2 REF
3 ANALOG GND
4 INT OUT
5 A-Z IN
6 BUF OUT
7 REF CAP 1
8 REF CAP 2
9 −INPUT
10 + INPUT
11 V⁺
12 MSD D5
13 LSB B1
14 B2
28 UNDERRANGE
27 OVERRANGE
26 STROBE
25 RUN/HOLD
24 DIGITAL GND
23 POLARITY
22 CLOCK IN
21 BUSY
20 LSD D1
19 D2
18 D3
17 D4
16 MSB B8
15 B4
CLOCK INPUT 120 kHz
TSC7135

Figure 1: TSC7135 Test Circuit

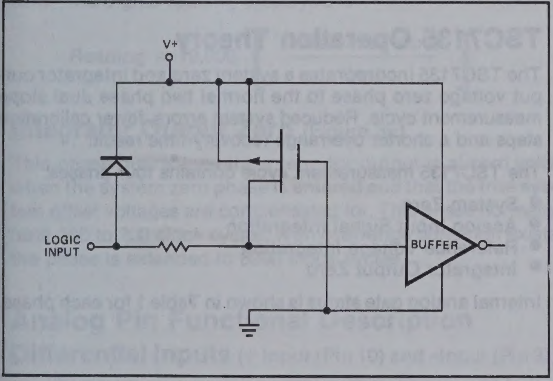

V+
LOGIC INPUT
BUFFER

Figure 2: TSC7135 Digital Logic Input

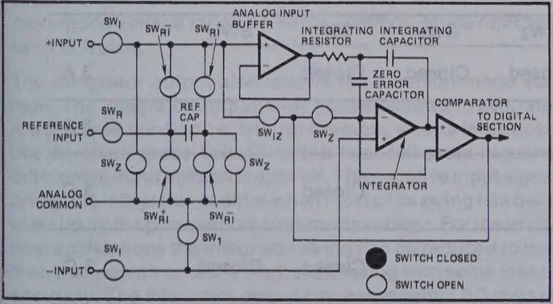

ANALOG INPUT BUFFER
INTEGRATING RESISTOR
INTEGRATING CAPACITOR
ZERO ERROR CAPACITOR
COMPARATOR
TO DIGITAL SECTION
INTEGRATOR
+INPUT
REFERENCE INPUT
ANALOG COMMON
−INPUT
SW_I
SW_{RI}^-
SW_{RI}^+
SW_R
REF CAP
SW_Z
SW_{IZ}
SW_1
SWITCH CLOSED
SWITCH OPEN

Figure 3A: TSC7135 Analog Circuit Function Diagram

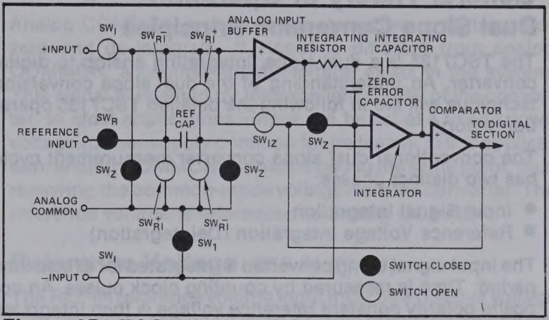

ANALOG INPUT BUFFER
INTEGRATING RESISTOR
INTEGRATING CAPACITOR
ZERO ERROR CAPACITOR
COMPARATOR
TO DIGITAL SECTION
INTEGRATOR
+INPUT
REFERENCE INPUT
ANALOG COMMON
−INPUT
SW_I
SW_{RI}^-
SW_{RI}^+
SW_R
REF CAP
SW_Z
SW_{IZ}
SW_1
SWITCH CLOSED
SWITCH OPEN

Figure 3B: TSC7135 System Zero Phase

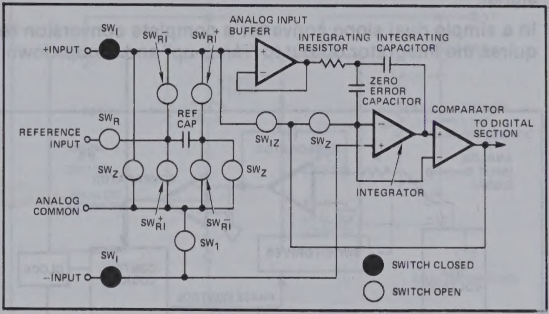

ANALOG INPUT BUFFER
INTEGRATING RESISTOR
INTEGRATING CAPACITOR
ZERO ERROR CAPACITOR
COMPARATOR
TO DIGITAL SECTION
INTEGRATOR
+INPUT
REFERENCE INPUT
ANALOG COMMON
−INPUT
SW_I
SW_{RI}^-
SW_{RI}^+
SW_R
REF CAP
SW_Z
SW_{IZ}
SW_1
SWITCH CLOSED
SWITCH OPEN

Figure 3C: TSC7135 Input Signal Integration Phase

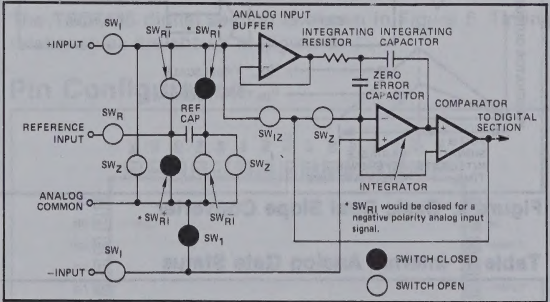

ANALOG INPUT BUFFER
INTEGRATING RESISTOR
INTEGRATING CAPACITOR
ZERO ERROR CAPACITOR
COMPARATOR
TO DIGITAL SECTION
INTEGRATOR
+INPUT
REFERENCE INPUT
ANALOG COMMON
−INPUT
SW_I
SW_{RI}^-
* SW_{RI}^+
SW_R
REF CAP
SW_Z
SW_{IZ}
SW_1
* SW_{RI} would be closed for a negative polarity analog input signal.
SWITCH CLOSED
SWITCH OPEN

Figure 3D: Reference Voltage Integration Cycle

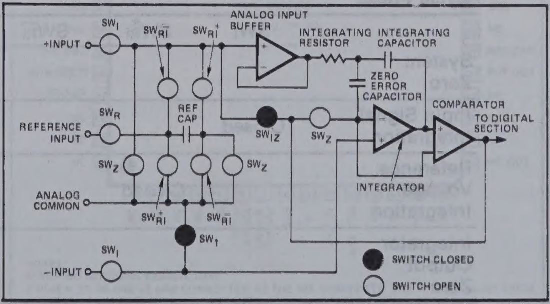

ANALOG INPUT BUFFER
INTEGRATING RESISTOR
INTEGRATING CAPACITOR
ZERO ERROR CAPACITOR
COMPARATOR
TO DIGITAL SECTION
INTEGRATOR
+INPUT
REFERENCE INPUT
ANALOG COMMON
−INPUT
SW_I
SW_{RI}^-
SW_{RI}^+
SW_R
REF CAP
SW_Z
SW_{IZ}
SW_1
SWITCH CLOSED
SWITCH OPEN

Figure 3E: TSC7135 Integrator Output Zero Phase

General Theory of Operation

Dual Slope Conversion Principles

The TSC7135 is a dual slope, integrating analog to digital converter. An understanding of the dual slope conversion technique will aid in following the detailed TSC7135 operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

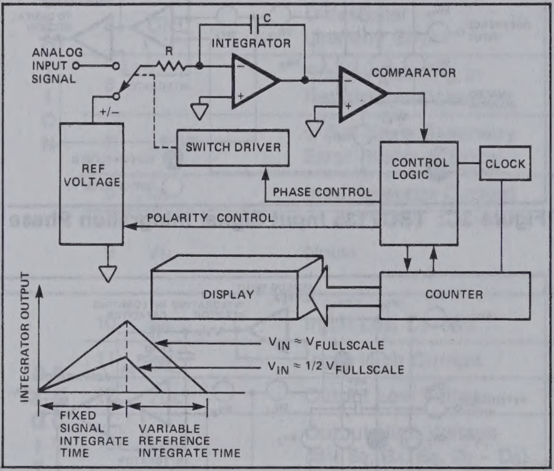


Figure 3: Basic Dual Slope Converter

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)\,dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage

T_{SI} = Signal Integration Time (Fixed)

T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R \left[\frac{T_{RI}}{T_{SI}}\right]$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments.

TSC7135 Operation Theory

The TSC7135 incorporates a system zero and integrator output voltage zero phase to the normal two phase dual slope measurement cycle. Reduced system errors, fewer calibration steps and a shorter overrange recovery time result.

The TSC7135 measurement cycle contains four phases:

- System Zero
- Analog Input Signal Integration
- Reference Voltage Integration
- Integrator Output Zero

Internal analog gate status is shown in Table 1 for each phase.

Table 1: Internal Analog Gate Status

Conversion Cycle Phase	Internal Analog Gate Status							Reference Schematic
	SW_I	$SW_{\overset{+}{RI}}$	$SW_{\overline{RI}}$	SW_Z	SW_R	SW_1	SW_{IZ}	
System Zero				Closed	Closed	Closed		3 A
Input Signal Integration	Closed							3 B
Reference Voltage Integration		Closed*				Closed		3 C
Integrator Output Zero						Closed	Closed	3 D

Note: *Assumes a positive polarity input signal. $SW_{\overline{RI}}$ would be closed for a negative input signal.

System Zero Phase (Figure 3B)

During this phase errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage. With a zero input voltage the integrator output will remain at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

Analog Input Signal Integration Phase (Figure 3C)

The TSC7135 integrates the differential voltage between the + Input and − Input. The differential voltage must be within the device common-mode range; −1 V from either supply rail typically.

The input signal polarity is determined at the end of this phase.

Reference Voltage Integration (Figure 3D)

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. The digital reading displayed is:

$$\text{Reading} = 10{,}000 \left[\frac{\text{Differential Input}}{V_{REF}} \right]$$

Integrator Output Zero (Figure 3E)

This phase guarantees the integrator output is at zero volts when the system zero phase is entered and that the true system offset voltages are compensated for. This phase normally lasts 100 to 200 clock cycles. If an overrange condition exists the phase is extended to 6200 clock cycles.

Analog Pin Functional Description

Differential Inputs (+ Input (Pin 10) and −Input (Pin 9))

The TSC7135 operates with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 0.5 V below the positive supply to 1.0 V above the negative supply. Within this common-mode voltage range an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst case condition exists, for example, when a large positive common-mode voltage with a near full scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4 V full scale swing with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common (Pin 3)

Analog COMMON is used as the −Input return during auto-zero and de-integrate. If −Input is different from analog COMMON, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications −Input will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to analog COMMON.

Reference Voltage (REF IN (Pin 2))

The REF IN reference voltage input must be a positive voltage with respect to analog COMMON. Two reference voltage circuits are shown in Figure 4.

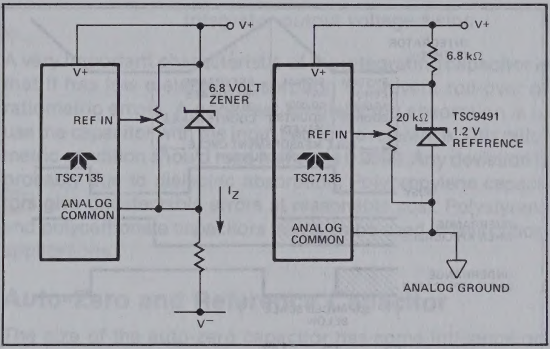
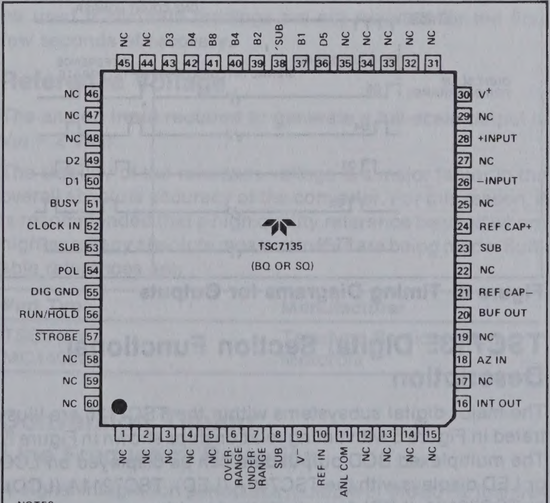

V+
V+
6.8 VOLT ZENER
REF IN
TSC7135
ANALOG COMMON
I_Z
V−
V+
V+
6.8 kΩ
20 kΩ
TSC9491 1.2 V REFERENCE
REF IN
TSC7135
ANALOG COMMON
ANALOG GROUND

Figure 4: Using an External Reference

The TSC7135 digital section is shown in Figure 5. Timing relationships are shown in Figure 6.

Pin Configuration


NC
NC
D3
D4
B8
B4
B2
SUB
B1
D5
NC
NC
NC
NC
45
44
43
42
41
40
39
38
37
36
35
34
33
32
31
NC 46
NC 47
NC 48
D2 49
D1 50
BUSY 51
CLOCK IN 52
SUB 53
POL 54
DIG GND 55
RUN/HOLD 56
STROBE 57
NC 58
NC 59
NC 60
30 V+
29 NC
28 +INPUT
27 NC
26 −INPUT
25 NC
24 REF CAP+
23 SUB
22 NC
21 REF CAP−
20 BUF OUT
19 NC
18 AZ IN
17 NC
16 INT OUT
TSC7135
(BQ OR SQ)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
NC
NC
NC
NC
NC
OVER RANGE
UNDER RANGE
SUB
V−
REF IN
ANL COM
NC
NC
NC
NC

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

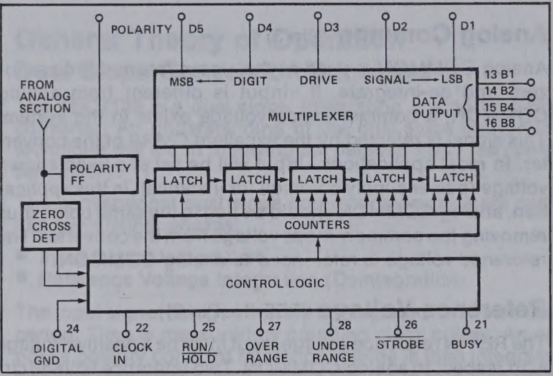

POLARITY
D5
D4
D3
D2
D1
FROM ANALOG SECTION
MSB ← DIGIT DRIVE SIGNAL → LSB
MULTIPLEXER
DATA OUTPUT
13 B1
14 B2
15 B4
16 B8
POLARITY FF
LATCH
LATCH
LATCH
LATCH
LATCH
ZERO CROSS DET
COUNTERS
CONTROL LOGIC
24 DIGITAL GND
22 CLOCK IN
25 RUN/HOLD
27 OVER RANGE
28 UNDER RANGE
26 STROBE
21 BUSY

Figure 5: TSC7135 Digital Section Function Diagram

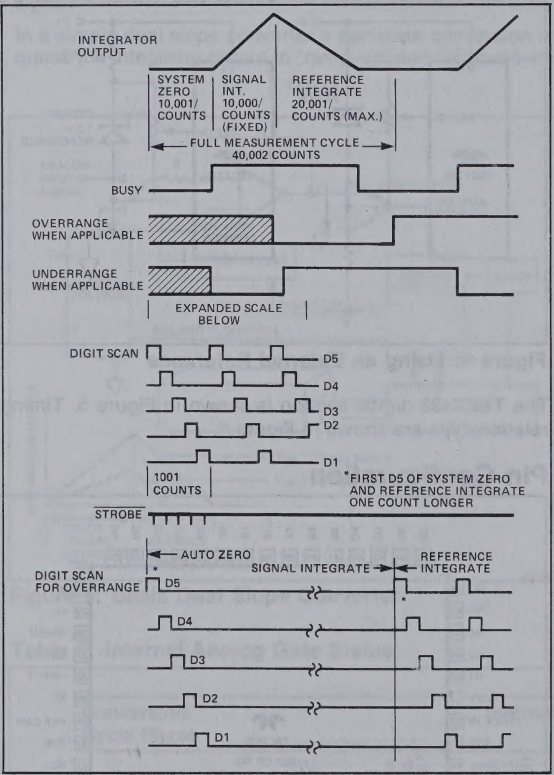

INTEGRATOR OUTPUT
SYSTEM ZERO 10,001/ COUNTS
SIGNAL INT. 10,000/ COUNTS (FIXED)
REFERENCE INTEGRATE 20,001/ COUNTS (MAX.)
FULL MEASUREMENT CYCLE 40,002 COUNTS
BUSY
OVERRANGE WHEN APPLICABLE
UNDERRANGE WHEN APPLICABLE
EXPANDED SCALE BELOW
DIGIT SCAN
D5
D4
D3
D2
D1
1001 COUNTS
*FIRST D5 OF SYSTEM ZERO AND REFERENCE INTEGRATE ONE COUNT LONGER
STROBE
AUTO ZERO
SIGNAL INTEGRATE
REFERENCE INTEGRATE
DIGIT SCAN FOR OVERRANGE
D5
D4
D3
D2
D1

Figure 6: Timing Diagrams for Outputs

TSC7135 Digital Section Functional Description

The major digital subsystems within the TSC7135 are illustrated in Figure 5 with timing relationships shown in Figure 6. The multiplexed BCD output data can be displayed on LCD or LED displays with the TSC700A (LED), TSC7211A (LCD), or TSC7212A (LED) four digit display drivers.

The digital section is best described through a discussion of the control signals and data outputs.

Run/$\overline{\text{Hold}}$ Input (Pin 25)

When left open this pin assumes a logic 1 level. With R/$\overline{\text{H}}$ = 1 the TSC7135 performs conversions continuously with a new measurement cycle beginning every 40,002 clock pulses. When R/$\overline{\text{H}}$ changes to a logic 0 the measurement cycle in progress will be completed and data held and displayed as long as the logic 0 condition exists.

A positive pulse (>300 ns) at R/$\overline{\text{H}}$ will initiate a new measurement cycle. The measurement cycle in progress when R/$\overline{\text{H}}$ initially assumed the logic "0" state must be completed before the positive pulse can be recognized as a single conversion run command.

The new measurement cycle begins with a 10,001 count auto-zero phase. At the end of this phase the busy signal goes high.

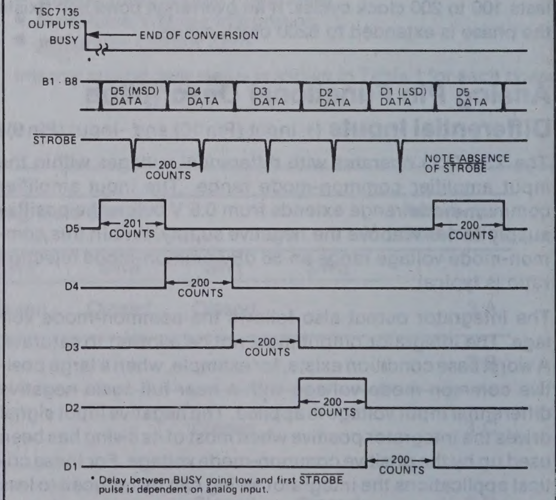
$\overline{\text{Strobe}}$ Output (Pin 26)

During the measurement cycle the $\overline{\text{STROBE}}$ control line is pulsed low five times. The five low pulses occur in the center of the digit drive signals (D_1, D_2, D_3, D_5). (Figure 7)

D_5 (MSD) goes high for 201 counts when the measurement cycles end. In the center of the D_5 pulse, 101 clock pulses after the end of the measurement cycle, the first $\overline{\text{STROBE}}$ occurs for one-half clock pulse. After the D_5 digit strobe, D_4 goes high for 200 clock pulses. The $\overline{\text{STROBE}}$ goes low 100 clock pulses after D_4 goes high. This continues through the D_1 digit drive pulse.

The digit drive signals will continue to permit display scanning. $\overline{\text{STROBE}}$ pulses are not repeated until a new measurement is completed. The digit drive signals will not continue if the previous signal resulted in an overrange condition.

The active low $\overline{\text{STROBE}}$ pulses aid BCD data transfer to UARTs, processors and external latches. See Application Note AN16.


TSC7135 OUTPUTS
BUSY
END OF CONVERSION
B1 - B8
D5 (MSD) DATA
D4 DATA
D3 DATA
D2 DATA
D1 (LSD) DATA
D5 DATA
STROBE
200 COUNTS
NOTE ABSENCE OF STROBE
D5
201 COUNTS
200 COUNTS
D4
200 COUNTS
D3
200 COUNTS
D2
200 COUNTS
D1
200 COUNTS

* Delay between BUSY going low and first $\overline{\text{STROBE}}$ pulse is dependent on analog input.

Figure 7: Strobe Signal Pulses Low 5 Times Per Conversion.

Busy Output (Pin 21)

At the beginning of the signal integration phase BUSY goes high and remains high until the first clock pulse after the integrator zero crossing. BUSY returns to the logic "0" state after the measurement cycle ends in a overrange condition. The internal display latches are loaded during the first clock pulse after busy and are latched at the clock pulse end. The busy signal does not go high at the beginning of the measurement cycle which starts with the auto-zero cycle.

Overrange Output (Pin 27)

If the input signal causes the reference voltage integration time to exceed 20,000 clock pulses the overrange output is set to a logic 1. The overrange output register is set when BUSY goes low and is reset at the beginning of the next reference integration phase.

TSC7135 Digital Section Functional Description (Cont.)

Underrange Output (Pin 28)

If the output count is 9% of full scale or less (≤1800 counts) the underrange register bit is set at the end of BUSY. The bit is set low at the next signal integration phase.

Polarity Output (Pin 23)

A positive input is registered by a logic 1 polarity signal. The polarity bit is valid at the beginning of reference integrate and remains valid until determined during the next conversion.

The polarity bit is valid even for a zero reading. Signals less than the converters LSB will have the signal polarity determined correctly. This is useful in null applications.

Digit Drive Outputs (Pins 12, 17, 18, 19 & 20)

Digit drive signals are positive going signals. The scan sequence is D_5 to D_1. All positive pulses are 200 clock pulses wide except D_5 which is 201 clock pulses wide.

All five digits are scanned continuously unless an overrange condition occurs. In an overrange condition all digit drives are held low from the final STROBE pulse until the beginning of the next reference integrate phase. The scanning sequence is then repeated. This provides a blinking visual display indication.

BCD Data Outputs (Pins 13, 14, 15 and 16)

The binary coded decimal bits B_8, B_4, B_2, B_1 are positive true logic signals. The data bits become active simultaneously with the digit drive signals. In an overrange condition all data bits are at a logic "0" state.

Applications Information

Component Value Selection

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. A 20 μA drive current gives negligible linearity errors. Values of 5 to 40 μA give good results. The exact value of integrating resistor for a 20 μA current is easily calculated.

$$R_{INT} = \frac{\text{full-scale voltage}}{20\ \mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). For ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt full scale integrator swing is adequate. A 0.10 μF to 0.47 μF is recommended. In general, the value of C_{INT} is given by:

$$C_{INT} = \frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{Integrator output voltage swing}}$$

$$= \frac{(10{,}000)\ (\text{clock period})\ (20\mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half scale 0.9999. Any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. A large capacitor reduces the noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Smaller or cheaper caps can be used if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made. Suitable references are:

Part Type	Manufacturer
TSC9491	Teledyne Semiconductor
MC1400U2	Motorola

Conversion Timing

Line Frequency Rejection

A signal integration period at a multiple of the 60 Hz line frequency will maximize 60 Hz "line noise" rejection.

A 100 kHz clock frequency will reject both 50 Hz, 60 Hz and 400 Hz noise. This corresponds to 2.5 readings per second.

Oscillator Frequency	Frequency Rejected
300 kHz, 200 kHz, 150 kHz, 120 kHz, 100 kHz, 40 kHz, 33 1/3 kHz	60 Hz
250 kHz, 166 2/3 kHz, 125 kHz, 100 kHz	50 Hz
100 kHz	50 Hz, 60 Hz, 400 Hz

Conversion Rate vs Clock Frequency

Oscillator Frequency (kHz)	Conversion Rate (Conv/Sec)
100	2.5
120	3
200	5
300	7.5
400	10
800	20
1,200	30

Power Supplies and Grounds

Power Supplies

The TSC7135 is designed to work from ±5 V supplies. The conditions to use a single +5 V supply are:

- The input signal is referenced to the center of the common mode range of the converter.
- The signal is less than ±1.5 volts.

Grounding

Systems should use separate digital and analog ground systems to avoid loss of accuracy.

Displays and Driver Circuits

Teledyne Semiconductor manufactures three display decoder/driver circuits to interface the TSC7135 to LCD or LED displays. Each driver has 28 outputs for driving four seven segment digit displays. The TSC700A features increased LED segment drive current for greater display brightness.

Device	Package	Description
TSC7211AIPL	40 Pin Epoxy	4 Digit LCD Driver/Decoder
TSC7212AIPL	40 Pin Epoxy	4 Digit LED Driver/Decoder
TSC700AIJL	40 Pin CerDIP	4 Digit LED Driver/Decoder with high LED Segment Current ($I_{SEG} \geq 11$ mA)

Several sources exist for LCD and LED displays:

Manufacturer	Address	Display Type
Hewlett Packard Components	640 Page Mill Rd Palo Alto, CA 94304	LED
Litronix, Inc.	19000 Homestead Rd. Cupertino, CA 94010	LED
And	770 Airport Blvd. Burlingame, CA 94010	LCD and LED
Epson America, Inc.	3415 Kanhi Kawa St. Torrence, CA 90505	LCD

High Speed Operation

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3 μs delay, and at a clock frequency of 160 kHz (6 μs period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50 μV input, 1 to 2 with 150 μV, 2 to 3 at 250 μV, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160 kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many-dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to ~1 MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 160 kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant non-linearities in the first few counts of the instrument.

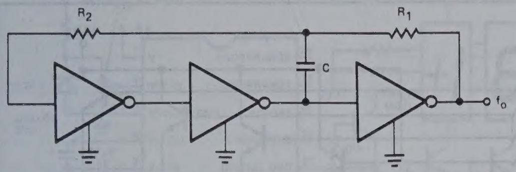
The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of the reference integrate (de-integrate) phase. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of auto-zero gives an overload display of 0000 instead of 0001. No delay occurs during signal integrate, so that true ratiometric readings result.

Application Circuits



Gates are 74C04

1. $f_O \approx \dfrac{1}{2\,C[0.41\,R_P + 0.70\,R_1]}$, $R_P = \dfrac{R_1\,R_2}{R_1 + R_2}$

   a. If $R_1 = R_2 = R_1$, $f \cong 0.55/RC$

   b. If $R_2 >> R_1$, $f \cong 0.45/R_1C$

   c. If $R_2 << R_1$, $f \cong 0.72/R_1C$

   a. f = 120 kHz, C = 420 pF
   $R_1 = R_2 \approx 10.9$ k Ω

   b. f = 120 kHz, C = 420 pF, $R_2 = 50$ k Ω
   $R_1 = 8.93$ k Ω

   c. f = 120 kHz, C = 220 pF, $R_2 = 5$ k Ω
   $R_1 = 27.3$ k Ω

Figure A: R/C Oscillator

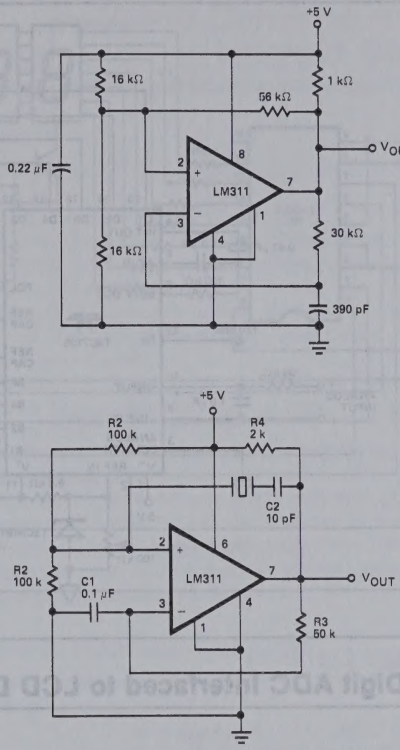
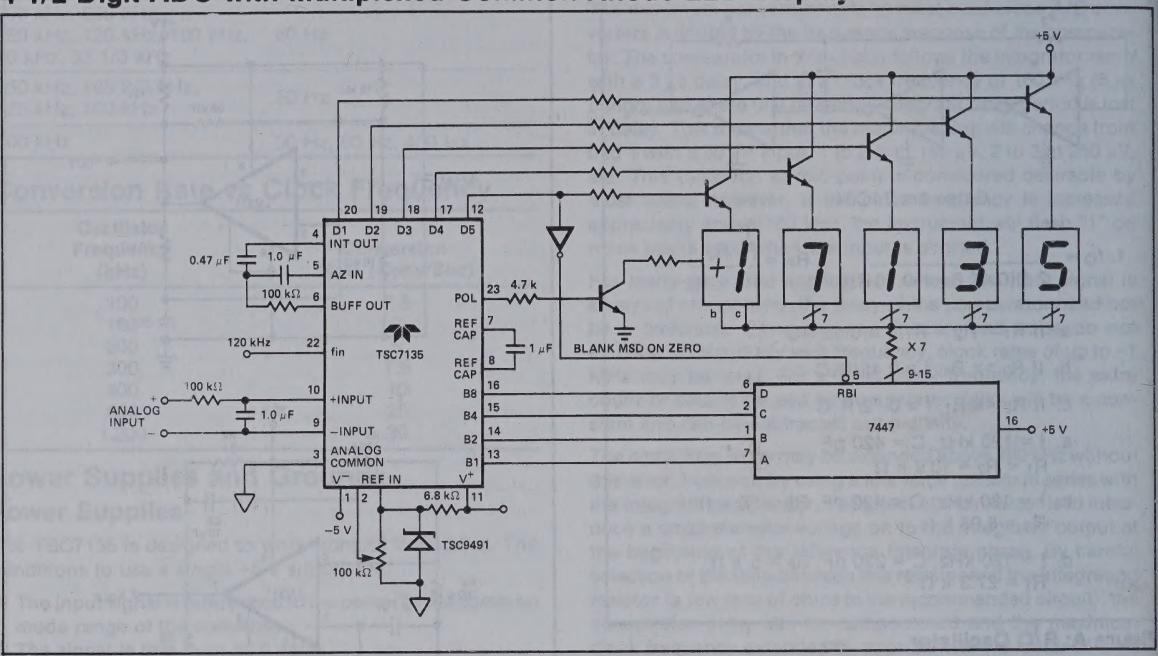
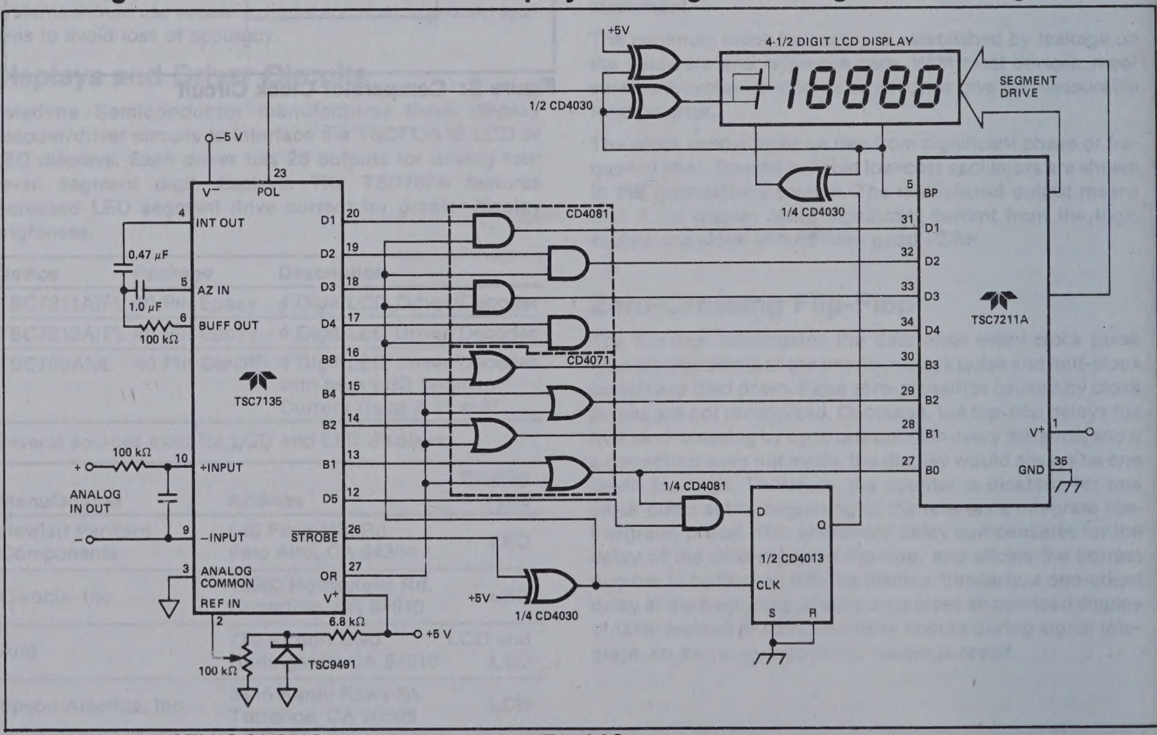

+5 V
16 kΩ
1 kΩ
56 kΩ
VOUT
0.22 µF
2
8
LM311
7
3
1
4
16 kΩ
30 kΩ
390 pF
+5 V
R2
100 k
R4
2 k
C2
10 pF
2
6
R2
100 k
C1
0.1 µF
LM311
7
VOUT
3
4
1
R3
50 k

Figure B: Comparator Clock Circuit

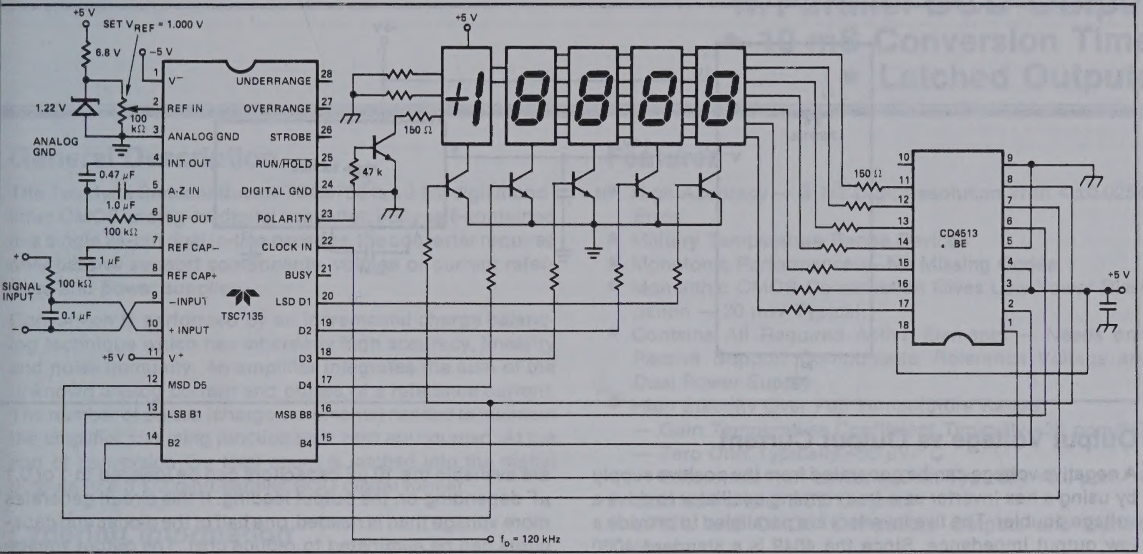
4 1/2 Digit ADC with Multiplexed Common Anode LED Display


+5 V
20
19
18
17
12
D1
D2
D3
D4
D5
4
INT OUT
0.47 µF
1.0 µF
5
AZ IN
100 kΩ
6
BUFF OUT
POL
23
4.7 k
REF CAP
7
1 µF
REF CAP
8
120 kHz
22
fin
TSC7135
100 kΩ
10
+INPUT
ANALOG INPUT
1.0 µF
9
−INPUT
3
ANALOG COMMON
B8
16
B4
15
B2
14
B1
13
V−
REF IN
V+
1
2
11
6.8 kΩ
−5 V
TSC9491
100 kΩ
+
1
7
1
3
5
b
c
7
7
7
7
X 7
BLANK MSD ON ZERO
5
9-15
6
D
2
C
1
B
7
A
RBI
7447
16
+5 V

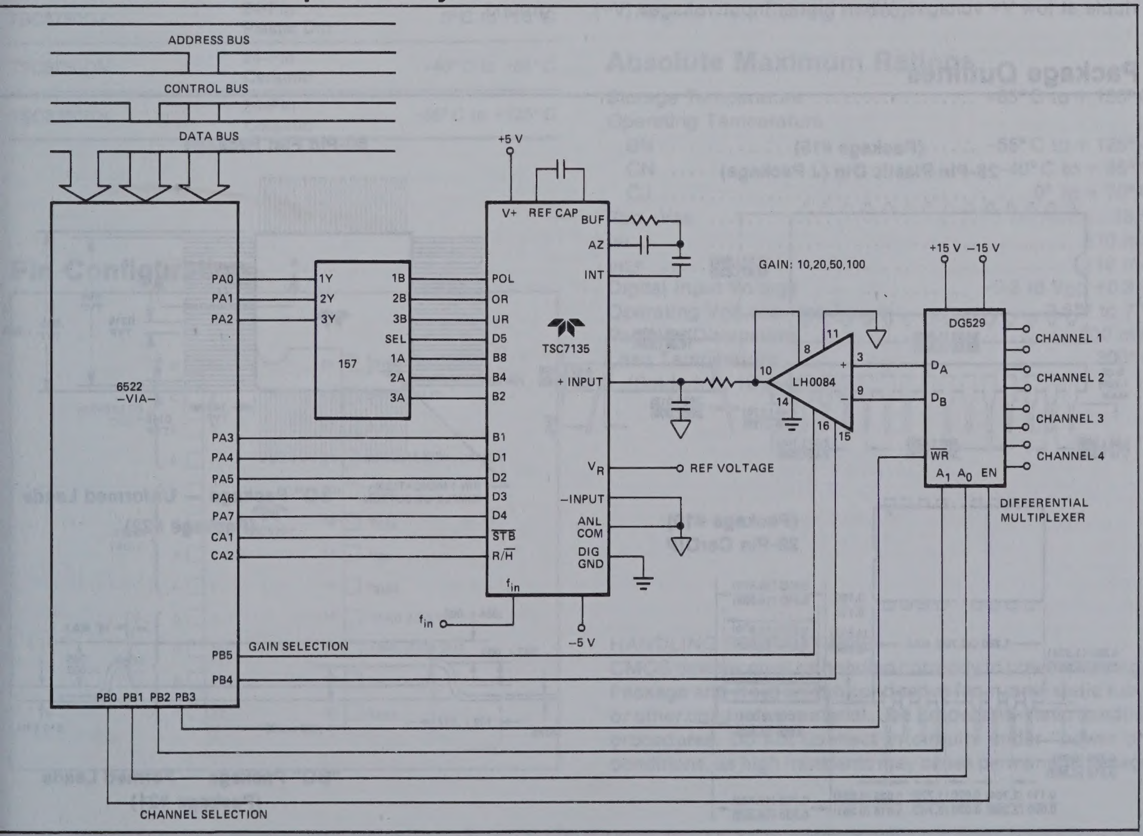
4 1/2 Digit ADC Interfaced to LCD Display with Digit Blanking on Overrange


+5V
4-1/2 DIGIT LCD DISPLAY
+18888
SEGMENT DRIVE
1/2 CD4030
−5 V
23
V−
POL
4
INT OUT
D1
20
CD4081
0.47 µF
D2
19
5
AZ IN
D3
18
1.0 µF
6
BUFF OUT
D4
17
100 kΩ
B8
16
CD4071
TSC7135
B4
15
B2
14
100 kΩ
10
+INPUT
B1
13
ANALOG IN OUT
D5
12
9
−INPUT
STROBE
26
3
ANALOG COMMON
OR
27
REF IN
V+
2
6.8 kΩ
+5 V
100 kΩ
TSC9491
+5V
1/4 CD4030
1/4 CD4081
D
Q
1/2 CD4013
CLK
S
R
1/4 CD4030
5
BP
31
D1
32
D2
33
D3
TSC7211A
34
D4
30
B3
29
B2
28
B1
1
V+
27
B0
35
GND

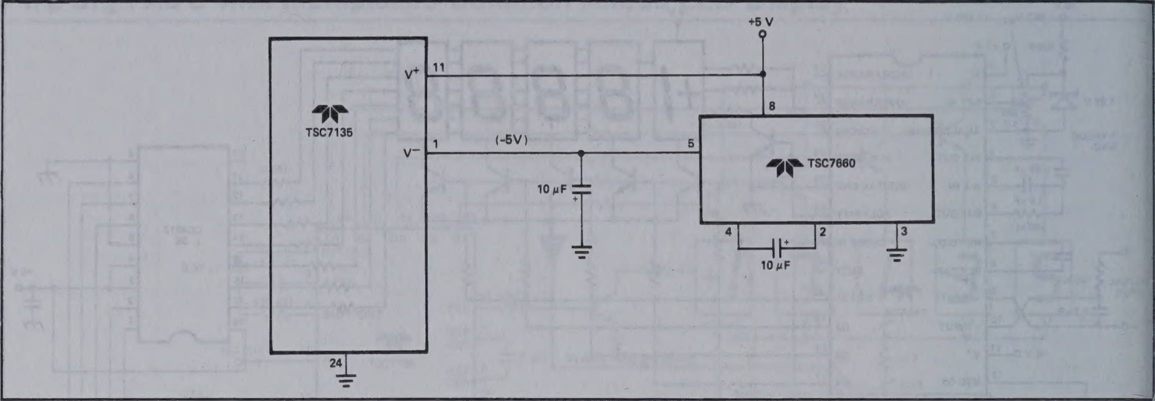
4 1/2 Digit ADC with Multiplexed Common Cathode LED Display


+5 V
SET V_{REF} = 1.000 V
6.8 V
−5 V
1.22 V
100 kΩ
ANALOG GND
0.47 μF
1.0 μF
100 kΩ
1 μF
SIGNAL INPUT
100 kΩ
0.1 μF
+5 V
1 V⁻
2 REF IN
3 ANALOG GND
4 INT OUT
5 A-Z IN
6 BUF OUT
7 REF CAP−
8 REF CAP+
9 −INPUT
10 + INPUT
11 V⁺
12 MSD D5
13 LSB B1
14 B2
UNDERRANGE 28
OVERRANGE 27
STROBE 26
RUN/HOLD 25
DIGITAL GND 24
POLARITY 23
CLOCK IN 22
BUSY 21
LSD D1 20
D2 19
D3 18
D4 17
MSB B8 16
B4 15
TSC7135
+5 V
150 Ω
47 k
+18888
150 Ω
CD4513 BE
+5 V
f_o = 120 kHz

Four Channel Data Acquisition System


ADDRESS BUS
CONTROL BUS
DATA BUS
6522 −VIA−
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
CA1
CA2
PB5
PB4
PB0 PB1 PB2 PB3
1Y 2Y 3Y
1B 2B 3B SEL 1A 2A 3A
157
+5 V
V+ REF CAP
BUF
AZ
INT
POL
OR
UR
D5
B8
B4
B2
B1
D1
D2
D3
D4
STB
R/H̄
TSC7135
+ INPUT
V_R
−INPUT
ANL COM
DIG GND
f_{in}
f_{in}
−5 V
REF VOLTAGE
GAIN: 10,20,50,100
LH0084
+15 V −15 V
DG529
D_A
D_B
W̄R̄
A_1 A_0 EN
CHANNEL 1
CHANNEL 2
CHANNEL 3
CHANNEL 4
DIFFERENTIAL MULTIPLEXER
GAIN SELECTION
CHANNEL SELECTION

Negative Supply Voltage Generator

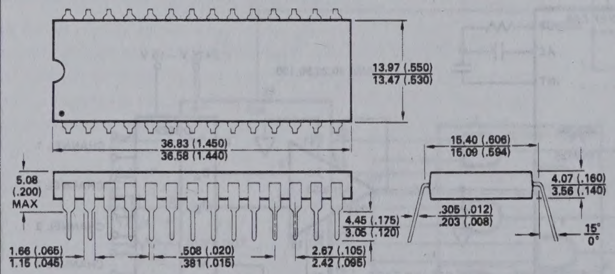

+5 V
V+
11
TSC7135
V−
1
(-5V)
5
8
TSC7660
10 µF
+
4
2
3
10 µF
24

Output Voltage vs Output Current

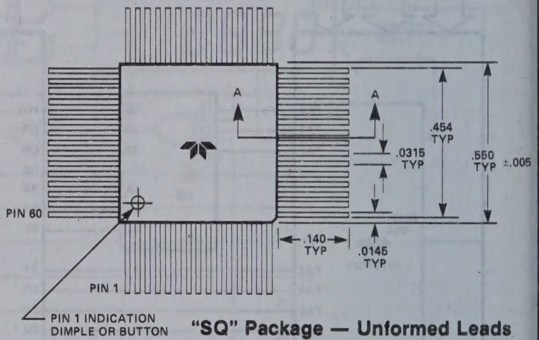
A negative voltage can be generated from the positive supply by using a hex inverter as a free running oscillator to drive a voltage doubler. The five inverters are paralleled to provide a low output impedance. Since the 4049 is a standard 4000 CMOS part, the circuit can be operated from 3 to 15 volts. The 10 μF capacitors were used in order to minimize output ripple at low V+ voltages. When higher input voltages (V+) are available the 10 μF capacitors can be lowered to 1 or 0.1 μF depending on the output loading. If this circuit generates more voltage than is needed, one half of the diodes and capacitors can be eliminated to reduce cost. The output voltage will then be one-half of that shown in the graph and is available on the negative side of the 10 μF capacitor connected to ground.

Package Outlines

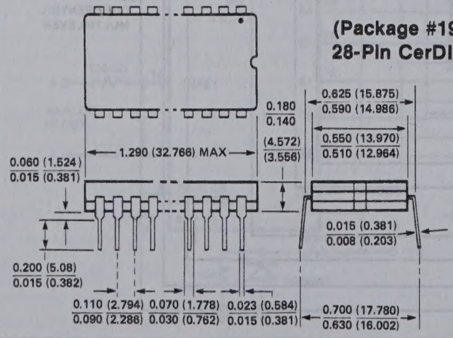
(Package #15)
28-Pin Plastic Dip (J Package)


13.97 (.550)
13.47 (.530)
36.83 (1.450)
36.58 (1.440)
15.40 (.606)
15.09 (.594)
5.08
(.200)
MAX
4.07 (.160)
3.56 (.140)
.305 (.012)
.203 (.008)
4.45 (.175)
3.05 (.120)
15°
0°
1.66 (.065)
1.15 (.045)
.508 (.020)
.381 (.015)
2.67 (.105)
2.42 (.095)

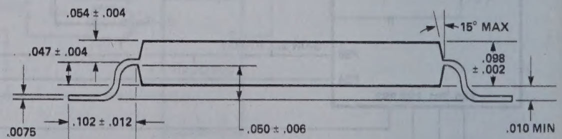
60-Pin Flat Package


A
A
.454
TYP
.0315
TYP
.550
TYP ±.005
PIN 60
.140
TYP
.0145
TYP
PIN 1
PIN 1 INDICATION
DIMPLE OR BUTTON

"SQ" Package — Unformed Leads
(Package #22)


0.180
0.140
(4.572)
(3.556)
0.625 (15.875)
0.590 (14.986)
0.550 (13.970)
0.510 (12.964)
1.290 (32.766) MAX
0.060 (1.524)
0.015 (0.381)
0.015 (0.381)
0.008 (0.203)
0.200 (5.08)
0.015 (0.382)
0.110 (2.794)
0.090 (2.286)
0.070 (1.778)
0.030 (0.762)
0.023 (0.584)
0.015 (0.381)
0.700 (17.780)
0.630 (16.002)

(Package #19)
28-Pin CerDIP


.054 ± .004
.047 ± .004
15° MAX
.098
± .002
.0075
.102 ± .012
.050 ± .006
.010 MIN

"BQ" Package — Formed Leads
(Package #21)

TELEDYNE SEMICONDUCTOR

TSC8750
3 1/2 Digit ADC w/Parallel BCD Output
• 10 mS Conversion Time • Latched Outputs

General Description

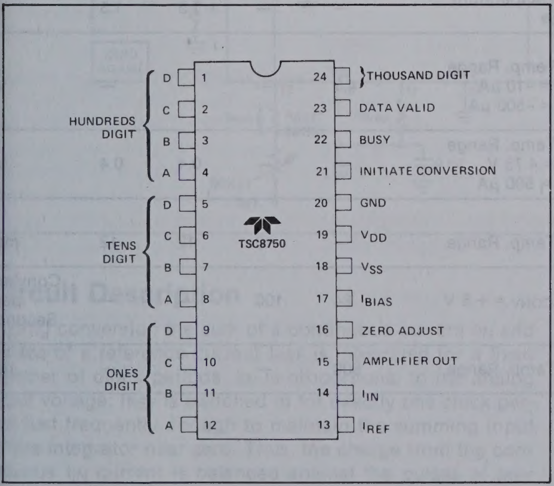
The Teledyne Semiconductor TSC8750 is a 3 1/2 digit monolithic CMOS analog-to-digital converter. Fully self-contained in a single 24-pin dual in-line package, the converter requires only passive support components, voltage or current reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current. The number of pulses (charge increments) needed to maintain the amplifier summing junction near zero are counted. At the end of conversion the total count is latched into the digital outputs in a 3 1/2 digit parallel BCD digital format.

Ordering Information

Part No.	Package	Temperature Range
TSC8750CJ	24-Pin Plastic Dip	0° C to +70° C
TSC8750CN	24-Pin Ceramic	-40° C to +85° C
TSC8750BN	24-Pin Ceramic	-55° C to +125° C

Pin Configuration



Features

- High Accuracy — 3 1/2 Digit Resolution With < ±0.025% Error
- Military Temperature Range Devices
- Monotonic Performance — No Missing Codes
- Monolithic CMOS Construction Gives Low Power Dissipation — 20 mW Typical
- Contains All Required Active Elements — Needs only Passive Support Components, Reference Voltage and Dual Power Supply
- High Stability Over Full Temperature Range
  - — Gain Temperature Coefficient Typically <25 ppm/° C
  - — Zero Drift Typically <30 μV/° C
  - — Differential Non-Linearity Drift Typically <2.5 ppm/° C
- Latched Parallel BCD Outputs
- LPTTL and CMOS Compatible Outputs and Control Inputs
- Strobed or Free Running Conversion
- Infinite Input Range — Any Positive Voltage Can Be Applied Via a Scaling Resistor

Absolute Maximum Ratings

Storage Temperature	-65° C to + 150° C
Operating Temperature	
BN	-55° C to + 125° C
CN	-40° C to + 85° C
CJ	0° to + 70° C
$V_{DD} - V_{SS}$	18 V
I_{IN}	±10 mA
I_{REF}	±10 mA
Digital Input Voltage	-0.3 to V_{DD} +0.3 V
Operating V_{DD} and V_{SS} Range	3.5 V to 7 V
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300° C

HANDLING PRECAUTIONS

CMOS devices must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

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Electrical Characteristics Unless otherwise specified, $V_{DD}=+5$ V, $V_{SS}=-5$ V, $V_{GND}=0$, $V_{REF}=-6.4$ V, $R_{BIAS}=100$ kΩ, test circuit shown. $T_A=25°$C unless Full Temperature Range is specified. (-55° C to +125° C for BN, -40° C to +85° C for CN package, 0° to 70° C for CJ package.)

PARAMETER	DEFINITION	CONDITIONS	MIN	TYP	CJ/CL MAX	BL MAX	UNITS
Accuracy							
Resolution Accuracy	BCD Word Length Of Digital Output		3 1/2 (1999 Counts)	—	—	—	Digits
Relative Accuracy	Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input		—	—	0.025	0.025	%
Differential Non-Linearity	Deviation From 1 LSB Between Transition Points		—	—	—	0.025	0.025
Differential Non-Linearity Temperature Drift	Variation in Differential Non-Linearity Due To Temperature Change	Full Temperature Range	—	±2.5	±5	±5	ppm/° C
Gain Variance	Variation From Exact (Compensate By Trimming R_{IN} or R_{REF})		—	±2	±5	±5	% of Nominal
Gain Temperature Drift	Variation In A Due To Temperature Change	Full Temperature Range	—	±25	±75	±80	ppm/° C
Zero Offset	Correction at Zero Adjust to Give Zero Output When Input Is Zero	$I_{IN}=0$	—	±10	±50	±50	mV
Zero Temperature Drift	Variation in Zero Offest Due to Temperature Change	Full Temperature Range	—	±3	±5	±8	ppm/° C
Analog Inputs							
I_{IN} Full-Scale	Full-Scale Analog Input Current To Achieve Specified Accuracy		—	10	—	—	μA
I_{REF} (Note 1)	Reference Current Input To Achieve Specified Accuracy		—	-20	—	—	μA
Digital Inputs							
$V_{IN}^{(1)}$	Logical "1" Input Threshold For Initiate Conversion Input	Full Temperature Range	3.5	—	—	—	V
$V_{IN}^{(0)}$	Logical "0" Input Threshold For Initiate Conversion Input	Full Temperature Range	—	—	1.5	1.5	V
Digital Outputs							
$V_{OUT}^{(1)}$	Logical "1" Output Voltage For Digits Out, Busy, and Data Valid Outputs	Full Temp. Range $I_{OUT}=-10$ μA $I_{OUT}=-500$ μA	4.5	—	—	—	V
$V_{OUT}^{(0)}$	Logical "0" Output Voltage For Digits Out, Busy, and Data Valid Outputs	Full Temp. Range $V_{DD}=4.75$ V $I_{OUT}=500$ μA	—	—	0.4	0.4	V
Dynamic							
Conversion Time	Time Required to Perform One Complete A/D Conversion	Full Temp. Range	—	10	12	12	ms
Conversion Rate in Free-Run Mode		$V_{INT\ CONV}=+5$ V	84	100	—	—	Conv'ns per Second
Minimum Pulse Width for Initiate Conversion		Full Temp. Range	500	—	—	—	ns

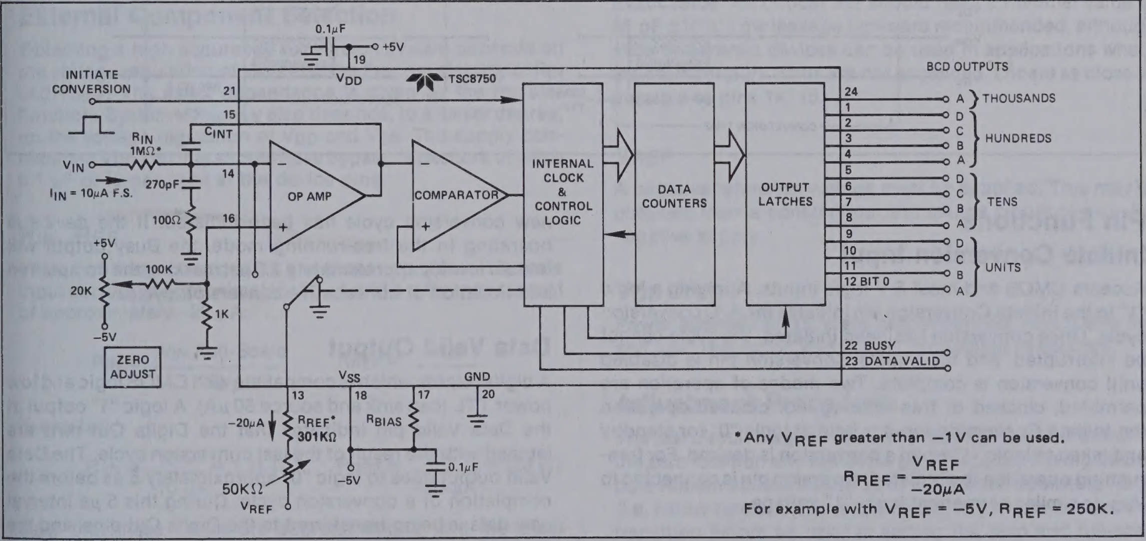
Electrical Characteristics

Unless otherwise specified, $V_{DD} = +5$ V, $V_{SS} = -5$ V, $V_{GND} = 0$, $V_{REF} = -6.4$ V, $R_{BIAS} = 100$ kΩ, test circuit shown. $T_A = 25°$C unless Full Temperature Range is specified. (-55° C to +125° C for BN, -40° C to +85° C for CN package, 0° to 70° C for CJ package.)

PARAMETER	DEFINITION	CONDITIONS	MIN	TYP	CJ/CL MAX	BL MAX	UNITS
Supply Current							
I_{DD} Quiescent (N Package)	Current Required From Positive Supply During Operation	Full Temp. Range	—	1.4	2.5	3.5	mA
(J Package)		$V_{INT\ CONV}$ = OV	—	1.4	5.0		mA
I_{SS} Quiescent (N Package)	Current Required From Negative Supply During Operation	Full Temp. Range	—	-1.6	-2.5	-3.5	mA
(J Package)		$V_{INIT\ CONV}$ = OV	—	-1.6	-5.0		mA
Supply Sensitivity	Change in Full-Scale Gain vs Supply Voltage Change	$V_{DD} \pm 1$V, $V_{SS} \pm 1$ V	—	±0.5	±1.0	±1.0	%/V
$\lvert V_{DD}\rvert = \lvert V_{SS}\rvert = 5$ V ± 1 V	Change in Full-Scale Gain vs Supply Voltage Change for Tracking Supplies		±0.05	±0.1	±0.1	±0.1	%/V

NOTE:
I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

Test Circuit


0.1µF
+5V
19
VDD
TSC8750
INITIATE CONVERSION
21
15
RIN 1MΩ*
CINT
VIN
IIN = 10µA F.S.
270pF
14
OP AMP
COMPARATOR
INTERNAL CLOCK & CONTROL LOGIC
DATA COUNTERS
OUTPUT LATCHES
BCD OUTPUTS
24 A THOUSANDS
1 D
2 C
3 B
4 A
HUNDREDS
5 D
6 C
7 B
8 A
TENS
9 D
10 C
11 B
12 BIT 0 A
UNITS
100Ω
16
+5V
100K
20K
1K
-5V
ZERO ADJUST
22 BUSY
23 DATA VALID
VSS
GND
13
18
17
20
-20µA
RREF* 301KΩ
RBIAS
0.1µF
-5V
50KΩ
VREF

*Any V_{REF} greater than −1V can be used.

$$R_{REF} = \frac{V_{REF}}{-20\mu A}$$

For example with $V_{REF} = -5$V, $R_{REF} = 250$K.

Circuit Description

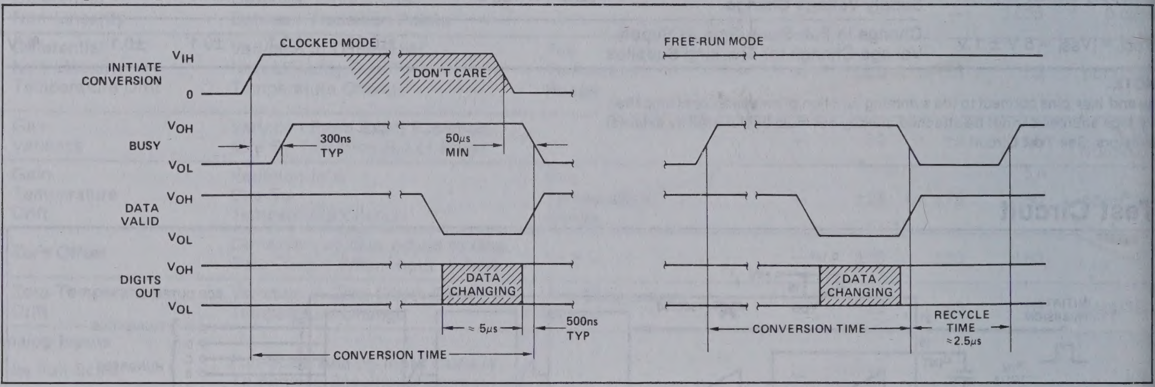
During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the summing input of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in BCD) is latched into the outputs at the end of conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine.

The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10 μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5 μs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

Timing Diagrams (Rise, fall times = 200 ns typ., C_L = 50 pF)



Pin Functions

Initiate Conversion Input

Accepts CMOS and most 5 V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500 μA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5 μs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low power TTL (can sink and source 50 μA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5 μs before the completion of a conversion cycle. During this 5 μs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out

(ones, tens, hundreds and thousand)

The BCD digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

Applications Information

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital Counts} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

$$A = 4128$$

where Digital Counts is the value of the BCD output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

Analog Input	Digital Output
$V_{IN} \leq$ Full-Scale	1100110011001
= Full-Scale –1 LSB	1100110011001
= 1 LSB	0 . . . 000 . . . 1
≤ 0	0 . . . 000 . . . 0

External Component Selection

Obtaining a high accuraccy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1 μF or larger right at the device pins.

R_{IN}, R_{EF}

Values of these components are chosen to give a full-scale input current of approximately 10 μA and a reference current of approximately -20 μA.

$$R_{IN} \cong \frac{V_{IN}\ \text{Full-Scale}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}$$

Examples:

$$R_{IN} \cong \frac{10\ V}{10\ \mu A} = 1\ M\ \Omega \qquad R_{REF} \cong \frac{-6.4\ V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} Full-Scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS}

Specifications for the TSC8750 are based on R_{BIAS} = 100 kΩ ±10% unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20 k the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When R_{BIAS} = 1 mΩ the conversion time will be six times longer, and the supply current is now reduced to .5 mA). For details of this relationship refer to AN-9 typical performance curves.

R_{DAMP}

Exact value not critical but should have a nominal value of 100 Ω ±10%. Locate close to pin 14.

C_{DAMP}

Exact value not critical but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT}

Exact value not critical but should have a nominal value of 68 pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15.

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of ±5 V are recommended, with 0.05% line and load regulation and 0.1 μF decoupling capacitors.

Adjustment Procedure

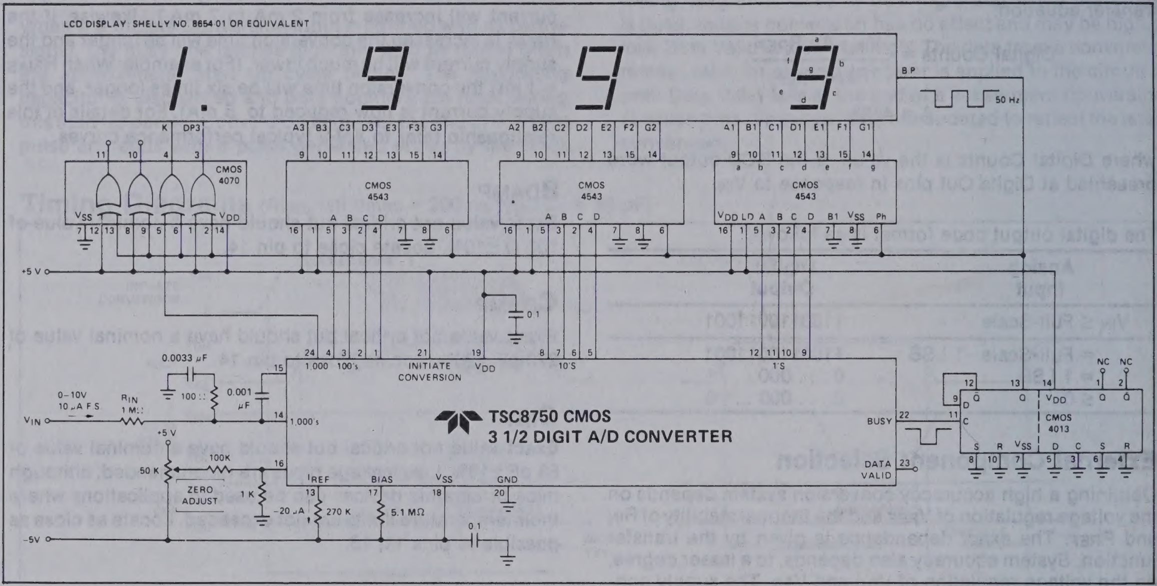
The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full-scale), it is recommended that transition points be used in setting the zero and full-scale values. Recommended procedure is as follows:

- Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
- Set V_{IN} to +1/2 LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
- For full-scale adjustment, set V_{IN} to the full-scale value less 1 1/2 LSB and trim the gain adjust circuit for a 1100110011000 to 1100110011001 transition.

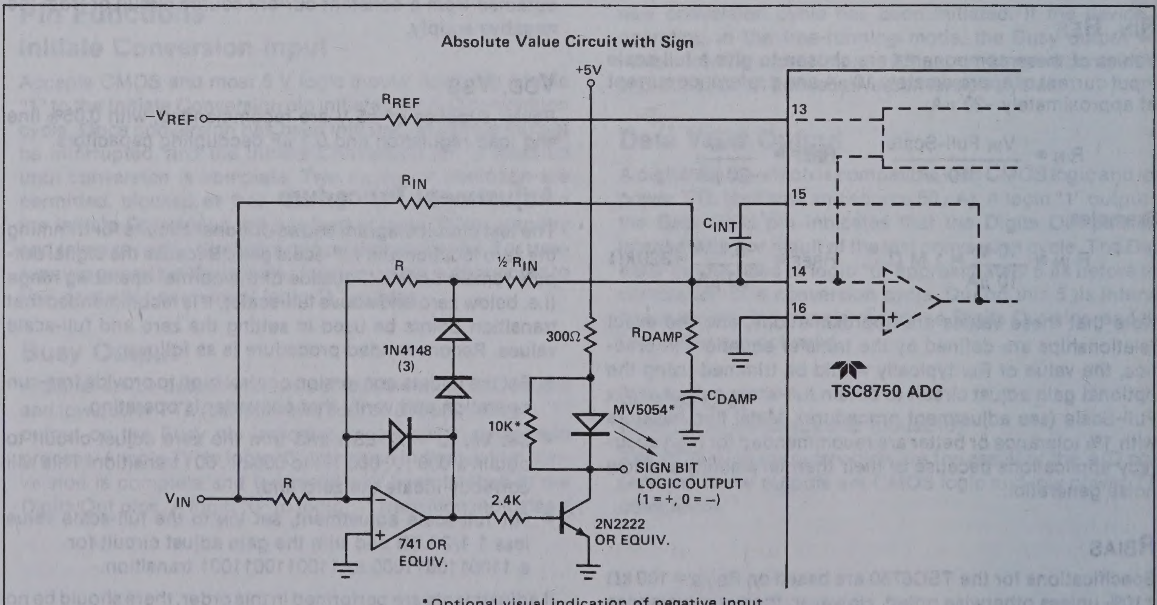
If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

Application/Design Circuits

3 1/2 Digit A/D with LCD Display


LCD DISPLAY: SHELLY NO. 8654-01 OR EQUIVALENT
BP
50 Hz
CMOS 4070
CMOS 4543
CMOS 4543
CMOS 4543
CMOS 4013
+5 V
-5 V
0.0033 µF
0.001 µF
0–10V
10 µA F.S.
RIN 1 MΩ
VIN
100 Ω
50 K
100K
ZERO ADJUST
1 K
-20 µA
270 K
5.1 MΩ
0.1
1,000
100's
INITIATE CONVERSION
VDD
10'S
1'S
1,000's
TSC8750 CMOS
3 1/2 DIGIT A/D CONVERTER
BUSY
DATA VALID
IREF
BIAS
VSS
GND
NC
NC

Bipolar Operation (+ and – inputs)

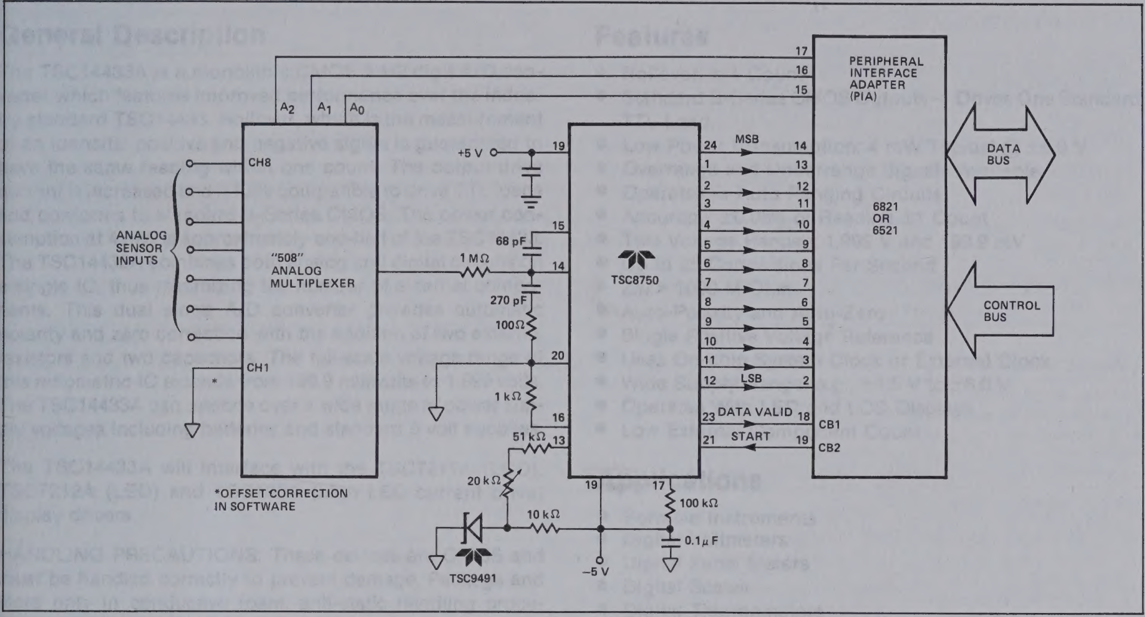

Absolute Value Circuit with Sign
+5V
–VREF
RREF
RIN
CINT
R
½ RIN
13
15
14
16
300Ω
RDAMP
1N4148 (3)
CDAMP
TSC8750 ADC
10K*
MV5054*
SIGN BIT LOGIC OUTPUT (1 = +, 0 = –)
VIN
R
2.4K
741 OR EQUIV.
2N2222 OR EQUIV.

*Optional visual indication of negative input
NOTE: Values for R should be between 10KΩ and 100KΩ

3 1/2 Digit ADC w/Parallel BCD Output

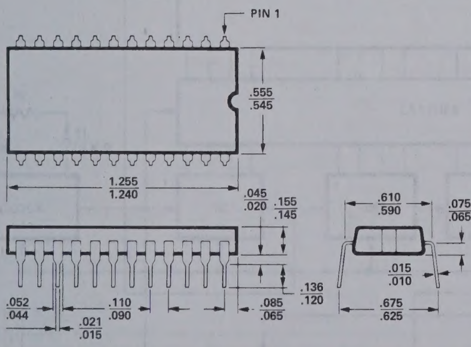
- **10 mS Conversion Time**
- **Latched Outputs**

Microprocessor-Based ADC System

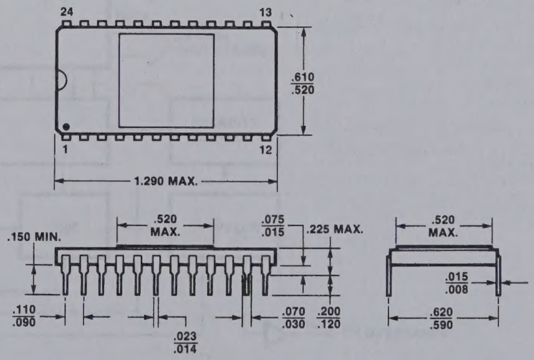

A2
A1
A0
CH8
ANALOG SENSOR INPUTS
"508" ANALOG MULTIPLEXER
CH1
*
*OFFSET CORRECTION IN SOFTWARE
+5 V
19
15
68 pF
1 MΩ
14
270 pF
100Ω
20
1 kΩ
16
51 kΩ
13
20 kΩ
10 kΩ
TSC9491
TSC8750
19
17
100 kΩ
0.1µF
−5 V
24
MSB
14
1
13
2
12
3
11
4
10
5
9
6
8
7
7
8
6
9
5
10
4
11
3
12
LSB
2
23
DATA VALID
18
21
START
19
17
16
15
PERIPHERAL INTERFACE ADAPTER (PIA)
6821 OR 6521
CB1
CB2
DATA BUS
CONTROL BUS

Package Information

(Package #12)
24-Pin Plastic Dip (J Package)


PIN 1
.555
.545
1.255
1.240
.045
.020
.155
.145
.610
.590
.075
.065
.015
.010
.136
.120
.052
.044
.110
.090
.021
.015
.085
.065
.675
.625

(Package #13)
24-Pin Ceramic Dip (N Package)


24
13
1
12
.610
.520
1.290 MAX.
.520 MAX.
.075
.015
.225 MAX.
.150 MIN.
.110
.090
.023
.014
.070
.030
.200
.120
.520 MAX.
.015
.008
.620
.590

TSC14433A
3 1/2 Digit ADC
• ±1 Count Rollover Error
• Low Power

General Description

The TSC14433A is a monolithic CMOS 3 1/2 digit A/D converter which features improved performance over the industry standard TSC14433. Rollover, which is the measurement of an idencital positive and negative signal is guaranteed to have the same reading within one count. The output drive current is increased and is fully compatible to drive TTL loads and conforms to standard B-Series CMOS. The power consumption at 4 mW is approximately one-half of the TSC14433. The TSC14433A combines both analog and digital circuits on a single IC, thus minimizing the number of external components. This dual slope A/D converter provides automatic polarity and zero correction with the addition of two external resistors and two capacitors. The full-scale voltage range of this ratiometric IC extends from 199.9 millivolts to 1.999 volts. The TSC14433A can operate over a wide range of power supply voltages including batteries and standard 5 volt supplies.

The TSC14433A will interface with the TSC7211A (LCD), TSC7212A (LED) and TSC700A (high LED current drive) display drivers.

HANDLING PRECAUTIONS: These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

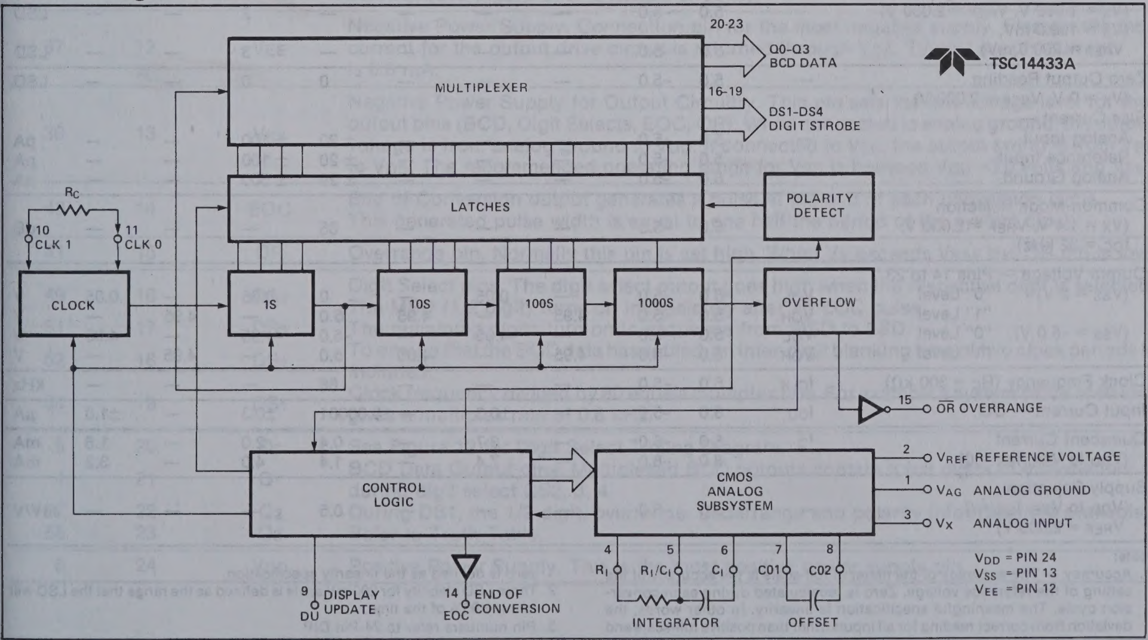
Features

- Rollover: ± 1 Count
- Standard B-Series CMOS Outputs — Drives One Standard TTL Load
- Low Power Consumption: 4 mW Typical @ ±5.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions Per Second
- $Z_{IN} > 1000$ M Ohm
- Auto-Polarity and Auto-Zero
- Single Positive Voltage Reference
- Uses On-chip System Clock or External Clock
- Wide Supply Range: e.g., ±4.5 V to ±8.0 V
- Operates With LED and LCD Displays
- Low External Component Count

Applications

- Portable Instruments
- Digital Voltmeters
- Digital Panel Meters
- Digital Scales
- Digital Thermometers
- Remote A/D Sensing Systems
- MPU Systems
- See Application Notes 19 and 21

Block Diagram


TSC14433A
MULTIPLEXER
20-23
Q0-Q3
BCD DATA
16-19
DS1-DS4
DIGIT STROBE
LATCHES
POLARITY DETECT
R_C
10
CLK 1
11
CLK 0
CLOCK
1S
10S
100S
1000S
OVERFLOW
15
OR OVERRANGE
CONTROL LOGIC
CMOS ANALOG SUBSYSTEM
2
V_{REF} REFERENCE VOLTAGE
1
V_{AG} ANALOG GROUND
3
V_X ANALOG INPUT
4
R_I
5
R_I/C_I
6
C_I
7
C01
8
C02
INTEGRATOR
OFFSET
V_{DD} = PIN 24
V_{SS} = PIN 13
V_{EE} = PIN 12
9
DISPLAY UPDATE
DU
14
END OF CONVERSION
EOC

Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD} to V_{EE}	-0.5 to +18 Vdc	Vdc
Voltage, Any Pin, Referenced V_{EE}	V	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain Per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

Recommended Operating Conditions

(V_{SS} = 0 or V_{EE})

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage —			
V_{DD} to Analog Ground	V_{DD}	+5.0 to +8.0	Vdc
V_{EE} to Analog Ground	V_{EE}	-2.8 to -8.0	
Clock Frequency	f_{CLK}	32 to 400	kHz
Zero Offset Correction Capacitor	C_O	0.1 ±20%	μF

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{EE} \leq (V_{IN}$ or $V_{OUT}) \leq V_{DD}$.

Electrical Characteristics:

(C_I = 0.1 μF mylar, R_I = 470 kΩ @ V_{REF} = 2.000 V, R_I = 27 kΩ @ V_{REF} = 200.0 mV. C_O = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1.)

		V_{DD}	V_{EE}	-40° C		25° C			85° C		
CHARACTERISTIC	SYMBOL	V_{dc}	V_{dc}	MIN	MAX	MIN	TYP	MAX	MIN	MAX	UNIT
Rollover Error (Difference in reading for equal positive and negative reading near Full-Scale) $-V_{IN} = +V_{IN}$: 200 mV Full-Scale	—			—	—	-1	—	+1	—	—	Cnts
Output Current — Pins 14 to 23											
(V_{SS} = 0V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	-5.0	-0.25	—	-0.2	-0.36	—	-0.16	—	mA
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	-5.0	1.6	—	1.6	3.2	—	1.6	—	mA
(V_{SS} = -5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	-5.0	-0.62	—	-0.5	-0.9	—	-0.35	—	mA
(V_{OL} = -4.5 V) Sink	I_{OL}	5.0	-5.0	1.6	—	1.6	5.50	—	1.6	—	mA
Linearity Output Reading (Note 1)	—										
(V_{REF} = 2.000 V)		5.0	-5.0	—	—	-0.05	+0.05	+0.05	—	—	%rdg
(V_{REF} = 200.0 mV)		5.0	-5.0	—	—	-1 count	—	+1 count	—	—	
Stability Output Reading (Note 2)	—										
(V_X = 1.990 V, V_{REF} = 2.000 V)		5.0	-5.0	—	—	—	—	2	—	—	LSD
(V_X = 199.0 mV, V_{REF} = 200.0 mV)		5.0	-5.0	—	—	—	—	3	—	—	LSD
Zero Output Reading (V_X = 0 V, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	0	0	—	—	LSD
Bias Current —											
Analog Input	—	5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Reference Input		5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Analog Ground		5.0	-5.0	—	—	—	± 20	± 500	—	—	pA
Common-Mode Rejection (V_X = 1.4 V, V_{REF} = 2.000 V, f_{OC} = 32 kHz)		5.0	-5.0	—	—	—	65	—	—	—	dB
Output Voltage — Pins 14 to 23											
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	-5.0	—	0.05	—	0	0.05	—	0.05	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
(V_{SS} = -5.0 V) "0" Level	V_{OL}	5.0	-5.0	—	-4.95	—	-5.0	-4.95	—	-4.95	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
Clock Frequency (R_C = 300 kΩ)	f_{CLK}	5.0	-5.0	—	—	—	66	—	—	—	kHz
Input Current — DU	I_{DU}	5.0	-5.0	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Quiescent Current (V_{DD} to V_{EE}, I_{SS} = 0)	I_Q	5.0	-5.0	—	3.7	—	0.4	2.0	—	1.6	mA
		8.0	-8.0	—	7.4	—	1.4	4.0	—	3.2	mA
Supply Rejection (V_{DD} to V_{EE}, I_{SS} = 0, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	0.5	—	—	—	mV/V

Note:

1. Accuracy — The accuracy of the meter at full-scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full-scale and zero is defined as the linearity specification.
2. Three LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.
3. Pin numbers refer to 24-Pin DIP.

Pin Description

PIN NO. 60-Pin FP	PIN NO. 24-Pin DIP	SYMBOL	DESCRIPTION
7	1	V_{AG}	This is the Analog Ground. It has a high input impedance. This pin determines the reference level for the unknown input voltage (V_X) and the reference voltage (V_{REF}).
10	2	V_{REF}	Reference voltage. Full-scale output is equal to the voltage applied to V_{REF}. Therefore, full-scale voltage of 1.999 V requires 2.000 V reference and 199.9 mV full-scale requires a 200 mV reference. V_{REF} functions as system reset, also. When switched to V_{EE} the system is reset to the beginning of the conversion cycle.
12	3	V_X	The Unknown Input Voltage (V_X) is measured as a ratio of the reference voltage (V_{REF}) in a ratio-metric A/D conversion.
19 22 24	4 5 6	R_1 R_1/C_1 C_1	These pins are for external components used for the integration function in the dual slope conversion. Typical values are 0.1 μF (mylar) capacitor for C_1. $R_1 = 470$ kΩ (resistor) for 2.0 V full-scale. $R_1 = 27$ kΩ (resistor) for 200 mV full-scale. Clock frequency of 66 kHz gives 250 ms conversion time. See equation below for calculation of integrator component values.
25 26	7 8	$C0_1$ $C0_2$	These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF.
27	9	DU	Display Update input pin. When DU is connected to the EOC output every conversion is displayed. New data will be strobed into the output latches during the conversion cycle if a positive edge is received on DU prior to the ramp-down cycle. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.
34 36	10 11	CLK_1 CLK_0	Clock input pins. The TSC14433 has its own oscillator system clock. Connecting a single resistor between CLK_1 and CLK_0 sets the clock frequency. A crystal or LC circuit may be inserted in lieu of a resistor for improved stability. CLK_1, the clock input, can be driven from an external clock source, which need only have standard CMOS output drive. This pin is referenced to V_{EE} for external clock inputs. A 300 kΩ resistor yields a clock frequency of about 66 kHz. (See typical characteristic curves). (See Figure 9 for alternate circuits).
37	12	V_{EE}	Negative Power Supply. Connection pin for the most negative supply. Please note the current for the output drive circuit is returned through V_{SS}. Typical supply current is 0.8 mA.
39	13	V_{SS}	Negative Power Supply for Output Circuitry. This pin sets the low voltage level for the output pins (BCD, Digit Selects, EOC, OR). When connected to analog ground, the output voltage is from analog ground to V_{DD}. If connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The recommended operating range for V_{SS} is between V_{DD} −3.0 volts and V_{EE}.
40	14	EOC	End of Conversion output generates a pulse at the end of each conversion cycle. This generated pulse width is equal to one half the period of the system clock.
41	15	OR	Overrange pin. Normally this pin is set high. When V_X exceeds V_{REF} the OR pin is low.
49 51 52 54	16 17 18 19	DS_4 DS_3 DS_2 DS_1	Digit Select pins. The digit select output goes high when the respective digit is selected. The MSD (1/2 digit) turns on immediately after an EOC pulse. The remaining digits turn on in sequence from MSD to LSD. To ensure that the BCD data has settled, an inter-digit blanking time of two clock periods is included. Clock frequency divided by 80 equals multiplex rate. For example a system clock of 66 kHz gives a multiplex rate of 0.8 kHz.
5 4 57 55	20 21 22 23	Q_0 Q_1 Q_2 Q_3	See Figure 12 for Digit Select Timing Diagram. BCD Data Output pins. Multiplexed BCD outputs contain 3 full digits of information during digit select DS2, 3, 4. During DS1, the 1/2 digit, overrange, underrange and polarity information is available. Refer to Truth Table.
6	24	V_{DD}	Positive Power Supply. This is the most positive power supply pin.

3 1/2 Digit ADC

- **Low Power**
- **±1 Count Rollover Error**

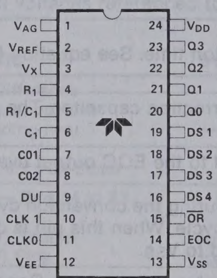
TSC14433A

Ordering Information

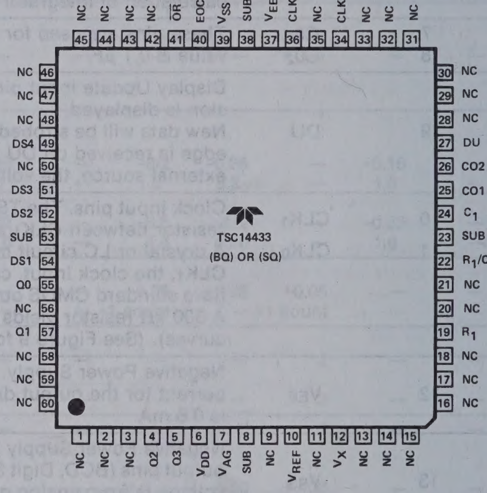
Part No.	Package	Temperature Range
TSC14433ACJ	24-Pin Plastic Dip	-40° C to +85° C
TSC14433ACL	24-Pin CerDIP	-40° C to +85° C
TSC14433ACBQ	60-Pin Plastic Flat Package: Formed Leads	-40° C to +85° C

Part No.	Package	Temperature Range
TSC14433ACSQ	60-Pin Plastic Flat Package: Unformed Leads	-40° C to +85° C
Devices with 160 Hour, +125° C Burn-In		
TSC14433ACJ/BI	24-Pin Plastic Dip	-40° C to +85° C
TSC14433ACL/BI	24-Pin CerDIP	-40° C to +85° C

Pin Configuration



V_AG 1
V_REF 2
V_X 3
R1 4
R1/C1 5
C1 6
C01 7
C02 8
DU 9
CLK 1 10
CLK0 11
V_EE 12
24 V_DD
23 Q3
22 Q2
21 Q1
20 Q0
19 DS 1
18 DS 2
17 DS 3
16 DS 4
15 OR
14 EOC
13 V_SS



45 NC
44 NC
43 NC
42 NC
41 OR
40 EOC
39 V_SS
38 SUB
37 V_EE
36 CLK 0
35 NC
34 CLK 1
33 NC
32 NC
31 NC
46 NC
47 NC
48 NC
49 DS4
50 NC
51 DS3
52 DS2
53 SUB
54 DS1
55 Q0
56 NC
57 Q1
58 NC
59 NC
60 NC
30 NC
29 NC
28 NC
27 DU
26 CO2
25 CO1
24 C1
23 SUB
22 R1/C1
21 NC
20 NC
19 R1
18 NC
17 NC
16 NC
1 NC
2 NC
3 NC
4 Q2
5 Q3
6 V_DD
7 V_AG
8 SUB
9 NC
10 V_REF
11 NC
12 V_X
13 NC
14 NC
15 NC
TSC14433
(BQ) OR (SQ)

$$R_1 = \frac{V_X(\max)}{C_1} \times \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X\ (\max) - 0.5$$

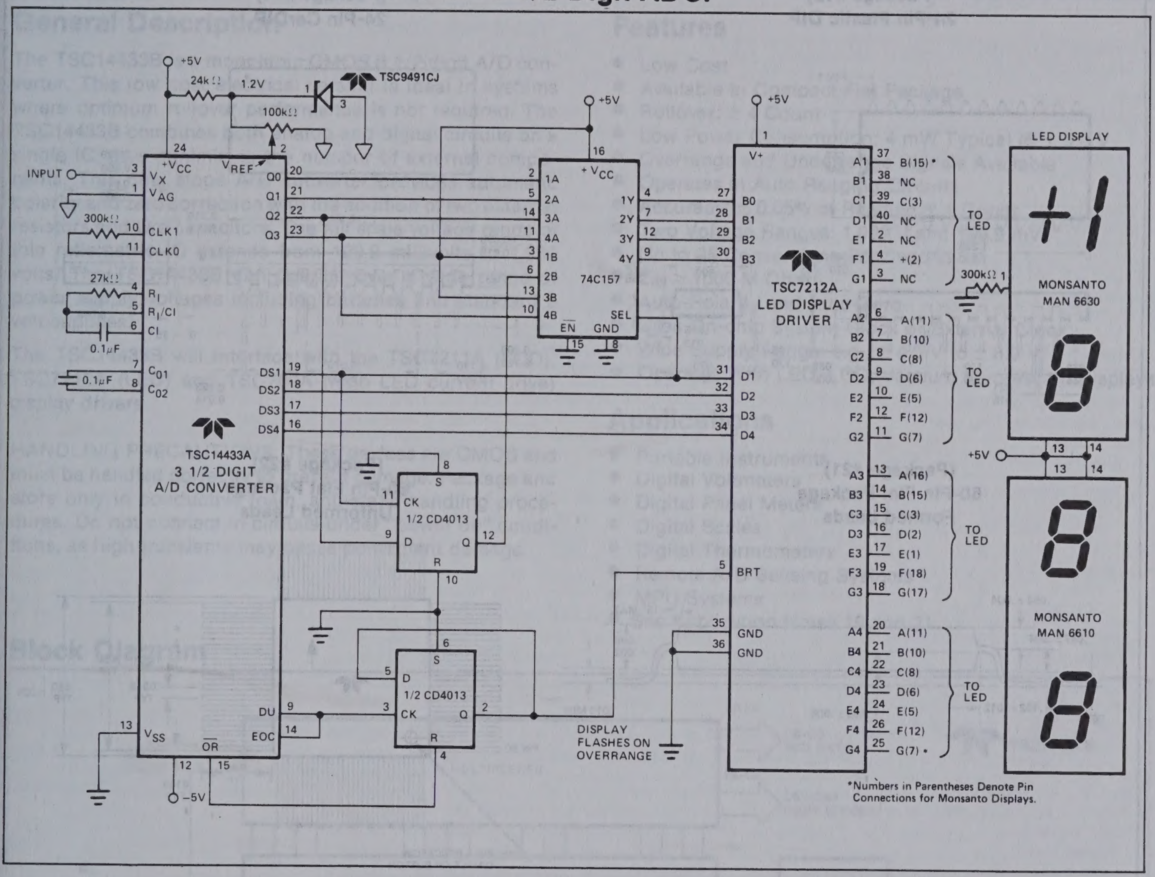
$$T = 4000 \times \frac{1}{f_{CLK}}$$

Where
R_1 is in kΩ
V_{DD} is the voltage at pin 24 referenced to V_{AG}
V_X is the voltage at pin 3 referenced to V_{AG}
f_{CLK} is the clock frequency at pin 10 in kHz

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Typical Applications

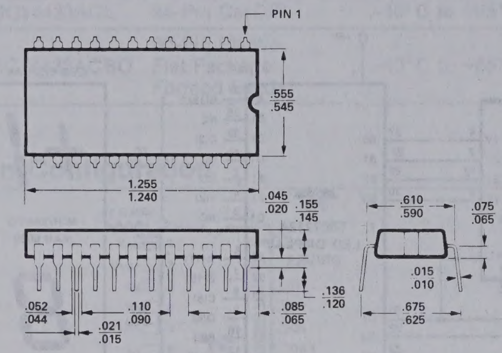
TSC7212A Interface to TSC14433A 3 1/2 Digit ADC.


+5V
24kΩ
1.2V
TSC9491CJ
100kΩ
INPUT
300kΩ
27kΩ
0.1µF
0.1µF
+VCC
VX
VAG
VREF
Q0
Q1
Q2
Q3
CLK1
CLK0
RI
RI/CI
CI
C01
C02
DS1
DS2
DS3
DS4
TSC14433A
3 1/2 DIGIT
A/D CONVERTER
DU
EOC
VSS
OR
−5V
74C157
1A
2A
3A
4A
1B
2B
3B
4B
1Y
2Y
3Y
4Y
EN
GND
SEL
1/2 CD4013
CK
D
Q
S
R
DISPLAY
FLASHES ON
OVERRANGE
V+
TSC7212A
LED DISPLAY
DRIVER
B0
B1
B2
B3
D1
D2
D3
D4
BRT
GND
A1
B1
C1
D1
E1
F1
G1
A2
B2
C2
D2
E2
F2
G2
A3
B3
C3
D3
E3
F3
G3
A4
B4
C4
D4
E4
F4
G4
B(15)*
NC
C(3)
+(2)
A(11)
B(10)
C(8)
D(6)
E(5)
F(12)
G(7)
A(16)
B(15)
D(2)
E(1)
F(18)
G(17)
G(7)*
TO LED
LED DISPLAY
300kΩ
MONSANTO
MAN 6630
MONSANTO
MAN 6610
+5V

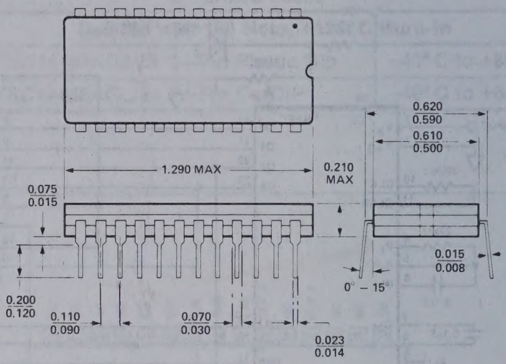
*Numbers in Parentheses Denote Pin Connections for Monsanto Displays.

Package Information

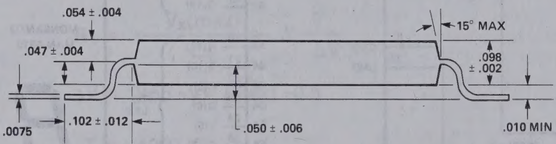
(Package #12)
24-Pin Plastic DIP


PIN 1
.555
.545
1.255
1.240
.045
.020
.155
.145
.610
.590
.075
.065
.015
.010
.136
.120
.052
.044
.110
.090
.021
.015
.085
.065
.675
.625

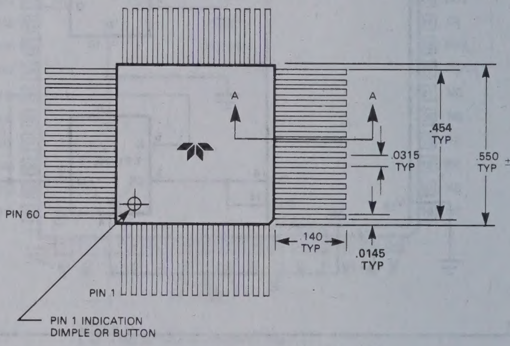
(Package #14)
24-Pin CerDIP


0.620
0.590
0.610
0.500
1.290 MAX
0.210
MAX
0.075
0.015
0.015
0.008
0° – 15°
0.200
0.120
0.110
0.090
0.070
0.030
0.023
0.014

(Package #21)
60-Pin Flat Package
Formed Leads


.054 ± .004
.047 ± .004
15° MAX
.098
± .002
.0075
.102 ± .012
.050 ± .006
.010 MIN

(Package #22)
60-Pin Flat Package
Unformed Leads


A
A
.454
TYP
.0315
TYP
.550
TYP ±.005
PIN 60
.140
TYP
.0145
TYP
PIN 1
PIN 1 INDICATION
DIMPLE OR BUTTON

TELEDYNE SEMICONDUCTOR

TSC14433B
3 1/2 Digit ADC
- Low Cost
- Multiplexed BCD Data
- ±4 Count Rollover Error

General Description

The TSC14433B is a monolithic CMOS 3 1/2 digit A/D converter. This low cost electrical version is ideal in systems where optimum rollover performance is not required. The TSC14433B combines both analog and digital circuits on a single IC, thus minimizing the number of external components. This dual slope A/D converter provides automatic polarity and zero correction with the addition of two external resistors and two capacitors. The full scale voltage range of this ratiometric IC extends from 199.9 millivolts to 1.999 volts. The TSC14433B can operate over a wide range of power supply voltages including batteries and standard 5 volt supplies.

The TSC14433B will interface with the TSC7211A (LCD), TSC7212A (LED) and TSC700A (high LED current drive) display drivers.

HANDLING PRECAUTIONS: These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

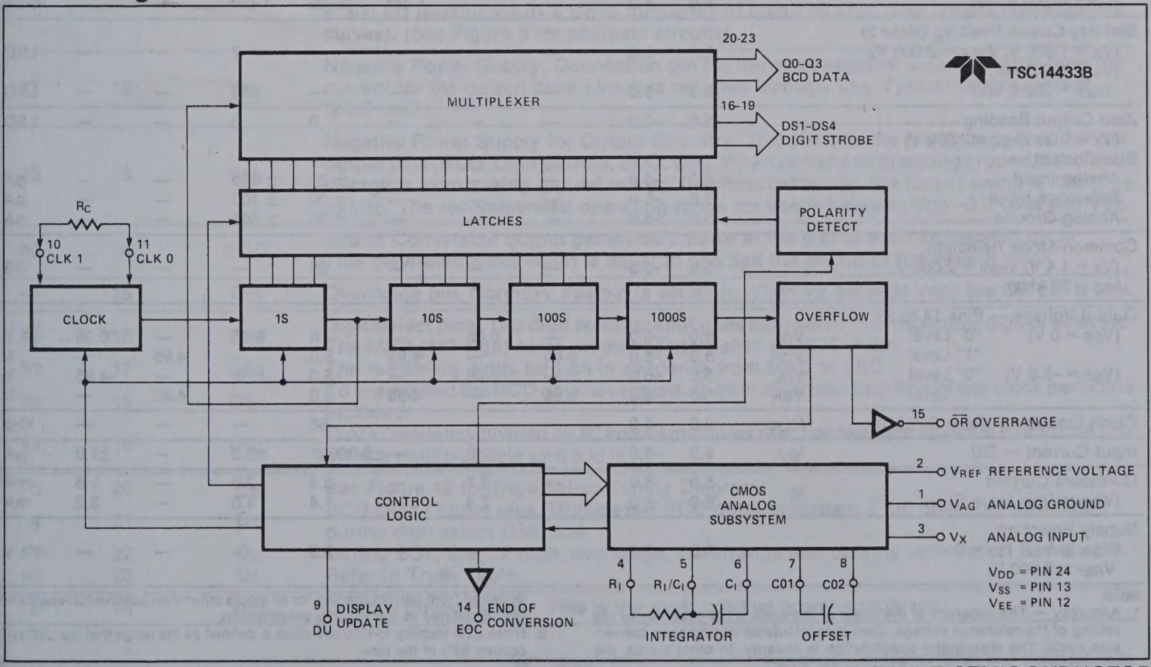
Features

- Low Cost
- Available in Compact Flat Package
- Rollover: ± 4 Count
- Low Power Consumption: 4 mW Typical @ ± 5.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Accuracy: ± 0.05% of Reading ± 1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions Per Second
- Z_{IN} > 1000 M Ohm
- Auto-Polarity and Auto-Zero
- Uses On-chip System Clock or External Clock
- Wide Supply Range: e.g., ± 4.5 V to ± 8.0 V
- Operates With LED, LCD, Vacuum Fluorescent Displays

Applications

- Portable Instruments
- Digital Voltmeters
- Digital Panel Meters
- Digital Scales
- Digital Thermometers
- Remote A/D Sensing Systems
- MPU Systems
- See Application Notes 19 and 21

Block Diagram


TSC14433B
MULTIPLEXER
20-23
Q0-Q3
BCD DATA
16-19
DS1-DS4
DIGIT STROBE
LATCHES
POLARITY DETECT
R_C
10
CLK 1
11
CLK 0
CLOCK
1S
10S
100S
1000S
OVERFLOW
15
$\overline{OR}$ OVERRANGE
CONTROL LOGIC
CMOS ANALOG SUBSYSTEM
2
V_{REF} REFERENCE VOLTAGE
1
V_{AG} ANALOG GROUND
3
V_X ANALOG INPUT
4
R_I
5
R_I/C_I
6
C_I
7
C01
8
C02
INTEGRATOR
OFFSET
9
DU
DISPLAY UPDATE
14
EOC
END OF CONVERSION
V_{DD} = PIN 24
V_{SS} = PIN 13
V_{EE} = PIN 12

Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD} to V_{EE}	-0.5 to +18 Vdc	Vdc
Voltage, Any Pin, Referenced V_{EE}	V	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain Per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

Recommended Operating Conditions

(V_{SS} = 0 or V_{EE})

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage —			
V_{DD} to Analog Ground	V_{DD}	+5.0 to +8.0	Vdc
V_{EE} to Analog Ground	V_{EE}	-2.8 to -8.0	
Clock Frequency	f_{CLK}	32 to 400	kHz
Zero Offset Correction Capacitor	C_O	0.1 ±20%	μF

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{EE} \leq (V_{IN}$ or $V_{OUT}) \leq V_{DD}$.

Electrical Characteristics: (C_I = 0.1 μF mylar, R_I = 470 kΩ @ V_{REF} = 2.000 V, R_I = 27 kΩ @ V_{REF} = 200.0 mV. C_O = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1.)

		V_{DD}	V_{EE}	-40°C		25°C			85°C		
CHARACTERISTIC	SYMBOL	Vdc	Vdc	MIN	MAX	MIN	TYP	MAX	MIN	MAX	UNIT
Rollover Error (Difference in reading for equal positive and negative reading near Full-Scale) $-V_{IN} = +V_{IN}$: 200 mV Full-Scale	—			—	—	-4	—	+4	—	—	counts
Output Current — Pins 14 to 23											
(V_{SS} = 0V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	-5.0	-0.25	—	-0.2	-0.36	—	-0.16	—	mA
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	-5.0	0.64	—	0.51	0.88	—	0.36	—	mA
(V_{SS} = -5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	-5.0	-0.52	—	-0.5	-0.9	—	-0.35	—	mA
(V_{OL} = -4.5 V) Sink	I_{OL}	5.0	-5.0	1.3	—	1.3	2.25	—	0.9	—	mA
Linearity Output Reading (Note 1)											
(V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	-0.05-		+0.05+	—	—	%rdg
(V_{REF} = 200.0 mV)		5.0	-5.0	—	—	1 cnt	±0.05	1 cnt	—	—	%rdg
Stability Output Reading (Note 2)											
(V_X = 1.990 V, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	—	2	—	—	LSD
(V_X = 199.0 mV, V_{REF} = 200.0 mV)		5.0	-5.0	—	—	—	—	3	—	—	LSD
Zero Output Reading (V_X = 0 V, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	0	0	—	—	LSD
Bias Current —											
Analog Input	—	5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Reference Input		5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Analog Ground		5.0	-5.0	—	—	—	± 20	± 500	—	—	pA
Common-Mode Rejection (V_X = 1.4 V, V_{REF} = 2.000 V, f_{OC} = 32 kHz)		5.0	-5.0	—	—	—	65	—	—	—	dB
Output Voltage — Pins 14 to 23											
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	-5.0	—	0.05	—	0	0.05	—	0.05	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
(V_{SS} = -5.0 V) "0" Level	V_{OL}	5.0	-5.0	—	-4.95	—	-5.0	-4.95	—	-4.95	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
Clock Frequency (R_C = 300 kΩ)	f_{CLK}	5.0	-5.0	—	—	—	66	—	—	—	kHz
Input Current — DU	I_{DU}	5.0	-5.0	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Quiescent Current (V_{DD} to V_{EE}, I_{SS} = 0)	I_Q	5.0	-5.0	—	3.7	—	0.4	2.0	—	1.6	mA
		8.0	-8.0	—	7.4	—	1.4	4.0	—	3.2	mA
Supply Rejection (V_{DD} to V_{EE}, I_{SS} = 0, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	0.5	—	—	—	mV/V

Note:

1. Accuracy — The accuracy of the meter at full-scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full-scale and zero is defined as the linearity specification.
2. Three LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.

Pin Description

PIN NO. 60-Pin FP	PIN NO. 24-Pin DIP	SYMBOL	DESCRIPTION
7	1	V_{AG}	This is the Analog Ground. It has a high input impedance. This pin determines the reference level for the unknown input voltage (V_X) and the reference voltage (V_{REF}).
10	2	V_{REF}	Reference voltage. Full-scale output is equal to the voltage applied to V_{REF}. Therefore, full-scale voltage of 1.999 V requires 2.000 V reference and 199.9 mV full-scale requires a 200 mV reference. V_{REF} functions as system reset, also. When switched to V_{EE} the system is reset to the beginning of the conversion cycle.
12	3	V_X	The Unknown Input Voltage (V_X) is measured as a ratio of the reference voltage (V_{REF}) in a ratio-metric A/D conversion.
19 22 24	4 5 6	R_1 R_1/C_1 C_1	These pins are for external components used for the integration function in the dual slope conversion. Typical values are 0.1 μF (mylar) capacitor for C_1. R_1 = 470 kΩ (resistor) for 2.0 V full-scale. R_1 = 27 kΩ (resistor) for 200 mV full-scale. Clock frequency of 66 kHz gives 250 ms conversion time. See equation below for calculation of integrator component values.
25 26	7 8	$C0_1$ $C0_2$	These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF.
27	9	DU	Display Update input pin. When DU is connected to the EOC output every conversion is displayed. New data will be strobed into the output latches during the conversion cycle if a positive edge is received on DU prior to the ramp-down cycle. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.
34 36	10 11	CLK_1 CLK_0	Clock input pins. The TSC14433 has its own oscillator system clock. Connecting a single resistor between CLK_1 and CLK_0 sets the clock frequency. A crystal or LC circuit may be inserted in lieu of a resistor for improved stability. CLK_1, the clock input, can be driven from an external clock source, which need only have standard CMOS output drive. This pin is referenced to V_{EE} for external clock inputs. A 300 kΩ resistor yields a clock frequency of about 66 kHz. (See typical characteristic curves). (See Figure 9 for alternate circuits).
37	12	V_{EE}	Negative Power Supply. Connection pin for the most negative supply. Please note the current for the output drive circuit is returned through V_{SS}. Typical supply current is 0.8 mA.
39	13	V_{SS}	Negative Power Supply for Output Circuitry. This pin sets the low voltage level for the output pins (BCD, Digit Selects, EOC, OR). When connected to analog ground, the output voltage is from analog ground to V_{DD}. If connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The recommended operating range for V_{SS} is between V_{DD} -3.0 volts and V_{EE}.
40	14	EOC	End of Conversion output generates a pulse at the end of each conversion cycle. This generated pulse width is equal to one half the period of the system clock.
41	15	OR	Overrange pin. Normally this pin is set high. When V_X exceeds V_{REF} the OR pin is low.
49 51 52 54	16 17 18 19	DS_4 DS_3 DS_2 DS_1	Digit Select pins. The digit select output goes high when the respective digit is selected. The MSD (1/2 digit) turns on immediately after an EOC pulse. The remaining digits turn on in sequence from MSD to LSD. To ensure that the BCD data has settled, an inter-digit blanking time of two clock periods is included. Clock frequency divided by 80 equals multiplex rate. For example a system clock of 66 kHz gives a multiplex rate of 0.8 kHz.
5 4 57 55	20 21 22 23	Q_0 Q_1 Q_2 Q_3	See Figure 12 for Digit Select Timing Diagram. BCD Data Output pins. Multiplexed BCD outputs contain 3 full digits of information during digit select DS2, 3, 4. During DS1, the 1/2 digit, overrange, underrange and polarity information is available. Refer to Truth Table.
6	24	V_{DD}	Positive Power Supply. This is the most positive power supply pin.

3 1/2 Digit CMOS

- Low Cost
- Multiplexed BCD Data
- ±4 Count Rollover Error

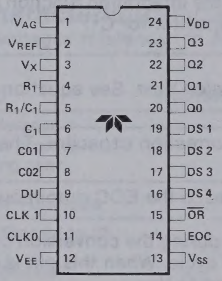
TSC14433B

Ordering Information

Part No.	Package	Temperature Range
TSC14433BCL	24-pin CerDIP	-40 to +85° C
TSC14433BCJ	24-pin Plastic Dip	-40 to +85° C
TSC14433BCBQ	60-Pin Plastic Flat Package: Formed Leads	-40 to +85° C

Part No.	Package	Temperature Range
TSC14433BCSQ	60-Pin Plastic Flat Package: Unformed Leads	-40 to +85° C

Pin Configuration

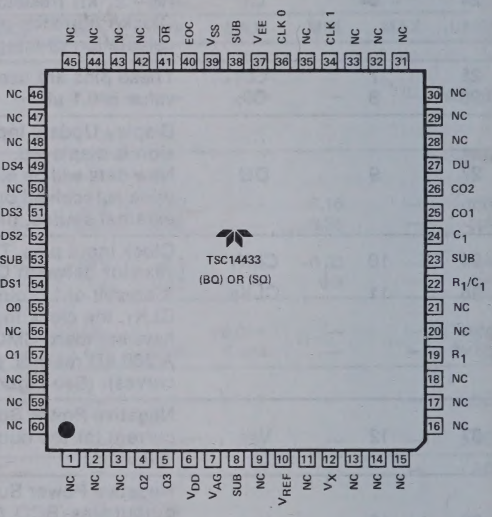

V_AG 1
V_REF 2
V_X 3
R_1 4
R_1/C_1 5
C_1 6
C01 7
C02 8
DU 9
CLK 1 10
CLK0 11
V_EE 12
24 V_DD
23 Q3
22 Q2
21 Q1
20 Q0
19 DS 1
18 DS 2
17 DS 3
16 DS 4
15 OR
14 EOC
13 V_SS

$$R_1 = \frac{V_X(max)}{C_1} \times \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X\ (max) - 0.5$$

$$T = 4000 \times \frac{1}{f_{CLK}}$$

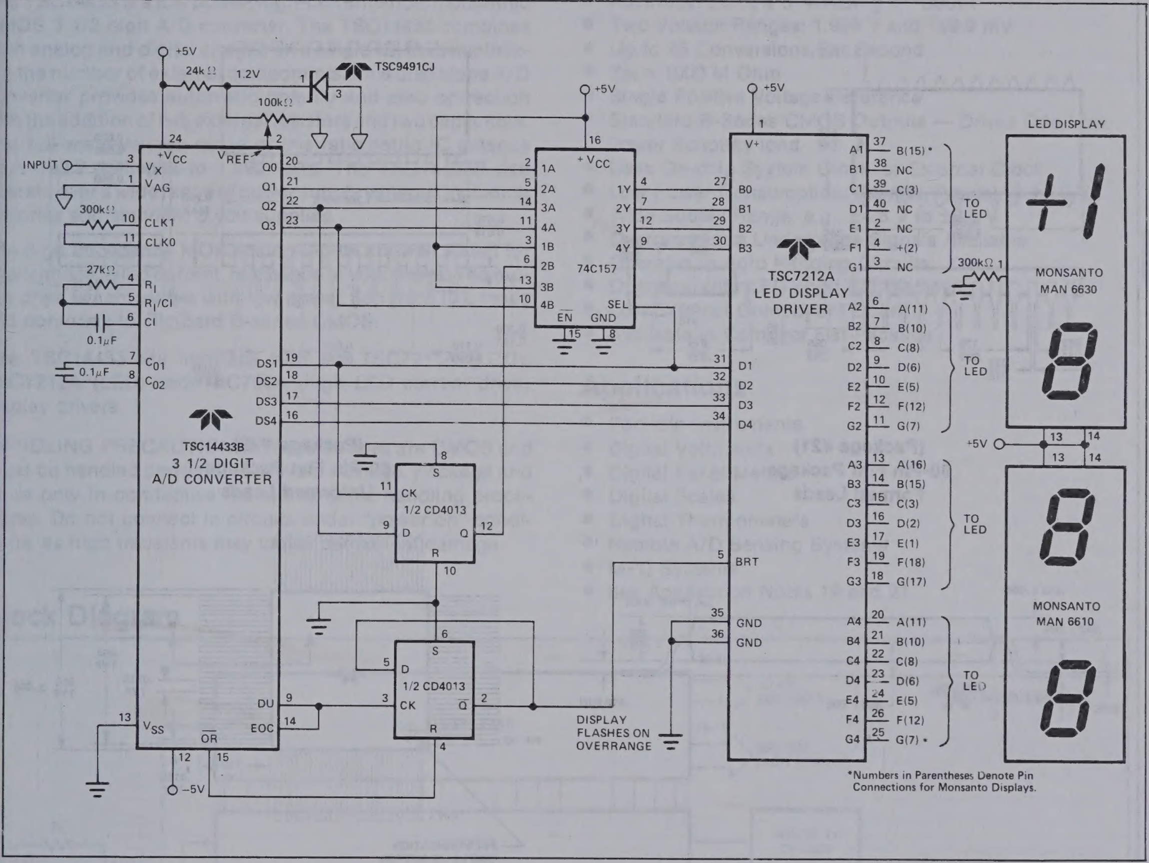
Where
R_1 is in kΩ
V_{DD} is the voltage at pin 24 referenced to V_{AG}
V_X is the voltage at pin 3 referenced to V_{AG}
f_{CLK} is the clock frequency at pin 10 in kHz


45 NC
44 NC
43 NC
42 NC
41 OR
40 EOC
39 V_SS
38 SUB
37 V_EE
36 CLK 0
35 NC
34 CLK 1
33 NC
32 NC
31 NC
46 NC
47 NC
48 NC
49 DS4
50 NC
51 DS3
52 DS2
53 SUB
54 DS1
55 Q0
56 NC
57 Q1
58 NC
59 NC
60 NC
30 NC
29 NC
28 NC
27 DU
26 CO2
25 CO1
24 C_1
23 SUB
22 R_1/C_1
21 NC
20 NC
19 R_1
18 NC
17 NC
16 NC
1 NC
2 NC
3 NC
4 Q2
5 Q3
6 V_DD
7 V_AG
8 SUB
9 NC
10 V_REF
11 NC
12 V_X
13 NC
14 NC
15 NC
TSC14433
(BQ) OR (SQ)

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

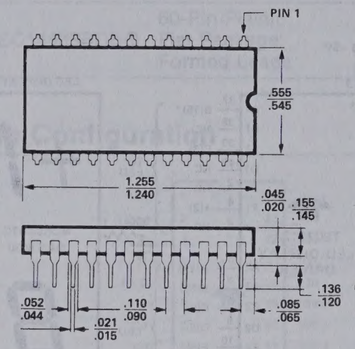
Typical Applications

TSC7212A Interface to TSC14433B 3 1/2 Digit ADC.

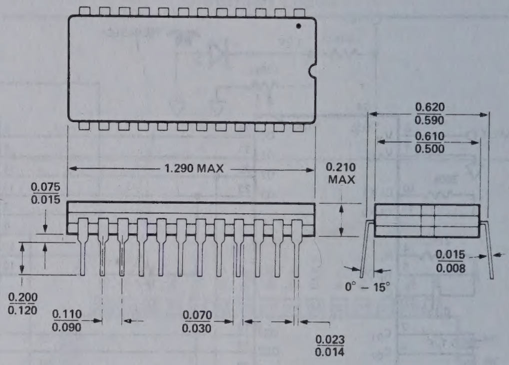

+5V
24kΩ
1.2V
TSC9491CJ
100kΩ
INPUT
300kΩ
27kΩ
0.1μF
0.1μF
+VCC
VREF
VX
VAG
CLK1
CLK0
RI
RI/CI
CI
C01
C02
Q0
Q1
Q2
Q3
DS1
DS2
DS3
DS4
TSC14433B
3 1/2 DIGIT
A/D CONVERTER
VSS
OR
DU
EOC
−5V
74C157
+VCC
1A
2A
3A
4A
1B
2B
3B
4B
1Y
2Y
3Y
4Y
EN
GND
SEL
1/2 CD4013
CK
S
D
Q
R
1/2 CD4013
DISPLAY
FLASHES ON
OVERRANGE
TSC7212A
LED DISPLAY
DRIVER
V+
B0
B1
B2
B3
D1
D2
D3
D4
BRT
GND
GND
A1 B1 C1 D1 E1 F1 G1
A2 B2 C2 D2 E2 F2 G2
A3 B3 C3 D3 E3 F3 G3
A4 B4 C4 D4 E4 F4 G4
B(15)*
NC
C(3)
NC
NC
+(2)
NC
A(11)
B(10)
C(8)
D(6)
E(5)
F(12)
G(7)
A(16)
B(15)
C(3)
D(2)
E(1)
F(18)
G(17)
A(11)
B(10)
C(8)
D(6)
E(5)
F(12)
G(7) •
TO LED
TO LED
TO LED
TO LED
LED DISPLAY
300kΩ
MONSANTO
MAN 6630
+5V
MONSANTO
MAN 6610
*Numbers in Parentheses Denote Pin Connections for Monsanto Displays.

Package Information

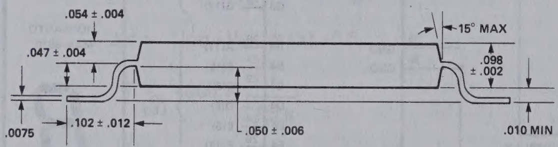
(Package #12)
24-Pin Plastic DIP


PIN 1
.555
.545
1.255
1.240
.045
.020
.155
.145
.610
.590
.075
.065
.015
.010
.136
.120
.052
.044
.110
.090
.021
.015
.085
.065
.675
.625

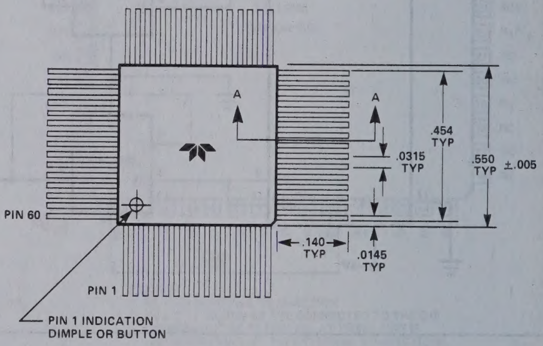
(Package #14)
24-Pin CerDIP


0.620
0.590
0.610
0.500
1.290 MAX
0.210
MAX
0.075
0.015
0.015
0.008
0° – 15°
0.200
0.120
0.110
0.090
0.070
0.030
0.023
0.014

(Package #21)
60-Pin Flat Package
Formed Leads


.054 ± .004
.047 ± .004
15° MAX
.098
± .002
.0075
.102 ± .012
.050 ± .006
.010 MIN

(Package #22)
60-Pin Flat Package
Unformed Leads


A
A
.454
TYP
.0315
TYP
.550
TYP
±.005
PIN 60
.140
TYP
.0145
TYP
PIN 1
PIN 1 INDICATION
DIMPLE OR BUTTON

TELEDYNE SEMICONDUCTOR

TSC14433
3 1/2 Digit ADC
• Multiplexed BCD Data
• Low Power

General Description

The TSC14433 is a low power, high-performance, monolithic CMOS 3 1/2 digit A/D converter. The TSC14433 combines both analog and digital circuits on a single IC, thus minimizing the number of external components. This dual slope A/D onverter provides automatic polarity and zero correction with the addition of two external resistors and two capacitors. The full-scale voltage range of this ratiometric IC extends rom 199.9 millivolts to 1.999 volts. The TSC14433B can operate over a wide range of power supply voltages including batteries and standard 5 volt supplies.

The high impedance MOS analog inputs are well suited for applications using current, resistance or voltmeters. The output drive is compatible with low power Schottky TTL loads and conforms to standard B-series CMOS.

The TSC14433 will interface with the TSC7211A (LCD), TSC7212A (LED) and TSC700A (high LED current drive) display drivers.

HANDLING PRECAUTIONS: These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

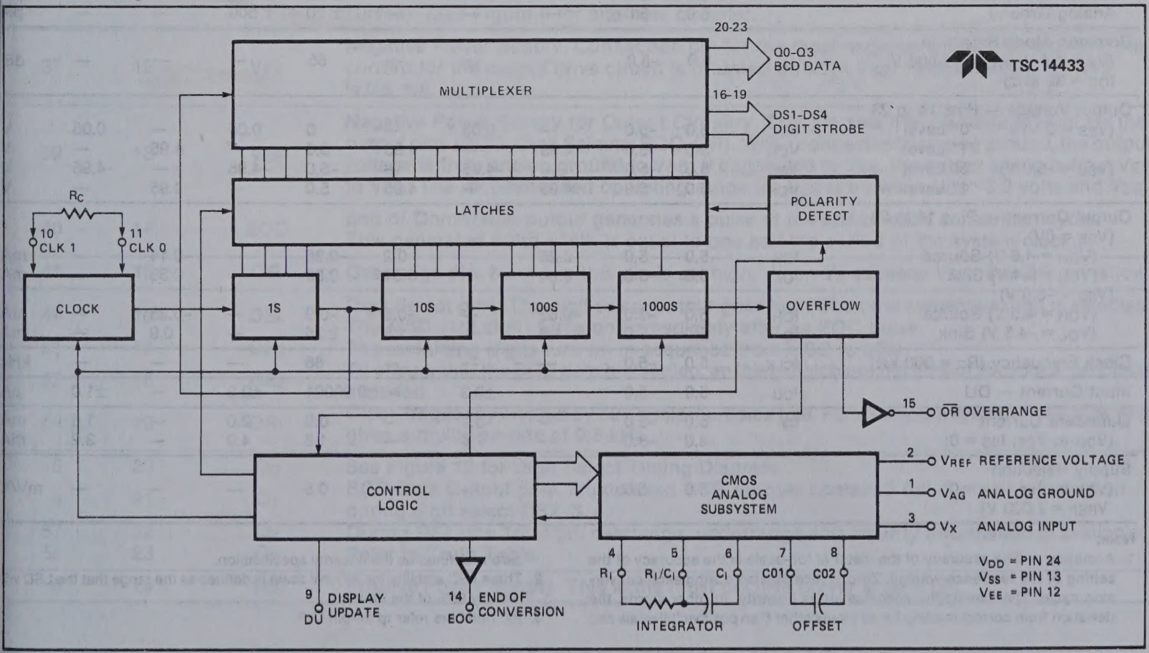
Features

- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions Per Second
- Z_{IN} > 1000 M Ohm
- Single Positive Voltage Reference
- Standard B-Series CMOS Outputs — Drives One Low Power Schottky load
- Uses On-chip System Clock, or External Clock
- Low Power Consumption: 8.0 mW Typical @ ±5.0 V
- Wide Supply Range: e.g., ±4.5 V to ±8.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Operates With LED and LCD Displays
- Low External Component Count
- Available in Compact Flat Package

Applications

- Portable Instruments
- Digital Voltmeters
- Digital Panel Meters
- Digital Scales
- Digital Thermometers
- Remote A/D Sensing Systems
- MPU Systems
- See Application Notes 19 and 21

Block Diagram


TSC14433
MULTIPLEXER
20-23
Q0-Q3 BCD DATA
16-19
DS1-DS4 DIGIT STROBE
LATCHES
POLARITY DETECT
R_C
10 CLK 1
11 CLK 0
CLOCK
1S
10S
100S
1000S
OVERFLOW
15 $\overline{OR}$ OVERRANGE
CONTROL LOGIC
CMOS ANALOG SUBSYSTEM
2 V_{REF} REFERENCE VOLTAGE
1 V_{AG} ANALOG GROUND
3 V_X ANALOG INPUT
4 R_I
5 R_I/C_I
6 C_I
7 C01
8 C02
INTEGRATOR
OFFSET
9 DU DISPLAY UPDATE
14 EOC END OF CONVERSION
V_{DD} = PIN 24
V_{SS} = PIN 13
V_{EE} = PIN 12

Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD} to V_{EE}	-0.5 to +18	Vdc
Voltage, Any Pin, Referenced to V_{EE}	V	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain Per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

Recommended Operating Conditions

(V_{SS} = 0 or V_{EE})

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage —			
V_{DD} to Analog Ground	V_{DD}	+5.0 to +8.0	Vdc
V_{EE} to Analog Ground	V_{EE}	-2.8 to -8.0	
Clock Frequency	f_{CLK}	32 to 400	kHz
Zero Offset Correction Capacitor	C_O	0.1 ±20%	μF

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{EE} \leq (V_{IN}$ or $V_{OUT}) \leq V_{DD}$.

Electrical Characteristics:

(C_I = 0.1 μF mylar, R_I = 470 kΩ @ V_{REF} = 2.000 V, R_I = 27 kΩ @ V_{REF} = 200.0 mV, C_O = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1.)

		V_{DD}	V_{EE}	-40°C		25°C			85°C		
CHARACTERISTIC	SYMBOL	Vdc	Vdc	MIN	MAX	MIN	TYP	MAX	MIN	MAX	UNIT
Linearity Output Reading (Note 1)	—										
(V_{REF} = 2.000 V)		5.0	-5.0	—	—	-0.05	+0.05	+0.05	—	—	%rdg
(V_{REF} = 200.0 mV)		5.0	-5.0	—	—	-1 count	—	+1 count	—	—	
Stability Output Reading (Note 2)	—										
(V_X = 1.990 V, V_{REF} = 2.000 V)		5.0	-5.0	—	—	—	—	2	—	—	LSD
(V_X = 199.0 mV, V_{REF} = 200.0 mV)		5.0	-5.0	—	—	—	—	3	—	—	LSD
Zero Output Reading (V_X = 0 V, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	0	0	—	—	LSD
Bias Current —											
Analog Input	—	5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Reference Input		5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Analog Ground		5.0	-5.0	—	—	—	± 20	± 500	—	—	pA
Common-Mode Rejection (V_X = 1.4 V, V_{REF} = 2.000 V, f_{OC} = 32 kHz)		5.0	-5.0	—	—	—	65	—	—	—	dB
Output Voltage — Pins 14 to 23											
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	-5.0	—	0.05	—	0	0.05	—	0.05	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
(V_{SS} = -5.0 V) "0" Level	V_{OL}	5.0	-5.0	—	-4.95	—	-5.0	-4.95	—	-4.95	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
Output Current — Pins 14 to 23											
(V_{SS} = 0V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	-5.0	-0.25	—	-0.2	-0.36	—	-0.14	—	mA
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	-5.0	0.64	—	0.51	0.88	—	0.36	—	mA
(V_{SS} = -5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	-5.0	-0.62	—	-0.5	-0.9	—	-0.35	—	mA
(V_{OL} = -4.5 V) Sink	I_O	5.0	-5.0	1.6	—	1.3	2.25	—	0.9	—	mA
Clock Frequency (R_C = 300 kΩ)	f_{CLK}	5.0	-5.0	—	—	—	66	—	—	—	kHz
Input Current — DU	I_{DU}	5.0	-5.0	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Quiescent Current (V_{DD} to V_{EE}, I_{SS} = 0)	I_Q	5.0	-5.0	—	3.7	—	0.9	2.0	—	1.6	mA
		8.0	-8.0	—	7.4	—	1.8	4.0	—	3.2	mA
Supply Rejection (V_{DD} to V_{EE}, I_{SS} = 0, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	0.5	—	—	—	mV/V

Note:

1. Accuracy — The accuracy of the meter at full-scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full-scale and zero is defined as the linearity specification.
2. Three LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.
3. Pin numbers refer to 24-pin DIP.

Pin Description

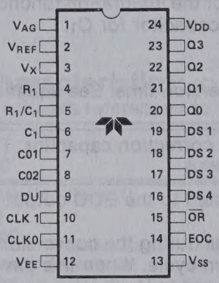
PIN NO. 60-Pin FP	PIN NO. 24-Pin DIP	SYMBOL	DESCRIPTION
7	1	V_{AG}	This is the Analog Ground. It has a high input impedance. This pin determines the reference level for the unknown input voltage (V_X) and the reference voltage (V_{REF}).
10	2	V_{REF}	Reference voltage. Full-scale output is equal to the voltage applied to V_{REF}. Therefore, full-scale voltage of 1.999 V requires 2.000 V reference and 199.9 mV full-scale requires a 200 mV reference. V_{REF} functions as system reset, also. When switched to V_{EE} the system is reset to the beginning of the conversion cycle.
12	3	V_X	The Unknown Input Voltage (V_X) is measured as a ratio of the reference voltage (V_{REF}) in a ratio-metric A/D conversion.
19 22 24	4 5 6	R_1 R_1/C_1 C_1	These pins are for external components used for the integration function in the dual slope conversion. Typical values are 0.1 μF (mylar) capacitor for C_1. R_1 = 470 kΩ (resistor) for 2.0 V full-scale. R_1 = 27 kΩ (resistor) for 200 mV full-scale. Clock frequency of 66 kHz gives 250 ms conversion time. See equation below for calculation of integrator component values.
25 26	7 8	CO_1 CO_2	These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF.
27	9	DU	Display Update input pin. When DU is connected to the EOC output every conversion is displayed. New data will be strobed into the output latches during the conversion cycle if a positive edge is received on DU prior to the ramp-down cycle. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.
34 36	10 11	CLK_1 CLK_0	Clock input pins. The TSC14433 has its own oscillator system clock. Connecting a single resistor between CLK_1 and CLK_0 sets the clock frequency. A crystal or LC circuit may be inserted in lieu of a resistor for improved stability. CLK_1, the clock input, can be driven from an external clock source, which need only have standard CMOS output drive. This pin is referenced to V_{EE} for external clock inputs. A 300 kΩ resistor yields a clock frequency of about 66 kHz. (See typical characteristic curves). (See Figure 9 for alternate circuits).
37	12	V_{EE}	Negative Power Supply. Connection pin for the most negative supply. Please note the current for the output drive circuit is returned through V_{SS}. Typical supply current is 0.8 mA.
39	13	V_{SS}	Negative Power Supply for Output Circuitry. This pin sets the low voltage level for the output pins (BCD, Digit Selects, EOC, OR). When connected to analog ground, the output voltage is from analog ground to V_{DD}. If connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The recommended operating range for V_{SS} is between V_{DD} −3.0 volts and V_{EE}.
40	14	EOC	End of Conversion output generates a pulse at the end of each conversion cycle. This generated pulse width is equal to one half the period of the system clock.
41	15	OR	Overrange pin. Normally this pin is set high. When V_X exceeds V_{REF} the OR pin is low.
49 51 52 54	16 17 18 19	DS_4 DS_3 DS_2 DS_1	Digit Select pins. The digit select output goes high when the respective digit is selected. The MSD (1/2 digit) turns on immediately after an EOC pulse. The remaining digits turn on in sequence from MSD to LSD. To ensure that the BCD data has settled, an inter-digit blanking time of two clock periods is included. Clock frequency divided by 80 equals multiplex rate. For example a system clock of 60 kHz gives a multiplex rate of 0.8 kHz.
5 4 57 55	20 21 22 23	Q_0 Q_1 Q_2 Q_3	See Figure 12 for Digit Select Timing Diagram. BCD Data Output pins. Multiplexed BCD outputs contain 3 full digits of information during digit select DS2, 3, 4. During DS1, the 1/2 digit, overrange, underrange and polarity information is available. Refer to Truth Table.
6	24	V_{DD}	Positive Power Supply. This is the most positive power supply pin.

Ordering Information

Part No.	Package	Temperature Range
TSC14433CJ	24-pin Plastic Dip	-40° C to +85° C
TSC14433CL	24-pin CerDIP	-40° C to +85° C
TSC14433CBQ	60-Pin Plastic Flat Package: Formed Leads	-40° C to +85° C

Part No.	Package	Temperature Range
TSC14433CSQ	60-Pin Plastic Flat Package: Unformed Leads	-40° C to +85° C
Devices with 160, Hour, +125° C Burn-In		
TSC14433CJ/BI	24-Pin Plastic Dip	-40° C to +85° C
TSC14433CL/BI	24-Pin CerDIP	-40° C to +85° C

Pin Configuration

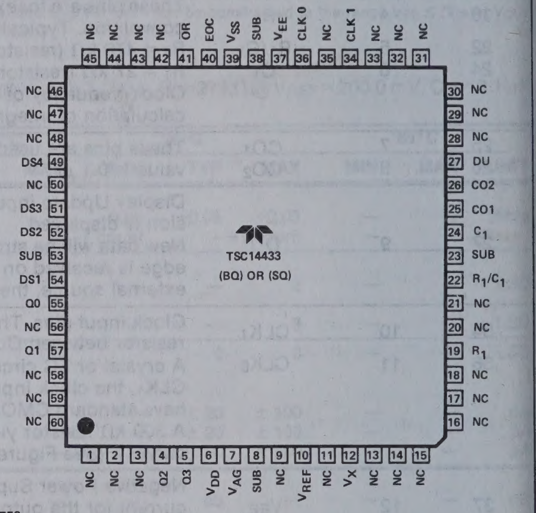

VAG 1
VREF 2
VX 3
R1 4
R1/C1 5
C1 6
CO1 7
CO2 8
DU 9
CLK 1 10
CLK0 11
VEE 12
24 VDD
23 Q3
22 Q2
21 Q1
20 Q0
19 DS 1
18 DS 2
17 DS 3
16 DS 4
15 OR
14 EOC
13 VSS

$$R_1 = \frac{V_X(\max)}{C_1} \times \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X\ (\max) - 0.5$$

$$T = 4000 \times \frac{1}{f_{CLK}}$$

Where
R_1 is in kΩ
V_{DD} is the voltage at pin 24 referenced to V_{AG}
V_X is the voltage at pin 3 referenced to V_{AG}
f_{CLK} is the clock frequency at pin 10 in kHz


NC 45
NC 44
NC 43
NC 42
OR 41
EOC 40
VSS 39
SUB 38
VEE 37
CLK 0 36
NC 35
CLK 1 34
NC 33
NC 32
NC 31
NC 46
NC 47
NC 48
DS4 49
NC 50
DS3 51
DS2 52
SUB 53
DS1 54
Q0 55
NC 56
Q1 57
NC 58
NC 59
NC 60
30 NC
29 NC
28 NC
27 DU
26 CO2
25 CO1
24 C1
23 SUB
22 R1/C1
21 NC
20 NC
19 R1
18 NC
17 NC
16 NC
TSC14433
(BQ) OR (SQ)
1 NC
2 NC
3 NC
4 Q2
5 Q3
6 VDD
7 VAG
8 SUB
9 NC
10 VREF
11 NC
12 VX
13 NC
14 NC
15 NC

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Typical Characteristics

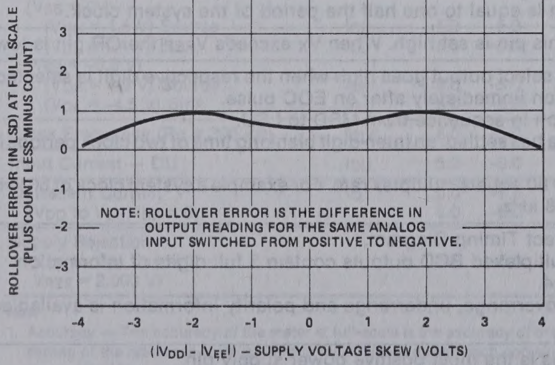


Figure 1: Typical Rollover Error vs. Power Supply Skew.

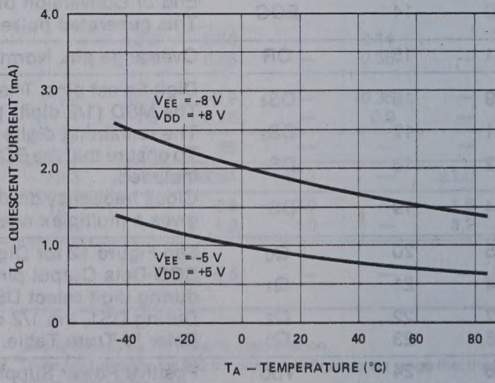


Figure 2: Typical Quiescent Power Supply Current vs. Temperature.

Typical Characteristics (Cont.)

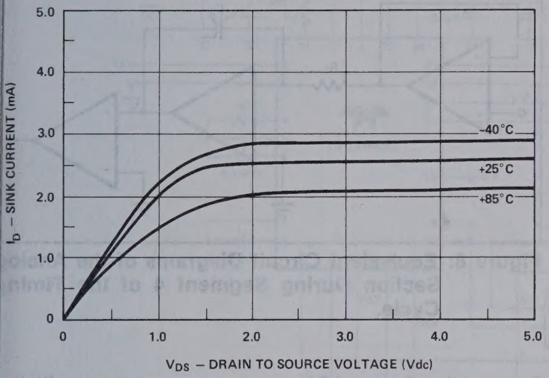


Figure 3: Typical N-Channel Sink Current at $V_{DD}-V_{SS}$ = 5 Volts.

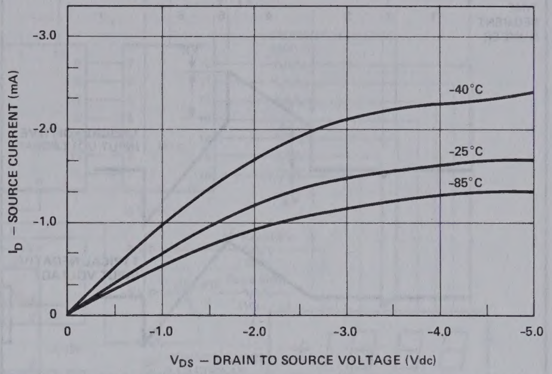


Figure 4: Typical P-Channel Source Current at $V_{DD}-V_{SS}$ = 5 Volts.

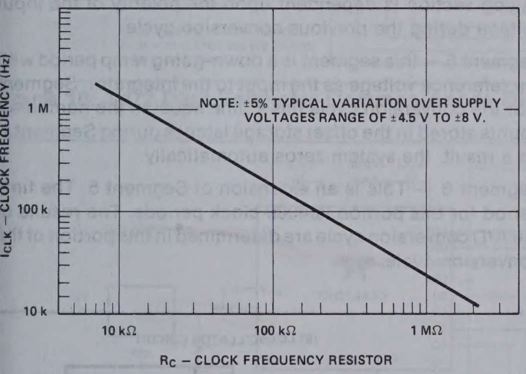


Figure 5: Typical Clock Frequency vs. Resistor (R_C).

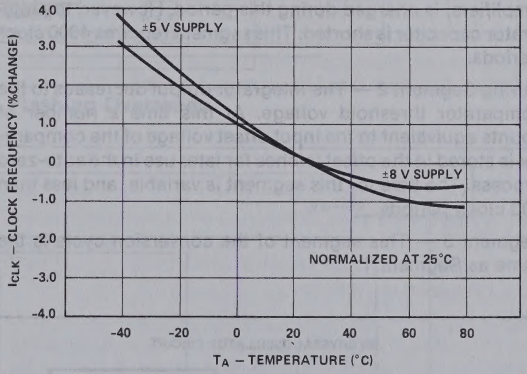


Figure 6: Typical % Change of Clock Frequency vs. Temperature.

$$\text{CONVERSION RATE} = \frac{\text{CLOCK FREQUENCY}}{16{,}400} \pm 1.5\%$$

$$\text{MULTIPLEX RATE} = \frac{\text{CLOCK FREQUENCY}}{80}$$

Circuit Description

The TSC14433 CMOS IC becomes a modified dual slope A/D with a minimum of external components. This IC has the customary CMOS digital logic circuitry as well as the CMOS analog circuitry. It provides the user with digital functions (Such as counters, latches, multiplexers) and analog functions (such as operational amplifiers and comparators) on a single chip.

Features of this sytem include auto-zero, high input impedances and autopolarity. Low power consumption and a wide range of power supply voltages are also advantages of this CMOS device. The system's auto-zero function compensates for the offset voltage of the internal amplifiers and comparators. In this "ratiometric system," the output reading is the ratio of the unknown voltage to the reference voltage where a ratio of 1 equal to the maximum count of 1999. It takes approximately 16,000 clock periods to complete one conversion cycle. Each conversion cycle may be divided into six segements. Figure 7 shows the conversion cycle in 6 segments for both positive and negative inputs.

Segment 1 — The offset capacitor (C_0), which compensates

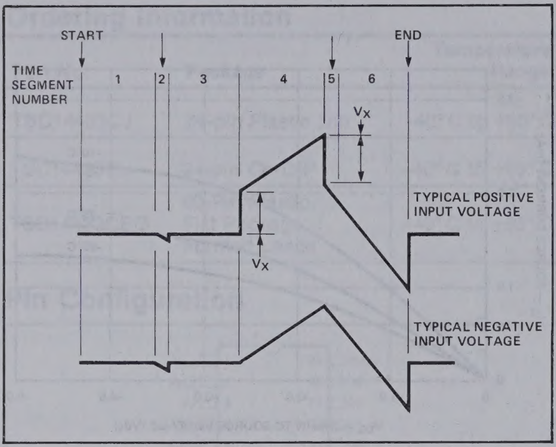


Figure 7: Integrator Waveforms at Pin 6.

for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. However, the integrator capacitor is shorted. This segment requires 4000 clock periods.

During Segment 2 — The integrator output decreases to the comparator threshold voltage. At this time a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the auto-zero process. The time for this segment is variable, and less than 800 clock periods.

Segment 3 — This segment of the conversion cycle is the same as Segment 1.

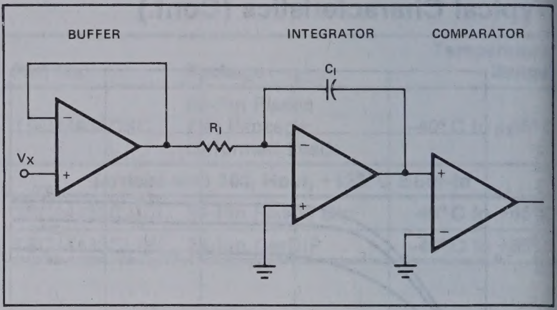


Figure 8: Equivalent Circuit Diagrams of the Analog Section During Segment 4 of the Timing Cycle.

Segment 4 — Segment 7 is an up-going ramp cycle with the unknown input voltage (Vx) as the input to the integrator. Figure 8 shows the equivalent configuration of the analog section of the TSC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

Segment 5 — this segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 — This is an extension of Segment 5. The time period for this portion is 4000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

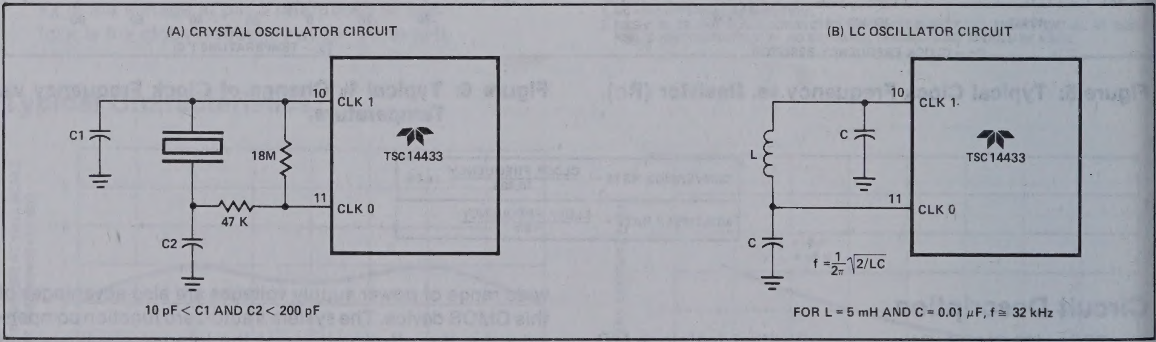
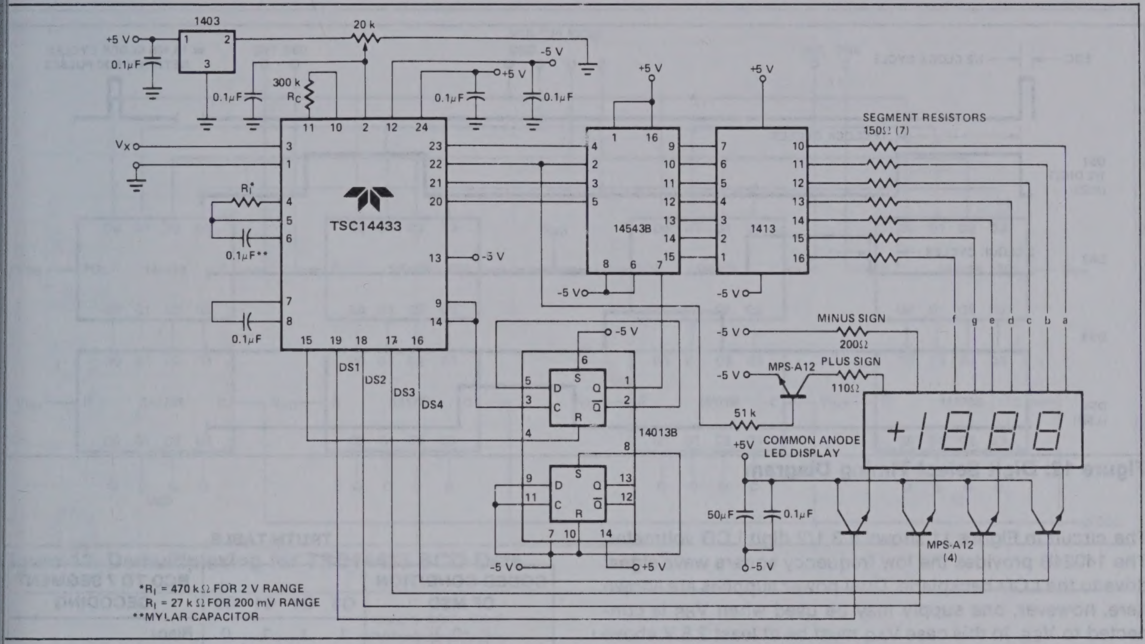

(A) CRYSTAL OSCILLATOR CIRCUIT
C1
C2
18M
47 K
10
11
CLK 1
CLK 0
TSC14433
10 pF < C1 AND C2 < 200 pF
(B) LC OSCILLATOR CIRCUIT
L
C
C
C
10
11
CLK 1
CLK 0
TSC14433
$f = \frac{1}{2\pi}\sqrt{2/LC}$
FOR L = 5 mH AND C = 0.01 μF, f ≅ 32 kHz

Figure 9: Alternate Oscillator Circuits.

Applications Information

Figure 10 is an example of a 3 1/2 digit voltmeter using the TSC14433 with common-anode displays. This system require a 2.5 V reference. Full-scale may be adjusted to 1.999 V or 199.9 mV. Input overrange is indicated by flashing a display.

This display uses LEDs with common anode digit lines. Power supply for this system is shown as a dual ±5 V supply; however, the TSC14433 will operate over a wide voltage range (see recommended operating conditions, page 3).


1403
+5 V
0.1µF
20 k
-5 V
+5 V
300 k
R_C
0.1µF
V_X
R_I^*
0.1µF**
0.1µF
TSC14433
-5 V
DS1
DS2
DS3
DS4
14543B
-5 V
+5 V
1413
SEGMENT RESISTORS
150Ω (7)
f g e d c b a
MINUS SIGN
200Ω
PLUS SIGN
110Ω
MPS-A12
51 k
14013B
+5V
COMMON ANODE
LED DISPLAY
50µF
0.1µF
MPS-A12
(4)
-5 V
+5 V
+1888

$^*R_I$ = 470 kΩ FOR 2 V RANGE
R_I = 27 kΩ FOR 200 mV RANGE
**MYLAR CAPACITOR

Figure 10: 3 1/2 Digit Voltmeter-Common Anode Displays, Flashing Overrange

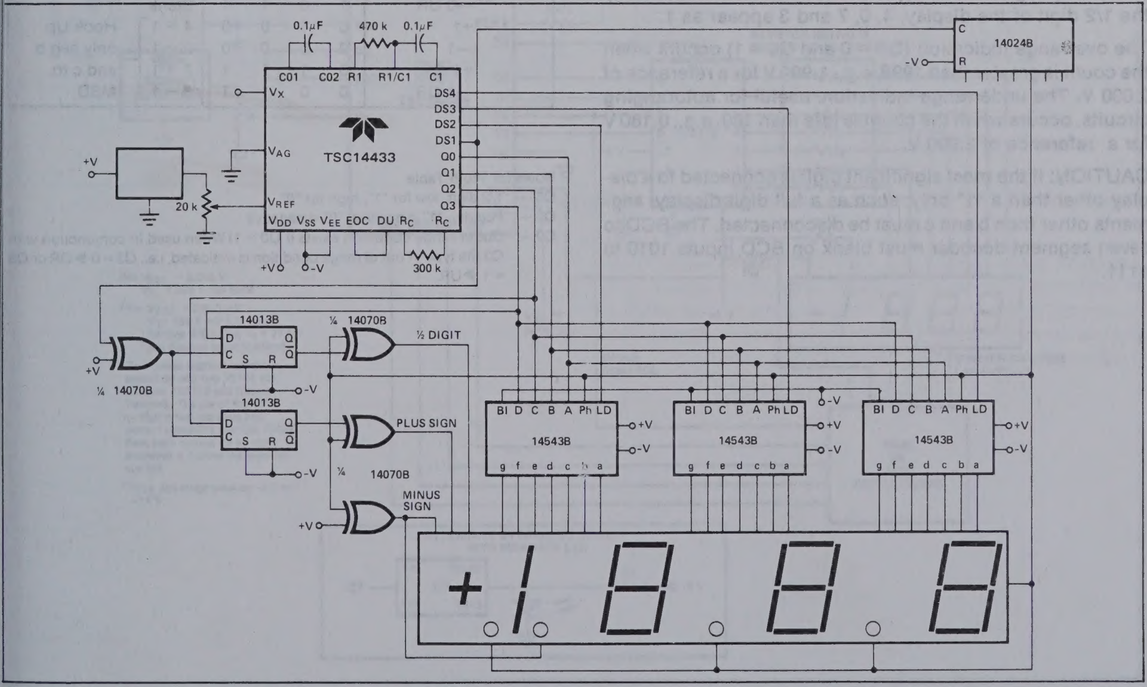

0.1µF
470 k
0.1µF
C01
C02
R1
R1/C1
C1
V_X
V_{AG}
TSC14433
V_{REF}
V_{DD} V_{SS} V_{EE} EOC DU R_C
R_C
DS4
DS3
DS2
DS1
Q0
Q1
Q2
Q3
+V
20 k
+V
-V
300 k
14024B
C
R
-V
14013B
¼ 14070B
½ DIGIT
¼ 14070B
14013B
PLUS SIGN
¼ 14070B
MINUS SIGN
+V
BI D C B A Ph LD
14543B
g f e d c b a
+V
-V
+18.8.8

Figure 11: 3 1/2 Digit Voltmeter with LCD Display.

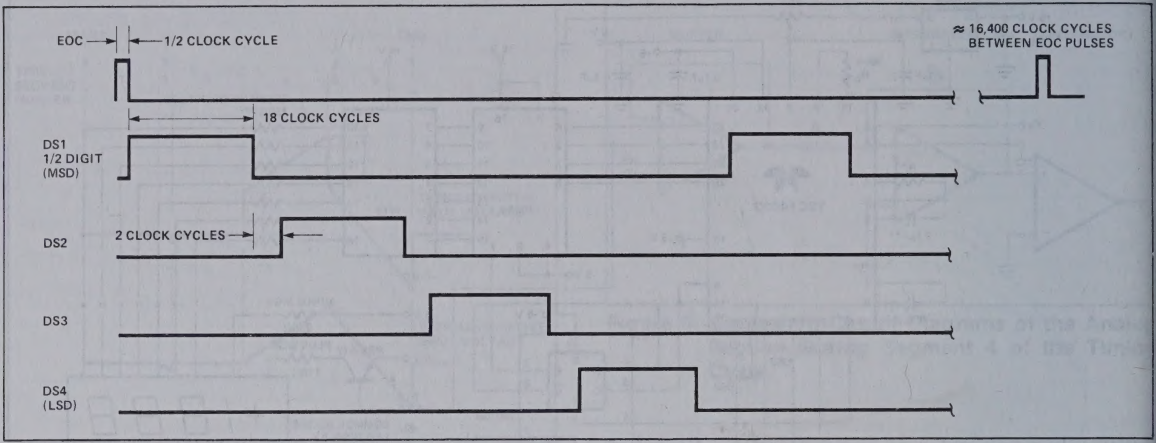


Figure 12: Digit Select Timing Diagram

The circuit in Figure 11 shows a 3 1/2 digit LCD voltmeter. The 14024B provides the low frequency square wave signal drive to the LCD backplane. Dual power supplies are shown here, however, one supply may be used when V_{SS} is connected to V_{EE}. In this case V_{AG} must be at least 2.8 V above V_{EE}.

When only segment b and c of the decoder are connected to the 1/2 digit of the display, 4, 0, 7 and 3 appear as 1.

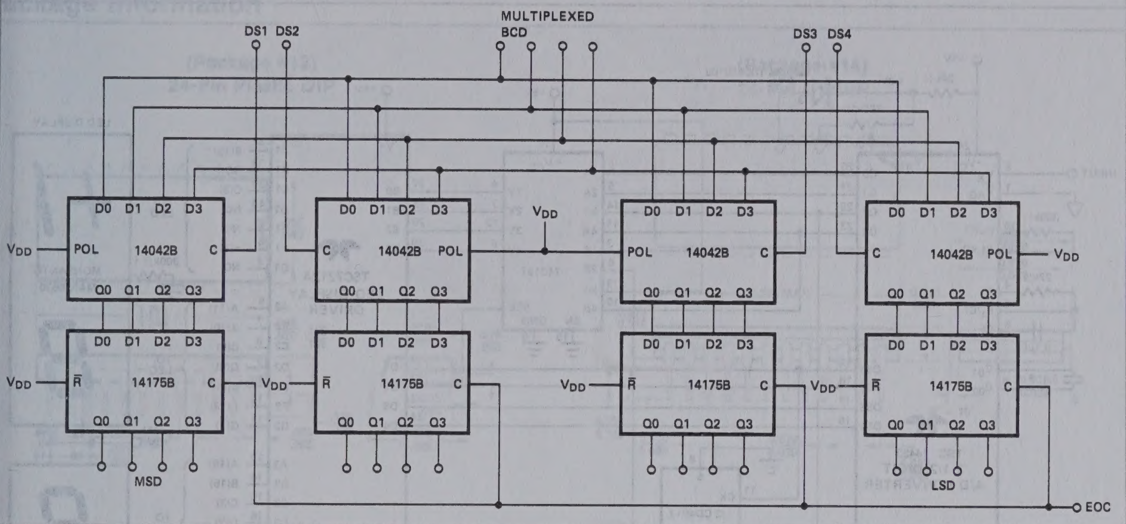
The overrange indication (Q3 = 0 and Q0 = 1) occurs when the count is greater than 1999, e.g., 1.999 V for a reference of 2.000 V. The underrange indication, useful for autoranging circuits, occurs when the count is less than 180, e.g., 0.180 V for a reference of 2.000 V.

CAUTION: If the most significant digit is connected to a display other than a "1" only; such as a full digit display, segments other than b and c must be disconnected. The BCD to seven segment decoder must blank on BCD inputs 1010 to 1111.

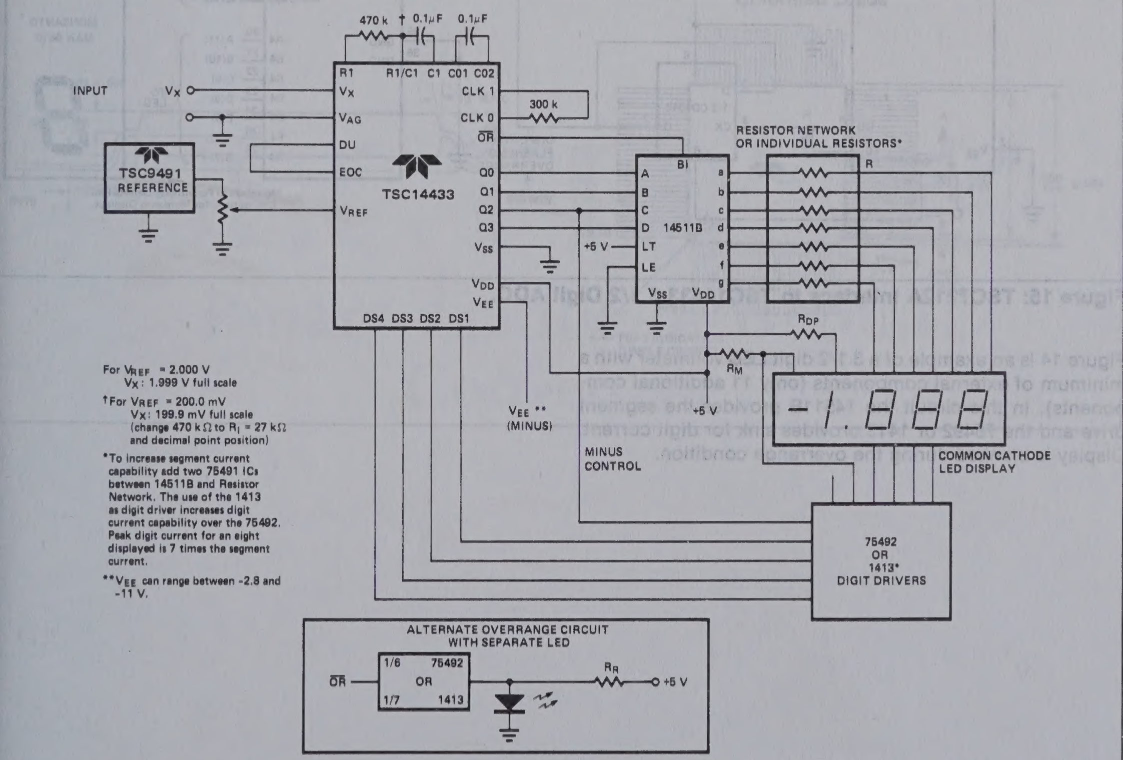
TRUTH TABLE

CODED CONDITION OF MSD	Q3	Q2	Q1	Q0	BCD TO 7 SEGMENT DECODING
+0	1	1	1	0	Blank
—0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
—0 UR	1	0	1	1	Blank
+1	0	1	0	0	4 → 1 Hook Up
—1	0	0	0	0	0 → 1 only seg b
+1 OR	0	1	1	1	7 → 1 and c to
—1 OR	0	0	1	1	3 → 1 MSD

Notes for Truth Table
Q3 — 1/2 digit, low for "1", high for "0"
Q2 — Polarity: "1" = positive, "0" = negative
Q0 — Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 ➔ OR or Q3 = 1 ➔ UR.


MULTIPLEXED BCD
DS1 DS2
DS3 DS4
D0 D1 D2 D3
VDD
POL
14042B
C
Q0 Q1 Q2 Q3
R̄
14175B
MSD
LSD
EOC

igure 13: Demultiplexing for TSC14433 BCD Data.


470 k
†
0.1µF
0.1µF
R1
R1/C1
C1
C01
C02
INPUT
VX
VAG
DU
EOC
VREF
CLK 1
CLK 0
OR̄
300 k
TSC14433
Q0
Q1
Q2
Q3
VSS
VDD
VEE
DS4 DS3 DS2 DS1
TSC9491 REFERENCE
RESISTOR NETWORK OR INDIVIDUAL RESISTORS*
R
BI
A
B
C
D
14511B
LT
LE
+5 V
a
b
c
d
e
f
g
VSS
VDD
RDP
RM
-1.888
COMMON CATHODE LED DISPLAY
VEE ** (MINUS)
+5 V
MINUS CONTROL
75492 OR 1413* DIGIT DRIVERS
ALTERNATE OVERRANGE CIRCUIT WITH SEPARATE LED
OR̄
1/6
75492
OR
1/7
1413
RR
+5 V

For V_{REF} = 2.000 V
V_X: 1.999 V full scale

†For V_{REF} = 200.0 mV
V_X: 199.9 mV full scale
(change 470 kΩ to R_I = 27 kΩ and decimal point position)

*To increase segment current capability add two 75491 ICs between 14511B and Resistor Network. The use of the 1413 as digit driver increases digit current capability over the 75492. Peak digit current for an eight displayed is 7 times the segment current.

**V_{EE} can range between -2.8 and -11 V.

Figure 14: 3 1/2 Digit Voltmeter with Low Component Count using Common Cathode Displays.

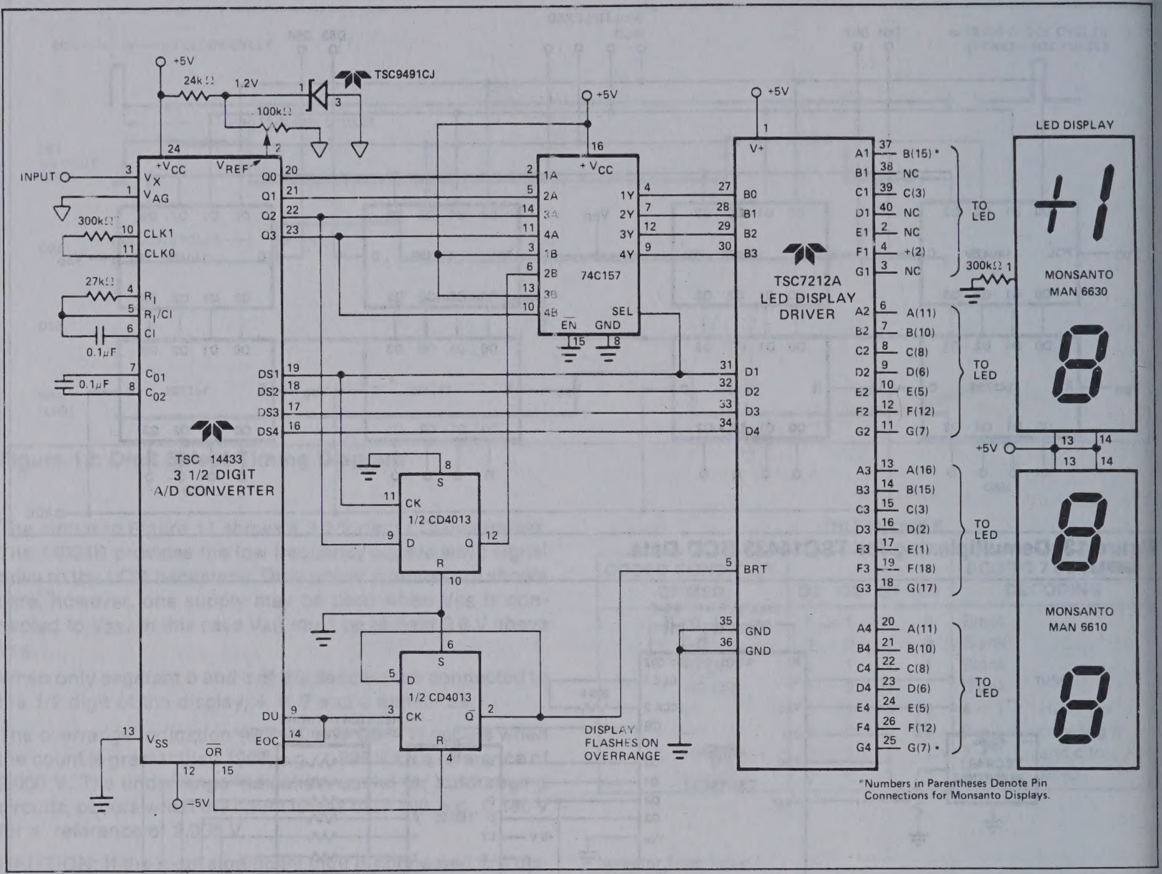
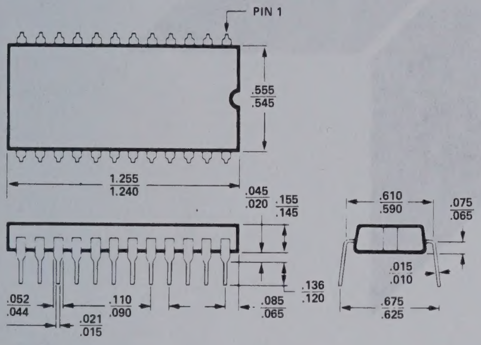

+5V
24kΩ
1.2V
TSC9491CJ
100kΩ
INPUT
+VCC
VREF
VX
VAG
300kΩ
CLK1
CLK0
27kΩ
RI
RI/CI
CI
0.1μF
CO1
CO2
Q0
Q1
Q2
Q3
DS1
DS2
DS3
DS4
TSC 14433
3 1/2 DIGIT
A/D CONVERTER
VSS
DU
EOC
OR
−5V
74C157
1A
2A
3A
4A
1B
2B
3B
4B
1Y
2Y
3Y
4Y
SEL
EN
GND
1/2 CD4013
CK
D
Q
S
R
Q̄
V+
B0
B1
B2
B3
D1
D2
D3
D4
BRT
GND
TSC7212A
LED DISPLAY
DRIVER
DISPLAY
FLASHES ON
OVERRANGE
A1
B1
C1
D1
E1
F1
G1
A2
B2
C2
D2
E2
F2
G2
A3
B3
C3
D3
E3
F3
G3
A4
B4
C4
D4
E4
F4
G4
B(15)*
NC
C(3)
+(2)
A(11)
B(10)
C(8)
D(6)
E(5)
F(12)
G(7)
A(16)
B(15)
D(2)
E(1)
F(18)
G(17)
G(7) •
TO LED
300kΩ
LED DISPLAY
MONSANTO
MAN 6630
MONSANTO
MAN 6610
*Numbers in Parentheses Denote Pin Connections for Monsanto Displays.

Figure 15: TSC7212A Interface to TSC14433 3 1/2 Digit ADC.

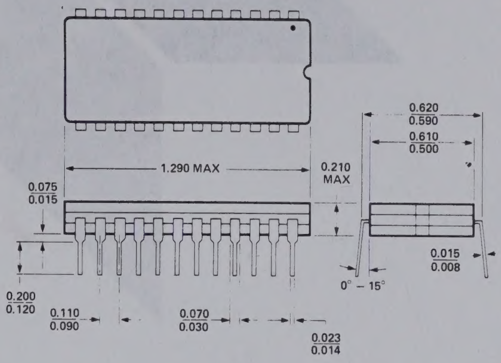
Figure 14 is an example of a 3 1/2 digit LED voltmeter with a minimum of external components (only 11 additional components). In this circuit the 14511B provides the segment drive and the 75492 or 1413 provides sink for digit current. Display is blanked during the overrange condition.

ackage Information

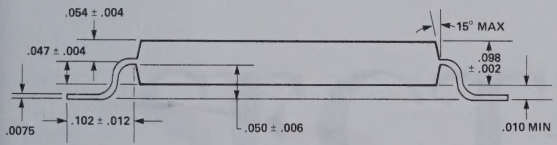
(Package #12)
24-Pin Plastic DIP


PIN 1
.555
.545
1.255
1.240
.045
.020
.155
.145
.610
.590
.075
.065
.015
.010
.136
.120
.052
.044
.110
.090
.021
.015
.085
.065
.675
.625

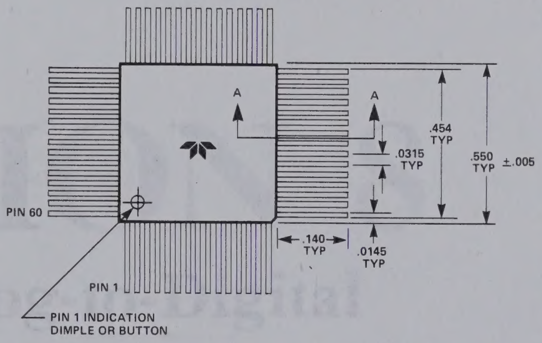
(Package #14)
24-Pin CerDIP


0.620
0.590
0.610
0.500
1.290 MAX
0.210
MAX
0.075
0.015
0.015
0.008
0° – 15°
0.200
0.120
0.110
0.090
0.070
0.030
0.023
0.014

(Package #21)
60-Pin Flat Package
Formed Leads


.054 ± .004
15° MAX
.047 ± .004
.098
± .002
.0075
.102 ± .012
.050 ± .006
.010 MIN

(Package #22)
60-Pin Flat Package
Unformed Leads


A
A
.454
TYP
.0315
TYP
.550
TYP
±.005
PIN 60
.140
TYP
.0145
TYP
PIN 1
PIN 1 INDICATION
DIMPLE OR BUTTON

Notes

SECTION 8

Binary Analog-to-Digital Converters

Section 8
Binary A/D Converters 8-3

TSC500	Integrating Converter Analog Processor	8-5
TSC800	15-Bit Plus Sign Integrating A/D Converter	8-13
TSC7109	12-Bit Plus Sign Integrating A/D Converter	8-29
TSC8700 (8-Bit)	Binary Output ADC	8-49
TSC8701 (10-Bit)	Binary Output ADC	8-49
TSC8702 (12-Bit)	Binary Output ADC	8-49
TSC8703 (8-Bit)	Three State Binary Output ADC	8-61
TSC8704 (10-Bit)	Three State Binary Output ADC	8-61
TSC8705 (12-Bit)	Three State Binary Output ADC	8-61

TELEDYNE SEMICONDUCTOR

TSC500
Integrating Converter Analog Processor

- **Automatic Zero Adjust**
- **μProcessor Controlled**

General Description

The CMOS TSC500 contains all the analog circuits needed to construct an integrating analog-to-digital converter. The analog input buffer, integrator, analog switches, comparator and phase control logic are all on chip. Resolution to 4 1/2 digits (1 part in 20,000) is possible.

The dual slope converter uses time to quantize the analog input signal. A microprocessor and software routine perform the digital function of "counting clocks" for the dual slope integrating converter process. The user can control resolution and conversion speed through software. The TSC500 analog building block can be used to construct an 8-bit or high resolution 14-bit converter by modifying software routines.

A microprocessor controls the TSC500 through the A and B logic input signals. Four TSC500 phases are possible: auto-zero, signal integrate, reference integrate (deintegrate), and integrator zero output.

The TSC500 comparator output provides polarity and integrator zero crossing information. The comparator output always makes a high to low transition when the integrator crosses zero. This signals the end of a conversion to the processor.

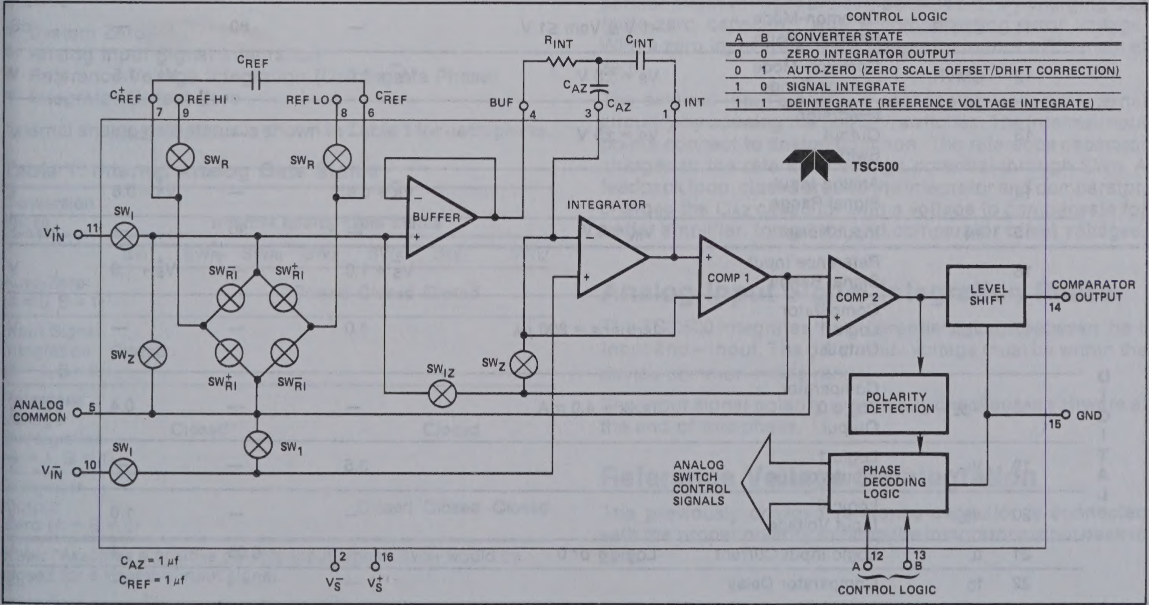
A precision dual slope integrating converter with automatic zero scale offset voltage and drift correction requires only a reference, two capacitors, a resistor and a microprocessor controller. The TSC500 contains the analog circuits needed to construct a dual slope integrating converter with an auto-zero phase. A zero-integrator output phase can be selected to eliminate errors caused by out-of-range input signals. The zero integrator phase makes the next conversion after an out-of-range conversion accurate.

The CMOS TSC500 operates from ±5 V supplies. Power dissipation is only 10 mW. Leakage currents at the differential inputs are a low 10 pA. The TSC500 differential reference inputs allow easy ratiometric measurements.

Features

- Differential Analog Input
- Differential Reference
- Low Linearity Error 0.005%
- Fast Zero-Crossing Comparator .... 4 μs
- Low Power Dissipation .... 10 mW
- Auto-Zero Cycle Eliminates Zero-Scale Error & Drift
- Zero Integrator Phase Speeds Recovery From Over-range Input Signals
- Automatic Internal Polarity Detection
- Low Input Current .... 15 pA Max
- Wide Analog Input Voltage .... ±4.2 V
- Microprocessor Control of Dual Slope ADC Conversion

Functional Diagram



A	B	CONVERTER STATE
0	0	ZERO INTEGRATOR OUTPUT
0	1	AUTO-ZERO (ZERO SCALE OFFSET/DRIFT CORRECTION)
1	0	SIGNAL INTEGRATE
1	1	DEINTEGRATE (REFERENCE VOLTAGE INTEGRATE)

CONTROL LOGIC
TSC500
R_{INT}
C_{INT}
C_{REF}
C^+_{REF} 7
REF HI 9
REF LO 8
C^-_{REF} 6
BUF 4
C_{AZ} 3
INT 1
SW_R
SW_R
SW_I
V^+_{IN} 11
BUFFER
INTEGRATOR
COMP 1
COMP 2
LEVEL SHIFT
COMPARATOR OUTPUT 14
SW^-_{RI}
SW^+_{RI}
SW^+_{RI}
SW^-_{RI}
SW_Z
SW_{IZ}
SW_Z
POLARITY DETECTION
ANALOG COMMON 5
GND 15
SW_1
SW_I
V^-_{IN} 10
ANALOG SWITCH CONTROL SIGNALS
PHASE DECODING LOGIC
$C_{AZ} = 1\,\mu f$
$C_{REF} = 1\,\mu f$
2 V^-_S
16 V^+_S
A 12
B 13
CONTROL LOGIC

Integrating Converter
Analog Processor
- **Automatic Zero Adjust**
- **μ Processor Controlled**

TSC500

Absolute Maximum Ratings

Supply (V_S^+ to V_S^-)	18 V
Positive Supply Voltage (V_S^+ to Gnd)	12 V
Negative Supply Voltage (V_S^- to Gnd)	-12 V
Analog Input Voltage (V_{IN}^+ or V_{IN}^-)	V_S^+ to V_S^-
Logic Input Voltage	V_S^+ + 0.3 V to Gnd - 0.3 V
Package Power Dissipation	0.5 W
Ambient Operating Temperature Range	
CerDIP Package (I)	-25°C to +85°C
Plastic Package (C)	0°C to +70°C
Storage Temperature	-55°C to 150°C
Lead Soldering Temperature (60 seconds)	+300°C

Electrical Specifications: T_A = 25°C, V_S = ±5 V unless otherwise specified. C_{AZ} = C_{REF} = 1.0 μf.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TSC500 TYP	MAX	UNIT
ANALOG	1		Resolution		—	—	50	ppm
	2	ZSE	Zero-Scale Error	Note 1		—	0.005	%
	3	ENL	End Point Linearity	Note 1	—	0.005	0.01	%
	4	NL	Best Case Straight Line Linearity	Note 1, 2			0.005	%
	5	DNL	Differential Non-Linearity		—	—	0.0025	%
	6	TC_{ZS}	Zero-Scale Temperature Coefficient	Over Operating Temperature Range	—	1.0	2.0	μV/°C
	7	SYE	Full-Scale Symmetry Error (Rollover Error)	4 1/2 Digit Resolution	—	—	0.01	%
	8		Ratiometric Reading	V_{IN} = V_{REF} = 1.0 V	—	—	0.035	%
	9	FS_{TC}	Full-Scale Temperature Coefficient	Over Operating Temperature Range External Reference T_C = 0 ppm/°C	—	—	10	ppm/°C
	10	I_{IN}	Input Current	V_{IN} = 0 V	—	6	15	pA
	11	CMRR	Common-Mode Rejection Ratio	-1 V ≤ Vcm ≤1 V	—	80	—	dB
	12	CMVR	Common-Mode Voltage Range	V_S = ±5 V	V_S^- + 1.5	—	V_S^+ - 1.5	V
	13		Integrator Output Swing	V_S = ±5 V	—	—	±4.1	V
	14		Analog Input Signal Range		V_S^- + 0.8	—	V_S^+ - 0.8	V
	15	e_N	Input Noise	V_{IN} + 0 V	—	30	—	μV_{p-p}
DIGITAL	16		Reference Input Signal Range		V_S^- + 1.0	—	V_S^+ - 1.0	V
	17	V_{OH}	Comparator Logic 1 Output	I_{SOURCE} = 800 μA	4.0	—	—	V
	18	V_{OL}	Comparator Logic 0 Output	I_{SINK} = 4.0 mA	—	—	0.4	V
	19	V_{IH}	Logic 1 Input Voltage		3.5	—	—	V
	20	V_{IL}	Logic 0 Input Voltage		—	—	1.0	V
	21	I_L	Logic Input Current	Logic 1 or 0	—	0.05	1	μA
	22	t_D	Comparator Delay		—	4	—	μs

Electrical Specifications: $T_A = 25°C$, $V_S = \pm 5$ V unless otherwise specified. $C_{AZ} = C_{REF} = 1.0$ μf. (Cont.)

					TSC500			
TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	23	I_S	Supply Current	$V_S = \pm 5$ V, A = 0, B = 1	—	1.0	1.5	mA
	24	P_D	Power Dissipation	$V_S = \pm 5$ V	—	—	15	mW
POWER	25	V_S^+	Positive Supply Operating Voltage Range		4	—	10	V
	26	V_S^-	Negative Supply Operating Voltage Range		-3	—	-8	V
	27	$V_S^+ - V_S^-$	Supply Operating Voltage Range		7	—	15	V

Notes:

1.) Integrate time = 10,000 T_P, Auto-Zero Time = 10,000 T_P, Full-Scale Deintegrate Time = 20,000 T_P, T_P = 8.3 μs (3.0 Conversions/Second) V_{FS} = 2.0 V, C_{INT} = 0.33 μf, R_{INT} = 125 kΩ

2.) End Point Linearity at, ±1/4, ±1/2, ±3/4 FS after Full-Scale Adjustment.

Ordering Information

Part No.	Package	Temperature Range	System Resolution
TSC500CPE	16-Pin Plastic Dip	0° C to 70° C	4 1/2 Digits (50 ppm)
TSC500IJE	16-Pin CerDIP	-25° C to +85° C	4 1/2 Digits (50 ppm)

TSC500 Operation Theory

The TSC500 incorporates a system zero and integrator output voltage zero phase to the normal two phase dual slope measurement cycle. Reduced system errors, fewer calibration steps and a shorter over-range recovery time result.

The TSC500 measurement cycle can use all four phases if desired.

- System Zero
- Analog Input Signal Integration
- Reference Voltage Integration (Deintegrate Phase)
- Integrator Output Zero

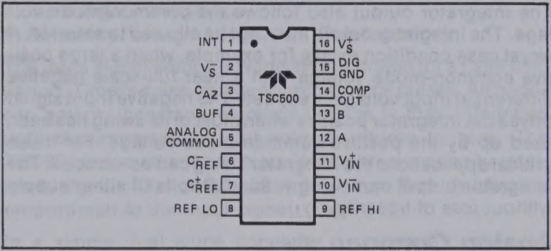
Internal analog gate status is shown in Table 1 for each phase.

Table 1: Internal Analog Gate Status

Conversion Phase	Internal Analog Gate Status						
	SW_I	SW_{RI}^+	SW_{RI}^-	SW_Z	SW_R	SW_1	SW_{IZ}
Auto-Zero (A = 0, B = 1)				Closed	Closed	Closed	
Input Signal Integration (A = 1, B = 0)	Closed						
Reference Voltage Deintegration (A = 1, B = 1)		Closed*				Closed	
Integrator Output Zero (A = B = 0)					Closed	Closed	Closed

Note: *Assumes a positive polarity input signal. SW_{RI}^- would be closed for a negative input signal.

Pin Configuration



System Zero Phase

During this phase errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage. With a zero input voltage the integrator output will remain at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

Analog Input Signal Integration Phase

The TSC500 integrates the differential voltage between the + Input and - Input. The differential voltage must be within the device common-mode range.

The input signal polarity is normally checked via software at the end of this phase.

Reference Voltage Deintegration

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero.

Integrator Output Zero

This phase guarantees the integrator output is at zero volts when the system zero phase is entered and that the true system offset voltages are compensated. It is normally used when the input has been over-ranged. The phase is not necessary for operation if over-range inputs do not occur or recovery time is not a system consideration.

TSC500 Analog Section

Differential Inputs (V_{IN}^{+} [Pin 11], V_{IN}^{-} [Pin 10])

The TSC500 operates with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 0.8 V below the positive supply to 0.8 V above the negative supply. Within this common-mode voltage range a common-mode rejection ratio is typically 80 dB. Full accuracy is maintained, however, when the inputs are no more than 1.5 V from either supply.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst case condition exists, for example, when a large positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced. The integrator output can swing within 0.9 volts of either supply without loss of linearity.

Analog Common (Pin 5)

Analog common is used as the V_{IN}^{-} return during system-zero and reference deintegrate. If V_{IN}^{-} is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications, V_{IN}^{-} will be set at a fixed known voltage (power supply common, for instance). A common-mode voltage will exist when V_{IN}^{-} is not connected to analog common.

Differential Reference (REF HI Pin 9, REF LO Pin 8)

The reference voltage can be generated anywhere within the power supply voltage of the converter. Roll-over error is caused by the reference capacitor losing or gaining charge due to stray capacitance on its nodes. The difference in reference for (+) or (-) input voltages will cause a roll-over error. This error can be minimized by using a large reference capacitor in comparison to the stray capacitance. A 1 μf capacitor is suitable.

Phase Control Inputs (A [Pin 12], B[Pin 13])

The A, B unlatched logic inputs select the TSC500 operating phase. The A, B inputs are normally driven by a microprocessor I/O port or peripheral input/output chip.

Comparator Output

By monitoring the comparator output during the fixed signal integrate time the input signal polarity can be determined by the microprocessor controlling the conversion. The comparator output is high for positive signals and low for negative signals during the signal integrate phase (Figure 2).

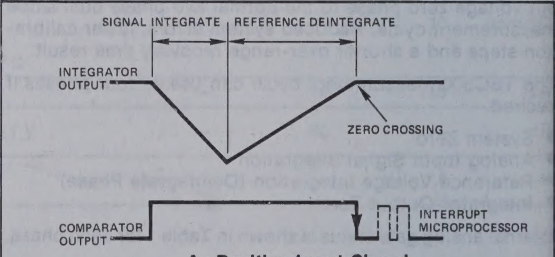
During the variable reference deintegrate phase the comparator output will make a high to low transition as the integrator output ramp crosses zero. This indicates the conversion is complete. The transition can be used to interrupt the processor controlling the conversion.

The internal comparator delay is 4 μsec typically.

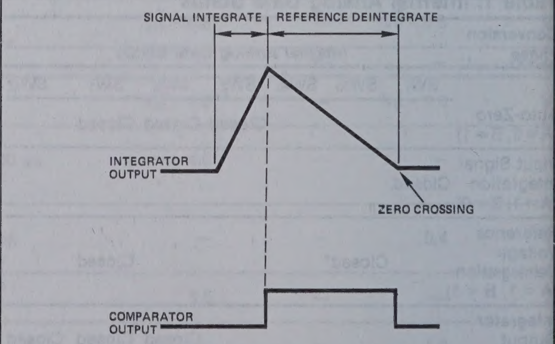
Figure 2 shows the comparator output for large positive and negative signal inputs. For signal inputs at or near zero volts, however, the integrator swing is nonexistent. If common-mode noise is present, the comparator can switch several times during the signal integrate period. To ensure that the polarity reading is correct, the comparator output should be read and stored at the end of Signal Integrate.

TSC500 Comparator Output

Input Signal	Operating Phase	Comparator Output
Positive	Signal Integrate	Logic 1
Negative	Signal Integrate	Logic 0
Positive	Reference Deintegrate	Logic 1 to 0 Transition At Zero-Crossing
Negative	Reference Deintegrate	Logic 1 to 0 Transition At Zero-Crossing



A. Positive Input Signal



B. Negative Input Signal

Figure 2: Comparator Output

Component Value Selection

Integrating Resistor (R_{INT})

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 20 µA drive current with minimal linearity error. R_{INT} is easily calculated for a 20 µA full-scale current:

$$R_{INT}\ (M\Omega) = \frac{\text{Full-Scale Input Voltage (V)}}{20}$$

Reference Capacitor (C_{REF})

A 1.0 µF capacitor is suggested. Larger values may be used to limit roll-over errors. Low leakage capacitors such as polypropylene are suggested.

Auto Zero Capacitor (C_{AZ})

A 1.0 µF polypropylene capacitor is suggested.

Integrating Capacitor (C_{INT})

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.8 V of V_S^+ or V_S^- without saturating.

Using the suggested 20 µA full-scale buffer output current, the integrating capacitor is easily calculated:

$$C_{INT} = \frac{(T)\,(V_{FS})}{\text{Integrator Output Voltage Swing }(R_{INT})}$$

Where T = Integration Period

V_{FS} = Full-Scale Input Voltage

A very important integrating capacitor characteristic is dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

General Theory of Operation
Dual Slope Conversion Principles

The TSC500 is an integrating analog-to-digital converter building block. An understanding of the dual slope conversion technique will aid in following the detailed TSC500 operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The TSC500 automatically switches in the proper polarity reference signal. The reference integration time is directly proportional to the input signal. (Figure 3)

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down." The TSC500 comparator zero-crossing interrupts the processor to indicate the deintegrate cycle is complete.

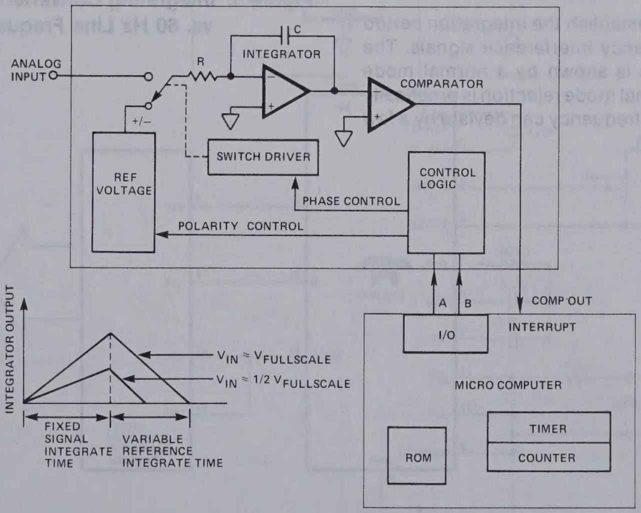

ANALOG INPUT
R
C
INTEGRATOR
COMPARATOR
+/−
SWITCH DRIVER
REF VOLTAGE
CONTROL LOGIC
PHASE CONTROL
POLARITY CONTROL
A
B
COMP OUT
I/O
INTERRUPT
MICRO COMPUTER
TIMER
COUNTER
ROM
INTEGRATOR OUTPUT
$V_{IN} \approx V_{FULLSCALE}$
$V_{IN} \approx 1/2\ V_{FULLSCALE}$
FIXED SIGNAL INTEGRATE TIME
VARIABLE REFERENCE INTEGRATE TIME

Figure 3: Basic Dual Slope Converter with TSC500

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN(t)}\ dt = \frac{V_R T_{RI}}{RC}$$

Where:

V_R = Reference Voltage

T_{SI} = Signal Integration Time (Fixed)

T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{T_{RI}}{T_{SI}}\right]$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle.

An inherent benefit is noise immunity. Input noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments.

Integrating converters provide noise rejection automatically with at least a 20 dB/decade attenuation rate. Interference signals with frequencies at integral multiples of the integration period are theoretically completely removed. This intuitively makes sense, since the average value of a sine wave of frequency 1/T averaged over a period T is zero.

Integrating converters often establish the integration period to reject 50/60 Hz line frequency interference signals. The ability to reject such signals is shown by a normal mode rejection plot (Figure 4). Normal mode rejection is practically set to 50-65 dB, since the line frequency can deviate by a few tenths of a percent (Figure 5).

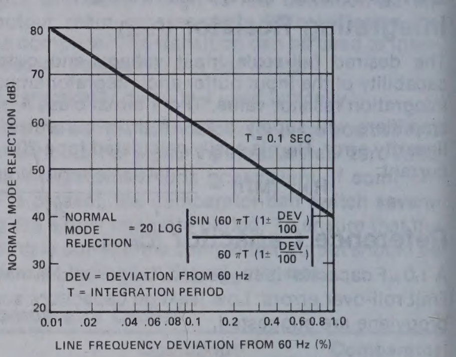


Figure 4: Normal Mode Rejection vs. Input Frequency

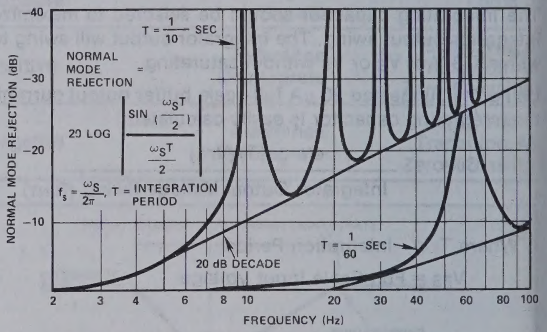
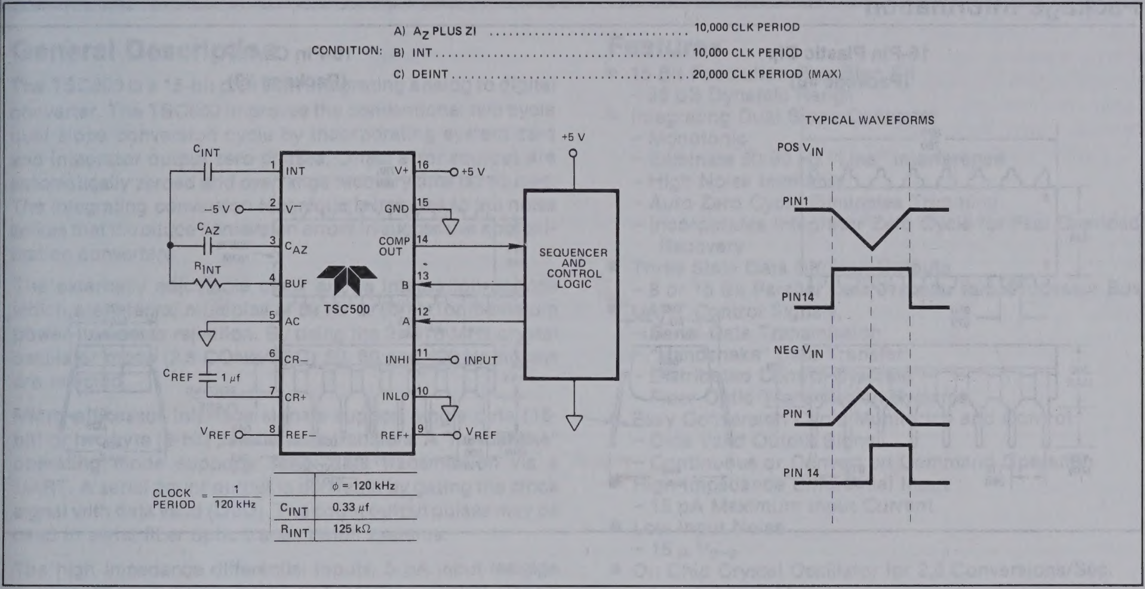


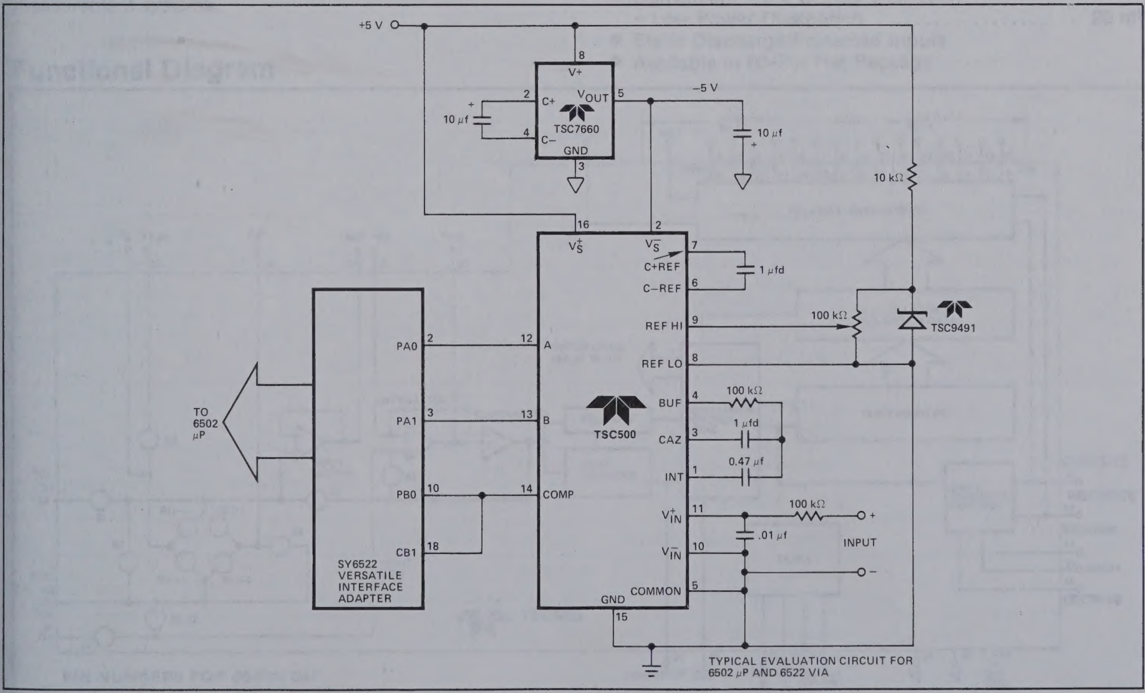
Figure 5: Integrating Converter Normal Mode Rejection vs. 60 Hz Line Frequency Variations.

Test Set Up


CONDITION:
A) A_Z PLUS ZI .... 10,000 CLK PERIOD
B) INT .... 10,000 CLK PERIOD
C) DEINT .... 20,000 CLK PERIOD (MAX)
TYPICAL WAVEFORMS
POS V_{IN}
PIN1
PIN14
NEG V_{IN}
PIN 1
PIN 14
C_{INT}
1 INT
−5 V
2 V^-
C_{AZ}
3 C_{AZ}
R_{INT}
4 BUF
5 AC
6 CR−
C_{REF}
1 μf
7 CR+
V_{REF}
8 REF−
TSC500
+5 V
16 V+
15 GND
14 COMP OUT
13 B
12 A
11 INHI
INPUT
10 INLO
9 REF+
V_{REF}
SEQUENCER AND CONTROL LOGIC
CLOCK PERIOD = 1 / 120 kHz

	ϕ = 120 kHz
C_{INT}	0.33 μf
R_{INT}	125 kΩ

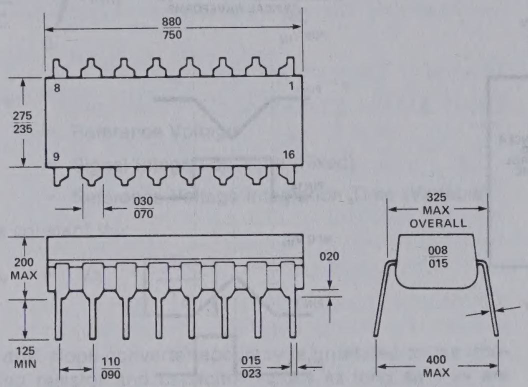
TSC500 to 6522 Peripheral I/O Chip


+5 V
8
V+
2 C+
V_{OUT} 5
−5 V
10 μf
4 C−
TSC7660
GND
3
10 μf
10 kΩ
16 V_S^+
2 V_S^-
7 C+REF
1 μfd
6 C−REF
9 REF HI
100 kΩ
TSC9491
8 REF LO
4 BUF
100 kΩ
1 μfd
3 CAZ
0.47 μf
1 INT
11 V_{IN}^+
100 kΩ
.01 μf
+
INPUT
10 V_{IN}^-
−
5 COMMON
GND 15
TSC500
12 A
13 B
14 COMP
PA0 2
PA1 3
PB0 10
CB1 18
SY6522 VERSATILE INTERFACE ADAPTER
TO 6502 μP

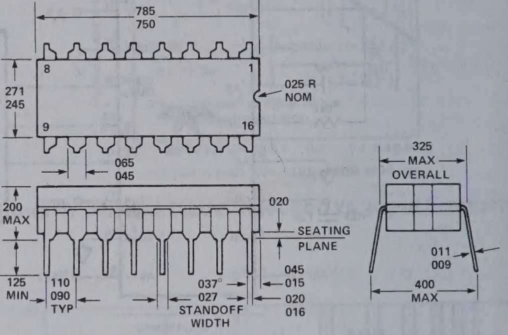
TYPICAL EVALUATION CIRCUIT FOR 6502 μP AND 6522 VIA

Package Information

**16-Pin Plastic Dip
(Package #8)**


880
750
8
1
275
235
9
16
030
070
325
MAX
OVERALL
200
MAX
020
008
015
125
MIN
110
090
015
023
400
MAX

**16-Pin CerDIP
(Package #9)**


785
750
8
1
271
245
025 R
NOM
9
16
065
045
325
MAX
OVERALL
200
MAX
020
SEATING
PLANE
011
009
125
MIN
110
090
TYP
037°
027
STANDOFF
WIDTH
045
015
020
016
400
MAX

TELEDYNE SEMICONDUCTOR

TSC800

15-Bit Plus Sign Integrating Analog to Digital Converter
• BUS Compatible
• UART Interface

General Description

The TSC800 is a 15-bit plus sign integrating analog to digital converter. The TSC800 improves the conventional two cycle dual slope conversion cycle by incorporating system zero and integrator output zero phases. Offset error sources are automatically zeroed and overrange recovery time is reduced. The integrating conversion technique is immune to the noise spikes that introduce conversion errors in successive approximation converters.

The externally adjustable clock allows integration periods which are integral multiples of 50 Hz or 60 Hz for maximum power-line noise rejection. By using the 2.4576 MHz crystal oscillator mode (2.5 CONV/SEC) 50, 60 and 400 Hz signals are rejected.

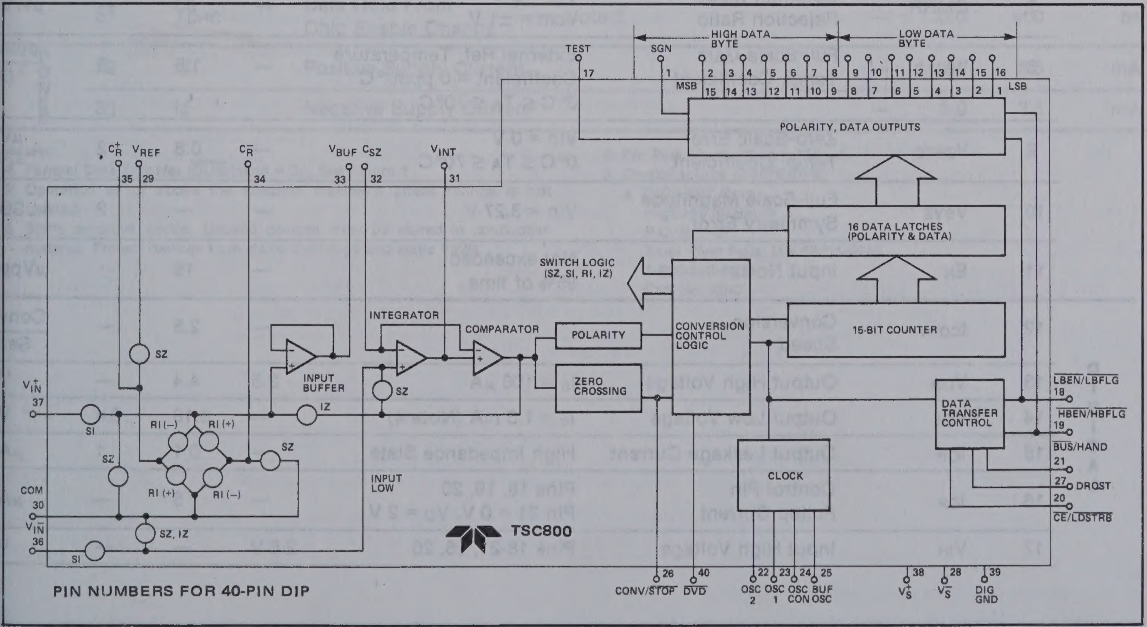
Micro-processor interface signals support single byte (16-bit) or two byte (8-bit) parallel data transfers. A "handshake" operating mode supports serial data transmission via a UART. A serial count output is derivable by gating the clock signal with data valid (DVD). The count output pulses may be used in serial fiber optic transmission systems.

The high impedance differential inputs, 5 pA input leakage current, 16-bit dynamic range and interface control signals make the high resolution TSC800 the ideal analog to digital converter for process control, data logging and "intelligent" measurement systems.

Features

- 15 Bit Resolution Plus Sign Bit
  - 96 dB Dynamic Range
- Integrating Dual Slope Converter
  - Monotonic
  - Eliminate 50/60 Hz "Line" Interference
  - High Noise Immunity
  - Auto Zero Cycle Eliminates Trimming
  - Incorporates Integrator Zero Cycle for Fast Overload Recovery
- Three State Data Bit/Sign Outputs
  - 8 or 16 Bit Parallel Data Transfer to μ-Processor Bus
- UART Control Signals
  - Serial Data Transmission
  - "Handshake" Data Transfer
  - Distributed Control Systems
  - Fiber Optic Transmission Systems
- Easy Conversion Cycle Monitoring and Control
  - Data Valid Output Signal
  - Continuous or Convert on Command Operation
- High Impedance Differential Input
  - 15 pA Maximum Input Current
- Low Input Noise
  - 15 μ V_{p-p}
- On Chip Crystal Oscillator for 2.5 Conversions/Sec.
  - $f_{xtal} = 2.4576$ MHz
  - 100 mSEC Integration Period Rejects 50, 60, 400 Hz Interference Signals
- Convenient ±5 V Supply Operation
  - Low Power Dissipation .... 20 mW
- Static Discharge Protected Inputs
- Available in 60-Pin Flat Package

Functional Diagram


TEST
17
SGN
HIGH DATA BYTE
LOW DATA BYTE
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
MSB
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
LSB
POLARITY, DATA OUTPUTS
16 DATA LATCHES (POLARITY & DATA)
15-BIT COUNTER
C_R^+
V_{REF}
35 29
C_R^-
34
V_{BUF} C_{SZ}
33 32
V_{INT}
31
SWITCH LOGIC (SZ, SI, RI, IZ)
INTEGRATOR
COMPARATOR
POLARITY
ZERO CROSSING
CONVERSION CONTROL LOGIC
INPUT BUFFER
SZ
IZ
SI
RI (–)
RI (+)
V_{IN}^+
37
COM
30
V_{IN}^-
36
SZ, IZ
INPUT LOW
DATA TRANSFER CONTROL
CLOCK
LBEN/LBFLG
18
HBEN/HBFLG
19
BUS/HAND
21
27 DRQST
20
CE/LDSTRB
TSC800
26 CONV/STOP
40 DVD
22 23 24 25
OSC 2
OSC 1
OSC CON
BUF OSC
38 V_S^+
28 V_S^-
39 DIG GND
PIN NUMBERS FOR 40-PIN DIP

15-Bit Plus Sign Integrating Analog to Digital Converter

• BUS Compatible
• UART Interface

TSC800

Absolute Maximum Ratings[2]

Positive Supply Voltage (V_S^+ to Gnd) .... +6.2 V
Negative Supply Voltage (V_S^- to Gnd) .... -9.0 V
Analog Input Voltage (V^+_{IN} or $V_{I\bar{N}}$) .... V_S^+ to V_S^-
Voltage Reference Input (V_{REF}) .... V_S^+ to V_S^-
Logic Input Voltage .... V_S^+ + 0.3 V to Gnd - 0.3 V
Package Power Dissipation
CerDIP Package .... 1 Watt @ +85° C
Plastic Package .... 0.5 Watt @ +70° C
Ambient Operating Temperature Range
CerDIP Package (MJL) .... -55° C to +125° C
(IJL) .... -25° C to +85° C
Plastic Package (CPL, CBQ, CSQ) ... 0° C to +70° C
Storage Temperature .... -55° C to 150° C
Lead Soldering Temperature (60 Seconds) ...... +300° C

Electrical Characteristics:

V_S = ±5 V, Conversion Rate = 2.5 CONV/SEC, Crystal Frequency = 2.4576 MHz, T_A = 25° C, Full-Scale Voltage = 3.2768 V, Note 1.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC800 MIN	TSC800 TYP	TSC800 MAX	UNIT
ANALOG INPUT	1	V_{ZSE}	Zero-Scale Error	Vin = 0 V	—	—	±0.5	LSB
	2	NL	Non-Linearity	Best Straight Line - Full-Scale ≤ V_{IN} ≤ + Full-Scale	—	1.3	2	LSB
	3	NL	Nonlinearity	End Point - Full-Scale ≤ V_{IN} ≤ + Full-Scale	—	2.8	—	LSB
	4	DNL	Differential Nonlinearity		—	—	±0.5	LSB
	5	I_{IN}	Input Current	Vin = 0 V, T_A = 25°C 0° C ≤ T_A ≤ 70° C -25° C ≤ T_A ≤ 85° C -55° C ≤ T_A ≤ 125° C	— — — —	5 25 70 2.5	15 125 175 7.5	pA pA pA nA
	6	V_{CMR}	Common-Mode Input Range	Over Operating Temp. Range	V_S^- +1.5 V	—	V_S^+ -1.0 V	V
	7	CMRR	Common-Mode Rejection Ratio	Vin = 0 V Vcm = ±1 V	—	80	—	μV/V
	8	V_{FSTC}	Full-Scale Gain Temp. Coefficient	External Ref. Temperature Coefficient = 0 ppm/° C 0° C ≤ T_A ≤ 70° C	—	1.5	5	ppm/°C
	9	V_{ZSTC}	Zero-Scale Error Temp. Coefficient	Vin = 0 V 0° C ≤ T_A ≤ 70° C	—	0.8	2	μV/°C
	10	V_{SYE}	Full-Scale Magnitude Symmetry Error	Vin = 3.27 V	—	—	2	LSB
	11	E_N	Input Noise	Not exceeded 95% of time	—	15	—	μVpp
DIGITAL	12	tconv	Conversion Speed		—	2.5	—	Conv/Sec
	13	V_{OH}	Output High Voltage	I_o = 100 μA	3.5	4.4	—	V
	14	V_{OL}	Output Low Voltage	I_o = 1.6 mA (Note 4)	—	0.18	0.4	V
	15	I_{OP}	Output Leakage Current	High Impedance State	—	0.1	1	μA
	16	I_{CP}	Control Pin Pullup Current	Pins 18, 19, 20 Pin 21 = 0 V, V_O = 2 V	—	5	—	μA
	17	V_{IH}	Input High Voltage	Pins 18-21, 26, 26	2.5 V	—	—	V

Electrical Characteristics: $V_S = \pm 5$ V, Conversion Rate = 2.5 CONV/SEC, Crystal Frequency = 2.4576 MHz, $T_A = 25°$ C, Full-Scale Voltage = 3.2768 V, Note 1.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC800			UNIT
					MIN	TYP	MAX	
DIGITAL	18	V_{IL}	Input Low Voltage	Pins 18-21, 26, 27	—	—	1	V
	19	I_{IP}	Input Pin Pullup Current	Pins 26,27 V = 2 V	—	5	—	μA
	20	I_{IP}	Input Pin Pullup Current	Pin 17, 24 V = 2 V	—	25	—	μA
	21	I_{ID}	Input Pin Pulldown Current	Pin 21 V = 3 V	—	5	—	μA
	22	I_{OSCI}	Oscillator Output Current	$V_O = 2.5$ V	—	1.0	—	mA
	23	I_{BUFOSC}	Buffered Oscillator Output Current	$V_O = 2.5$ V	—	5	—	mA
	24	C_{IN}	Input Capacitance	Pin 18, 19	—	—	50	pF
	25	T_{PW}	$\overline{\text{BUS}}$/Hand Control Pin Minimum Pulse Width	Pin 21	70	—	—	ns
	26	T_{WBE}	Byte Enable Pulse width	Note 1	350	200	—	ns
	27	T_{WCE}	Chip Enable Pulse Width	Note 1	400	250	—	ns
	28	T_{ABE}	Byte Enable Access Time	Note 1	—	200	350	ns
	29	T_{ACE}	Chip Enable Access Time	Note 1	—	250	400	ns
	30	T_{DHB}	Data Hold From Byte Enable Change	Note 1	—	140	300	ns
	31	T_{DHC}	Data Hold From Chip Enable Change	Note 1	—	240	400	ns
POWER	32	I_S^+	Positive Supply Current		—	2.0	3.5	mA
	33	I_S^-	Negative Supply Current		—	2.0	3.5	mA

Notes:
1. Parallel Data Transfer ($\overline{\text{BUS}}$/Hand = 0.). See Figure 1
2. Operation at or above the absolute maximum stress ratings is not implied.
3. Static sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields.
4. For Pins 18, 19, 20 $I_O = 750$ μA.
5. Crystal source (2.4576 mHz)
   a. DIGI-KEY Corp
   Highway 32 South
   P.O. Box 677
   Thief River Falls, MN 56701-9988
   1-800-344-4539
   Part No. X047

Pin Description and Function

PIN NO. 40-Pin DIP)	PIN NO. (60-Pin FP)	SYMBOL	DESCRIPTION
1	9	SGN	Sign Bit: 1 = Positive Input. The input signal polarity is determined at the end of the signal integrate phase.
2	10	DB_{15}	Data Bit 15 (MSB): Three State Output Data Bit
3	11	DB_{14}	14
4	12	DB_{13}	13
5	13	DB_{12}	12
6	18	DB_{11}	11
7	19	DB_{10}	10 NOTE: DB_{15} -DB, are at a logic "1" state for an overrange conversion.
8	20	DB_9	9
9	21	DB_8	8
10	22	DB_7	7
11	24	DB_6	6
12	25	DB_5	5
13	26	DB_4	4
14	27	DB_3	3
15	28	DB_2	2
16	33	DB_1	1 (LSB)
17	34	Test	Test: 0 V; Data Outputs forced to Logic 1 and clock is disabled Test = V^+; Counter latches enabled.
18	35	$\overline{\text{LBEN}}$/$\overline{\text{LBFLG}}$ (Input/Output)	A low data byte enable input or flag output depending on $\overline{\text{BUS}}$/HAND (Pin 21) status 1. $\overline{\text{BUS}}$/HAND = 0: With Pin 21 low and $\overline{\text{CE}}$/$\overline{\text{LDSTRB}}$ = 0 (Pin 20) data bits 8 through 1 are output (pins 9 - 16) when the input pin $\overline{\text{LBEN}}$ = 0. 2. $\overline{\text{BUS}}$/HAND = 1: Valid data on pins 9 - 16 is indicated by the flag output $\overline{\text{LBFLG}}$ = 0.
18	36	$\overline{\text{HBEN}}$/$\overline{\text{HBFLG}}$ (Input/Output)	A high data byte enable input or flag output depending on BUS/HAND (pin 21) status. 1. $\overline{\text{BUS}}$/HAND = 0: With pin 21 low and $\overline{\text{CE}}$/$\overline{\text{LDSTRB}}$ = 0 (pin 20) the high data byte (Sign Bit plus Data Bits 15 - 9) are output when the input $\overline{\text{HBEN}}$ = 0 2. $\overline{\text{BUS/HAND}}$ = 1: Valid Data on pins 1 - 8 is indicated by the flag output $\overline{\text{HBLFG}}$ = 0.
20	37	$\overline{\text{CE}}$/$\overline{\text{LDSTRB}}$ (Input/Output)	1. $\overline{\text{BUS}}$/HAND = 0: $\overline{\text{CE}}$ is master chip enable, With $\overline{\text{CE}}$ = 1 sign bit plus DB_{15} - DB_1 are disabled (Hi-Impedance State). $\overline{\text{CE}}$ = 0 enables outputs and data is transferred under control of $\overline{\text{LBEN}}$ and $\overline{\text{HBEN}}$ input signals.

$\overline{\text{CE}}$	$\overline{\text{LBEN}}$	$\overline{\text{HBEN}}$	FUNCTION
0	0	1	Low Data Byte Output
0	1	0	High Data Byte Output
0	0	0	Low + High Data Byte Output
0	1	1	High Impedance State

2. $\overline{\text{BUS}}$/HAND = 1: $\overline{\text{LDSTRB}}$ is a load strobe output sign. In the handshake mode, $\overline{\text{LDSTRB}}$ = 0 output signal instructs the receiving device to accept data.

Note:
Pin connections in description section refer to 40-pin package.

Pin Description and Function (Cont.)

PIN NO. 40-Pin DIP)	PIN NO. (60-Pin FP)	SYMBOL	DESCRIPTION
21	39	$\overline{BUS}$/HAND	1. $\overline{BUS}$ = 0: Parallel output data mode where the $\overline{CE}$, $\overline{HBEN}$, and $\overline{LBEN}$ signals are inputs that directly control the 16 data bits. 2. HAND = 1: $\overline{LDSTRB}$, $\overline{LBFLG}$, $\overline{HBFLG}$ are outputs used in the handshake data transfer mode. 3. Hand = __|‾|__ (Pulsed High): Causes entry into handsake mode for UART interfacing.
22	40	OSC_2	Oscillator input
23	41	OSC_1	Oscillator output
24	42	OSC CON	Selects internal oscillator structure 1. OSC CON = 1: RC oscillator. Internal clock frequency is same frequency and duty cycle as BUF OSC. 2. OSC CON = 0: Crystal oscillator, Internal clock frequency is frequency at BUF OSC ÷ 15.
25	43	BUFOSC	Buffered oscillator output
26	48	CONVERT/$\overline{STOP}$	CONVERT = 1: Conversions performed continuously. $\overline{STOP}$ = 0: Conversion process stops 7 counts before entering signal integrate phase. The conversion in progress when $\overline{STOP}$ = 0 is completed.
27	49	DRQST	DATA OUTPUT request signal. An input used in the handshake mode that indicates an external device is ready to accept data. If DRQST is not used connect to V_S^+.
28	50	V_S^-	Negative power supply
29	51	V_{REF}	Voltage reference input
30	52	COM	Analog common. The TSC800 is auto-zeroed to the analog common potential.
31	54	V_{INT}	Integrator output
32	55	C_{SZ}	SYSTEM-ZERO capacitor
33	56	V_{BUF}	Output of input signal buffer
34	57	C_R^-	Reference capacitor
35	59	C_R^+	Reference capacitor
36	1	V_{IN}^-	Negative differential analog input
37	3	V_{IN}^+	Positive differential analog input
38	5	V_S^+	Positive power supply
39	6	GND	Digital ground. Ground return point for Digital logic.
40	7	$\overline{DVD}$	DATA VALID SIGNAL: $\overline{DVD}$ = 1 during signal integrate and reference integrate phases until data is latched. $\overline{DVD}$ = 0 when in auto zero-phase. Data does not change when $\overline{DVD}$ = 0.

Note:
Pin connections in description section refer to 40-pin package.

General Theory of Operation

Dual Slope Conversion Principles

The TSC800 is a dual slope, integrating analog to digital converter. An understanding of the dual slope conversion technique will aid in following the detailed TSC800 operation theory.

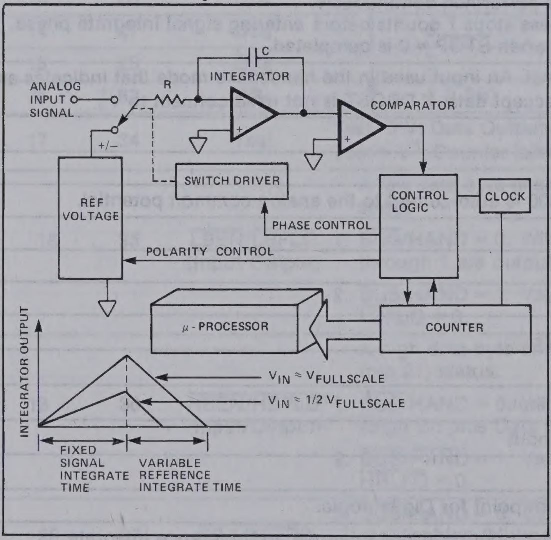
The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

Basic Dual Slope Converter


ANALOG INPUT SIGNAL
R
C
INTEGRATOR
COMPARATOR
+/−
SWITCH DRIVER
REF VOLTAGE
CONTROL LOGIC
CLOCK
PHASE CONTROL
POLARITY CONTROL
μ - PROCESSOR
COUNTER
INTEGRATOR OUTPUT
$V_{IN} \approx V_{FULLSCALE}$
$V_{IN} \approx 1/2\ V_{FULLSCALE}$
FIXED SIGNAL INTEGRATE TIME
VARIABLE REFERENCE INTEGRATE TIME

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments.

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_{0}^{T_{SI}} V_{IN}(t)\,dt = \frac{V_R\, T_{RI}}{RC}$$

where:

V_R = Reference Voltage

T_{SI} = Signal Integration Time (Fixed)

T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R \left[\frac{T_{RI}}{T_{SI}}\right]$$

TSC800 Analog Input Description

System Zero Phase (Figure 3A)

During this phase errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{SZ} (system-zero capacitor) with a compensating error voltage. With a zero input voltage the integrator output will remain at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{SZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

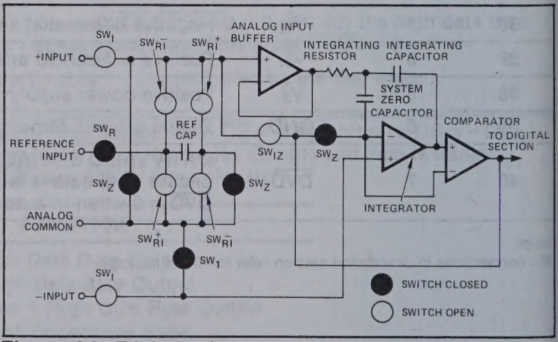

+INPUT
SW_I
SW_{RI}^-
SW_{RI}^+
ANALOG INPUT BUFFER
INTEGRATING RESISTOR
INTEGRATING CAPACITOR
SYSTEM ZERO CAPACITOR
REF CAP
REFERENCE INPUT
SW_R
SW_{IZ}
SW_Z
COMPARATOR
TO DIGITAL SECTION
INTEGRATOR
ANALOG COMMON
SW_{RI}^+
SW_{RI}^-
SW_1
−INPUT
SWITCH CLOSED
SWITCH OPEN

Figure 3A: TSC800 System Zero Phase

Analog Input Signal Integration Phase (Figure 3B)

The TSC800 integrates the differential voltage between the + input and - input. The differential voltage must be within the device common-mode range; 1 V from either supply rail typically. The input signal is integrated for 16, 384 clock cycles.

The input signal polarity is determined at the end of the phase.

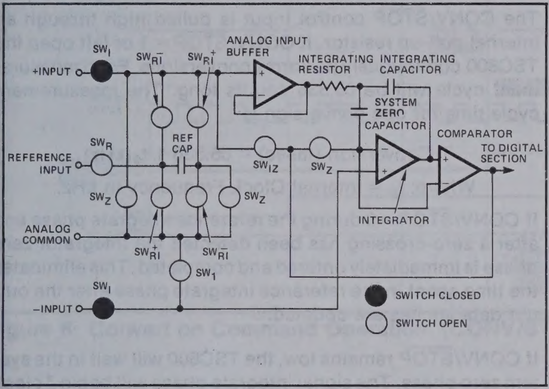

SW$_I$
+INPUT
SW$_{RI}^-$
SW$_{RI}^+$
ANALOG INPUT BUFFER
INTEGRATING RESISTOR
INTEGRATING CAPACITOR
SYSTEM ZERO CAPACITOR
SW$_R$
REF CAP
REFERENCE INPUT
SW$_{IZ}$
SW$_Z$
COMPARATOR
TO DIGITAL SECTION
SW$_Z$
SW$_Z$
ANALOG COMMON
INTEGRATOR
SW$_{RI}^+$
SW$_{RI}^-$
SW$_1$
SW$_I$
-INPUT
SWITCH CLOSED
SWITCH OPEN

Figure 3B: TSC800 Input Signal Integration Phase

Reference Voltage Integration (Figure 3C)

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. The time for the output to return to zero is proportional to the input signal magnitude. The phase lasts for a maximum of 32, 768 clock periods.

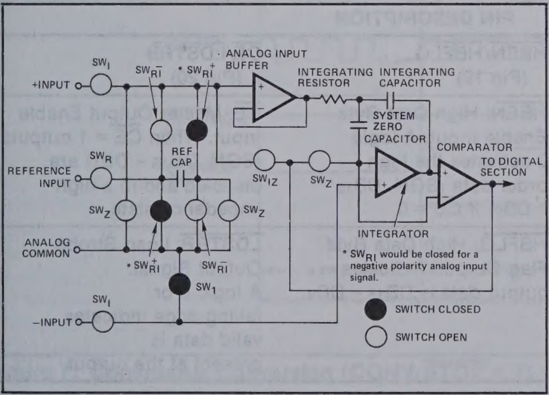

SW$_I$
+INPUT
SW$_{RI}^-$
• SW$_{RI}^+$
ANALOG INPUT BUFFER
INTEGRATING RESISTOR
INTEGRATING CAPACITOR
SYSTEM ZERO CAPACITOR
SW$_R$
REF CAP
REFERENCE INPUT
SW$_{IZ}$
SW$_Z$
COMPARATOR
TO DIGITAL SECTION
SW$_Z$
SW$_Z$
ANALOG COMMON
INTEGRATOR
• SW$_{RI}^+$
SW$_{RI}^-$
SW$_1$
SW$_I$
-INPUT
* SW$_{RI}$ would be closed for a negative polarity analog input signal.
SWITCH CLOSED
SWITCH OPEN

Figure 3C: TSC800 Reference Voltage Integration Cycle

Integrator Output Zero (Figure 3D)

This phase guarantees the integrator output is at zero volts when the system zero phase is entered and that the true system offset voltages are compensated for. This phase normally lasts 4096 clock cycles.

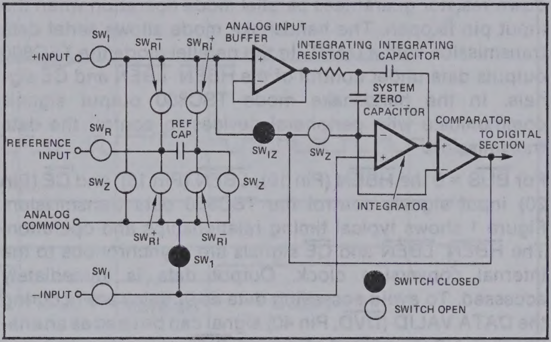

SW$_I$
+INPUT
SW$_{RI}^-$
SW$_{RI}^+$
ANALOG INPUT BUFFER
INTEGRATING RESISTOR
INTEGRATING CAPACITOR
SYSTEM ZERO CAPACITOR
SW$_R$
REF CAP
REFERENCE INPUT
SW$_{IZ}$
SW$_Z$
COMPARATOR
TO DIGITAL SECTION
SW$_Z$
SW$_Z$
ANALOG COMMON
INTEGRATOR
SW$_{RI}^+$
SW$_{RI}^-$
SW$_1$
SW$_I$
-INPUT
SWITCH CLOSED
SWITCH OPEN

Figure 3D: TSC800 Integrator Output Zero Phase

Differential Inputs (V_{IN}^+ (Pin 37) and V_{IN}^- (Pin 36))

The TSC800 operates with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 1.0 V below the positive supply to 1.0 V above the negative supply. Within this common-mode voltage range an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst case condition exists, for example, when a large positive common-mode voltage with a near full scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced. The integrator output can swing within 0.4 volts of either supply without loss of linearity.

Analog Common (Pin 30)

Analog common is used as the V_{IN}^- return during system-zero and reference-integrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications V_{IN}^- will be set at a fixed known voltage (power supply common, for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to analog common.

Digital Section Description

Digital Control Signals

$\overline{\text{BUS}}$/Hand (Pin 21)

The $\overline{\text{BUS}}$/Hand input signal selects the parallel BUS data transfer mode or handshake transfer mode. An internal pull-down resistor guarantees parallel mode operation when the input pin is open. The handshake mode allows serial data transmission with a UART. In the parallel mode the TSC800 outputs data under control of the $\overline{\text{HBEN}}$, $\overline{\text{LBEN}}$ and $\overline{\text{CE}}$ signals. In the handshake mode TSC800 output signals communicate with peripheral devices to control the data transmission.

For $\overline{\text{BUS}}$ = 0 the $\overline{\text{HBEN}}$ (Pin 19), $\overline{\text{LBEN}}$ (Pin 18), and $\overline{\text{CE}}$ (Pin 20) input signals control the TSC800 data transmission. Figure 1 shows typical timing relationships and operation. The $\overline{\text{HBEN}}$, $\overline{\text{LBEN}}$ and $\overline{\text{CE}}$ signals are asynchronous to the internal conversion clock. Output data is immediately accessed. To avoid accessing data as updates are occuring the DATA VALID ($\overline{\text{DVD}}$, Pin 40) signal can be used as an enable signal. Data will not change if $\overline{\text{DVD}}$ = 0.

In the handshake mode two data transfer methods are possible. If HAND is pulsed high (HAND = ⎍) for a minimum of 70 nsec the TSC800 enters the handshake mode. If HAND = 1 continuously the parallel mode is not re-entered, and a handshake data transfer will occur at the end of each conversion cycle.

The $\overline{\text{BUS}}$/Hand input signal configures dual purpose pins 18, 19 and 20 as inputs or outputs. In conjunction with the DATA REQUEST (DRQST, Pin 27) input signal the handshake data transfer is controlled by the output signals: $\overline{\text{LBFLG}}$, $\overline{\text{HBFLG}}$, and $\overline{\text{LDSTRB}}$.

Data Request Input (DRQST, Pin 27)

This input is used only in the handshake data transfer mode. a DRQST = 1 input signal indicates an external receiving device is ready to accept data from the TSC800. It serves as a send data command. When $\overline{\text{BUS}}$/HAND = 0, DRQST should be tied to V_S^+.

Convert/$\overline{\text{Stop}}$ Input (CONV/$\overline{\text{STOP}}$, Pin 26)

The CONV/$\overline{\text{STOP}}$ control input is pulled high through an internal pull-up resistor. If CONV/$\overline{\text{STOP}}$ = 1 or left open the TSC800 continuously performs conversions. Each measurement cycle will be 65,536 counts long. The measurement cycle time for one conversion is:

$$T\ \text{Conversion (msec)} = 65.536\ 1/f_c(\text{kHz})$$

Where: f_c = Internal Clock Frequency in kHz.

If CONV/$\overline{\text{STOP}}$ = 0 during the reference integrate phase and after a zero-crossing has been detected the integrator zero phase is immediately entered and completed. This eliminates the time spent in the reference integrate phase after the output data latches are updated.

If CONV/$\overline{\text{STOP}}$ remains low, the TSC800 will wait in the system zero phase. The signal integrate phase will begin 7 clock counts after a CONV = 1 signal is detected. The CONV/$\overline{\text{STOP}}$ signal is detected synchronously with the internal clock. The system zero phase should last a minimum of 70 msec. See Figures 6 and 7 for CONV/$\overline{\text{STOP}}$ conversion timing diagrams.

If CONV/$\overline{\text{STOP}}$ goes low and remains low during the system zero phase, the TSC800 will stop at the end of the phase and wait for CONV = 1. The signal integrate phase will start seven clock counts after CONV = 1 is detected.

OPERATING MODE	PIN DESCRIPTION		
$\overline{\text{BUS}}$ Transfer Mode	$\overline{\text{LBEN}}$/$\overline{\text{LBFLG}}$ (Pin 18)	$\overline{\text{HBEN}}$/$\overline{\text{HBFLG}}$ (Pin 19)	$\overline{\text{CE}}$/$\overline{\text{LDSTRB}}$ (Pin 20)
$\overline{\text{BUS}}$/HAND = 0	$\overline{\text{LBEN}}$: Low Data Byte Enable Input. A logic 0 activates the low order data (DB$_8$ - DB$_1$) if $\overline{\text{CE}}$ = 0.	$\overline{\text{HBEN}}$: High Data Byte Enable Input. A logic 0 activates the high order data (SGN, DB$_{15}$ - DB$_9$) if $\overline{\text{CE}}$ = 0.	$\overline{\text{CE}}$: Master Output Enable Input. When $\overline{\text{CE}}$ = 1 outputs (SGN, DB$_{15}$ - DB$_1$) are disabled and in a high impedance state.
Handshake Transfer Mode $\overline{\text{BUS}}$/HAND = 1 or ⎍	$\overline{\text{LBFLG}}$: Low Data Byte Flag Output. Indicates output data is DB$_8$ - DB$_1$.	$\overline{\text{HBFLG}}$: High Data Byte Flag Output. Indicates output data is DB$_{15}$ - DB$_9$.	$\overline{\text{LDSTRB}}$: Load Strobe Output Signal. A logic 0 or falling edge indicates valid data is present at the output.

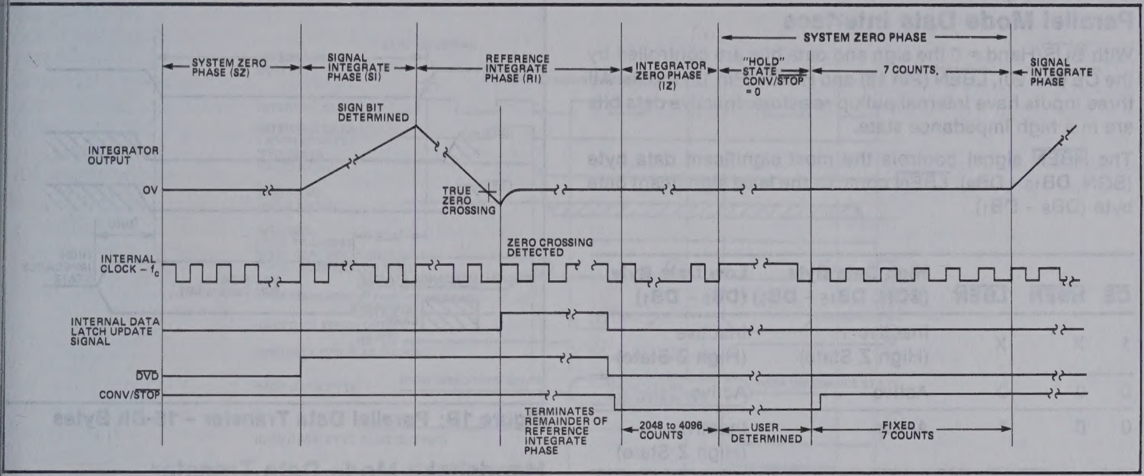

SYSTEM ZERO PHASE (SZ)
SIGNAL INTEGRATE PHASE (SI)
REFERENCE INTEGRATE PHASE (RI)
INTEGRATOR ZERO PHASE (IZ)
"HOLD" STATE CONV/STOP = 0
SYSTEM ZERO PHASE
7 COUNTS
SIGNAL INTEGRATE PHASE
SIGN BIT DETERMINED
INTEGRATOR OUTPUT
OV
TRUE ZERO CROSSING
ZERO CROSSING DETECTED
INTERNAL CLOCK – f_c
INTERNAL DATA LATCH UPDATE SIGNAL
DVD
CONV/STOP
TERMINATES REMAINDER OF REFERENCE INTEGRATE PHASE
2048 to 4096 COUNTS
USER DETERMINED
FIXED 7 COUNTS

Figure 6: Convert on Command Operation. (CONV/$\overline{\text{STOP}}$ = 0 After Zero Crossing Detected)

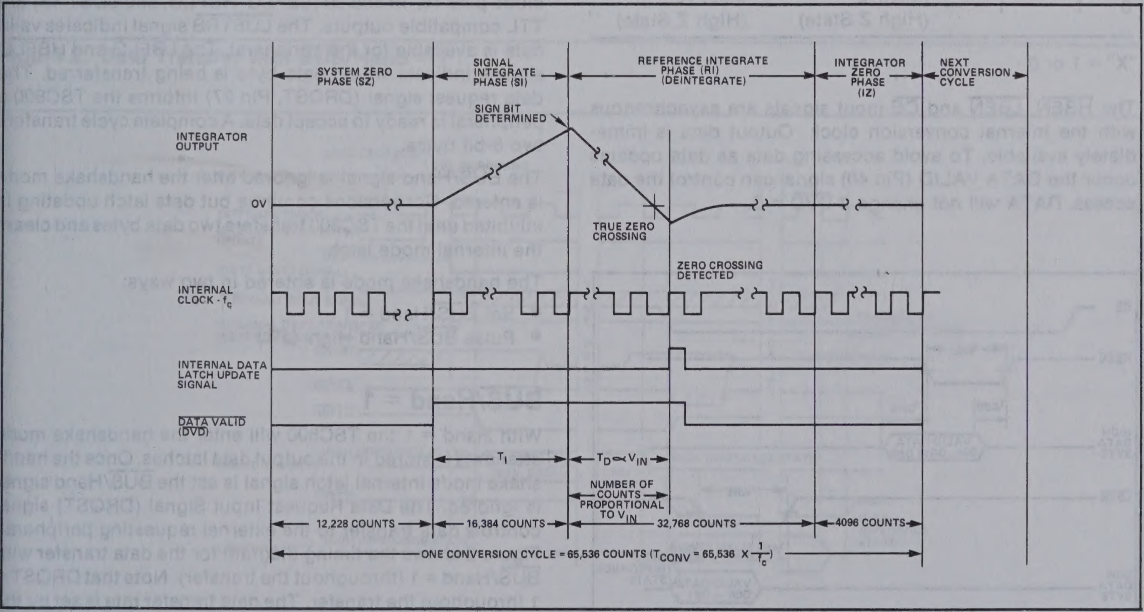

SYSTEM ZERO PHASE (SZ)
SIGNAL INTEGRATE PHASE (SI)
REFERENCE INTEGRATE PHASE (RI) (DEINTEGRATE)
INTEGRATOR ZERO PHASE (IZ)
NEXT CONVERSION CYCLE
SIGN BIT DETERMINED
INTEGRATOR OUTPUT
OV
TRUE ZERO CROSSING
ZERO CROSSING DETECTED
INTERNAL CLOCK - f_c
INTERNAL DATA LATCH UPDATE SIGNAL
DATA VALID (DVD)
T_I
$T_D \propto V_{IN}$
NUMBER OF COUNTS PROPORTIONAL TO V_{IN}
12,228 COUNTS
16,384 COUNTS
32,768 COUNTS
4096 COUNTS
ONE CONVERSION CYCLE = 65,536 COUNTS (T_{CONV} = 65,536 X $\frac{1}{f_c}$)

Figure 7: Continuous Conversion (CONV/$\overline{\text{STOP}}$ = 1)

Test Input (Pin 17)

When Test = 1 the counter data latches are enabled. If Test = 0 the counter outputs are forced to a 1 state and the internal clock is disabled. When Test is returned to a logic 1 and one clock pulse is applied all the counter outputs are clocked low.

Data Valid ($\overline{\text{DVD}}$, Pin 40)

$\overline{\text{DVD}}$ = 1 at the start of signal integrate and $\overline{\text{DVD}}$ = 0 one half clock period after new data is stored in the data latches. Since $\overline{\text{DVD}}$ is always low when data is not changing the signal may be used as a "Data Valid Flag". See Figures 6 and 7 for timing relationships.

Data Output Description

Parallel Mode Data Interface

With $\overline{\text{BUS}}$/Hand = 0 the sign and data bits are controlled by the $\overline{\text{CE}}$ (Pin 20), $\overline{\text{LBEN}}$ (Pin 18) and $\overline{\text{HBEN}}$ (Pin 19) inputs. All three inputs have internal pullup resistors. Inactive data bits are in a high impedance state.

The $\overline{\text{HBEN}}$ signal controls the most significant data byte (SGN, DB_{15} - DB_9). $\overline{\text{LBEN}}$ controls the least significant data byte (DB_8 - DB_1).

$\overline{\text{CE}}$	$\overline{\text{HBEN}}$	$\overline{\text{LBEN}}$	High Data Byte (SGN, DB_{15} - DB_9)	Low Data Byte (DB_8 - DB_1)
1	X	X	Inactive (High Z State)	Inactive (High Z State)
0	0	0	Active	Active
0	0	1	Active	Inactive (High Z State)
0	1	0	Inactive (High Z State)	Active
0	1	1	Inactive (High Z State)	Inactive (High Z State)

"X" = 1 or 0

The $\overline{\text{HBEN}}$, $\overline{\text{LBEN}}$ and $\overline{\text{CE}}$ input signals are asynchronous with the internal conversion clock. Output data is immediately available. To avoid accessing data as data updates occur the DATA VALID (Pin 40) signal can control the data access. DATA will not change if $\overline{\text{DVD}}$ = 0.

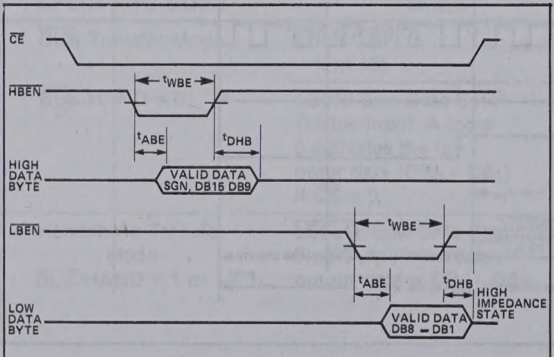


Figure 1A: Parallel Data Transfer - Two 8-Bit Bytes

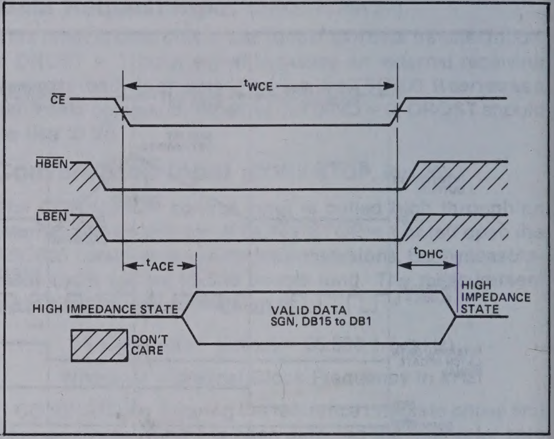


Figure 1B: Parallel Data Transfer - 16-Bit Bytes

Handshake Mode Data Transfer

The TSC800 actively controls the data transfer to peripherals through the handshake data transfer mode. In the handshake mode pins 18, 19 and 20 ($\overline{\text{LBFLG}}$, $\overline{\text{HBFLG}}$, and $\overline{\text{LDSTRB}}$) are TTL compatible outputs. The $\overline{\text{LDSTRB}}$ signal indicates valid data is available for the peripheral. The $\overline{\text{LBFLG}}$ and $\overline{\text{HBFLG}}$ signals indicate which data byte is being transferred. The data request signal (DRQST, Pin 27) informs the TSC800 a peripheral is ready to accept data. A complete cycle transfers two 8-bit bytes.

The $\overline{\text{BUS}}$/Hand signal is ignored after the handshake mode is entered. Conversions continue but data latch updating is inhibited until the TSC800 transfers two data bytes and clears the internal mode latch.

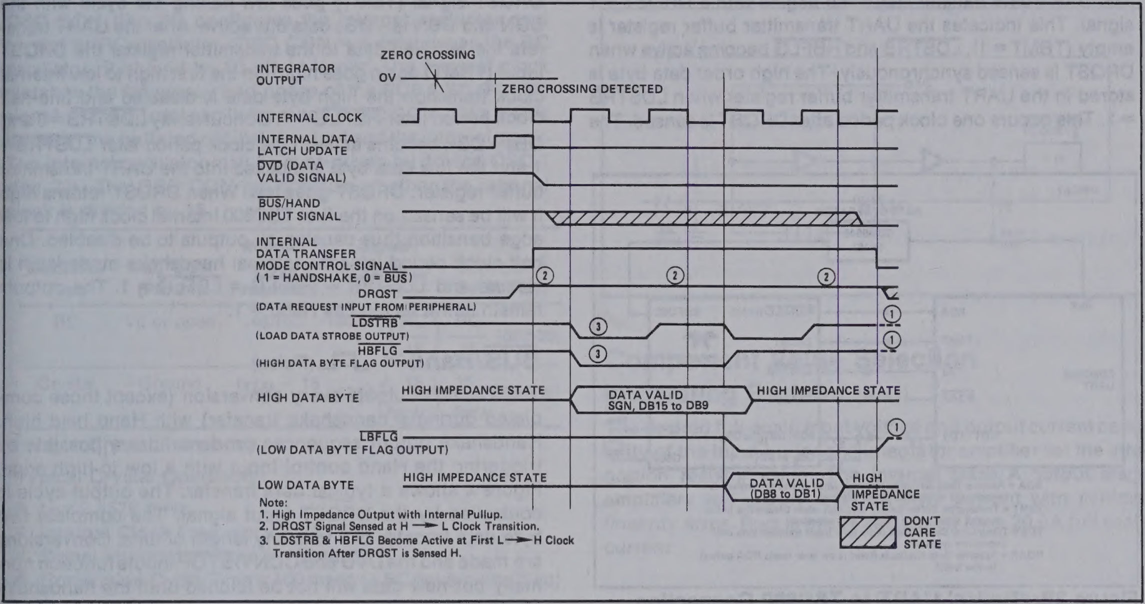
The handshake mode is entered in two ways:

- Set $\overline{\text{BUS}}$/Hand = 1
- Pulse $\overline{\text{BUS}}$/Hand High (⎍)

$\overline{\text{BUS}}$/Hand = 1

With Hand = 1 the TSC800 will enter the handshake mode after data is stored in the output data latches. Once the handshake mode internal latch signal is set the $\overline{\text{BUS}}$/Hand signal is ignored. The Data Request Input Signal (DRQST) signal controls data transfer to the external requesting peripheral. Figure 2 shows the timing diagram for the data transfer with $\overline{\text{BUS}}$/Hand = 1 (throughout the transfer). Note that DRQST = 1 throughout the transfer. The data transfer rate is set by the TSC800 internal clock. A complete data transfer occurs in 4 clock periods after a DRQST = 1 is detected on a high to low internal clock edge transition.

For peripherals that cannot accept data at the TSC800 clock rate the DRQST input signal can be used to delay the transmit sequence. This mode is useful in interfacing to UARTS. Figure 3 shows a typical 2502 UART interface.


ZERO CROSSING
INTEGRATOR OUTPUT
0V
ZERO CROSSING DETECTED
INTERNAL CLOCK
INTERNAL DATA LATCH UPDATE
DVD (DATA VALID SIGNAL)
BUS/HAND INPUT SIGNAL
INTERNAL DATA TRANSFER MODE CONTROL SIGNAL (1 = HANDSHAKE, 0 = BUS)
DRQST
(DATA REQUEST INPUT FROM PERIPHERAL)
LDSTRB
(LOAD DATA STROBE OUTPUT)
HBFLG
(HIGH DATA BYTE FLAG OUTPUT)
②
③
①
HIGH DATA BYTE
HIGH IMPEDANCE STATE
DATA VALID SGN, DB15 to DB9
HIGH IMPEDANCE STATE
LBFLG
(LOW DATA BYTE FLAG OUTPUT)
LOW DATA BYTE
HIGH IMPEDANCE STATE
DATA VALID (DB8 to DB1)
HIGH IMPEDANCE STATE
DON'T CARE STATE

Note:
1. High Impedance Output with Internal Pullup.
2. DRQST Signal Sensed at H ⟶ L Clock Transition.
3. LDSTRB & HBFLG Become Active at First L ⟶ H Clock Transition After DRQST is Sensed H.

Figure 2: Data Transfer with BUS/Hand = 1

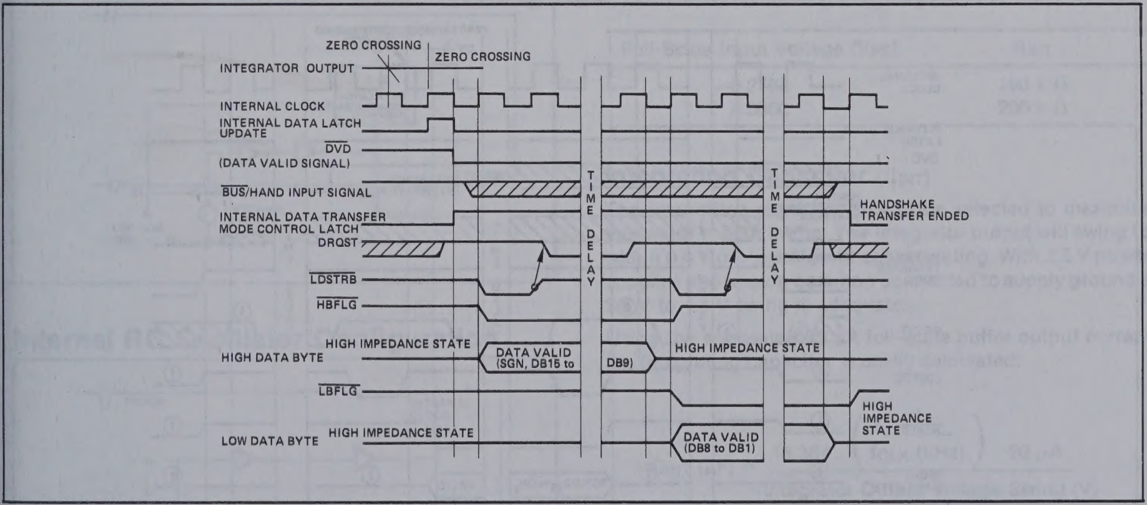
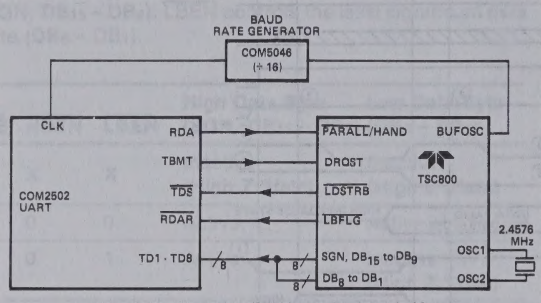

ZERO CROSSING
ZERO CROSSING
INTEGRATOR OUTPUT
INTERNAL CLOCK
INTERNAL DATA LATCH UPDATE
DVD
(DATA VALID SIGNAL)
BUS/HAND INPUT SIGNAL
INTERNAL DATA TRANSFER MODE CONTROL LATCH
DRQST
LDSTRB
HBFLG
TIME DELAY
TIME DELAY
HANDSHAKE TRANSFER ENDED
HIGH DATA BYTE
HIGH IMPEDANCE STATE
DATA VALID (SGN, DB15 to
DB9)
HIGH IMPEDANCE STATE
LBFLG
LOW DATA BYTE
HIGH IMPEDANCE STATE
DATA VALID (DB8 to DB1)
HIGH IMPEDANCE STATE

Figure 3A: Typical UART Interface Timing with DRQST Signal Controlling Data Transfer Timing

The UART data transfer sequence begins with a DRQST = 1 signal. This indicates the UART transmitter buffer register is empty (TBMT = 1). $\overline{LDSTRB}$ and $\overline{HBFLG}$ become active when DRQST is sensed synchronously. The high order data byte is stored in the UART transmitter buffer register when $\overline{LDSTRB}$ = 1. This occurs one clock period after DRQST is sensed. The


BAUD RATE GENERATOR
COM5046
(÷ 16)
CLK
RDA
TBMT
TDS
RDAR
TD1 · TD8
8
COM2502 UART
PARALL/HAND
BUFOSC
DRQST
LDSTRB
LBFLG
TSC800
2.4576 MHz
OSC1
OSC2
SGN, DB15 to DB9
DB8 to DB1
8
8

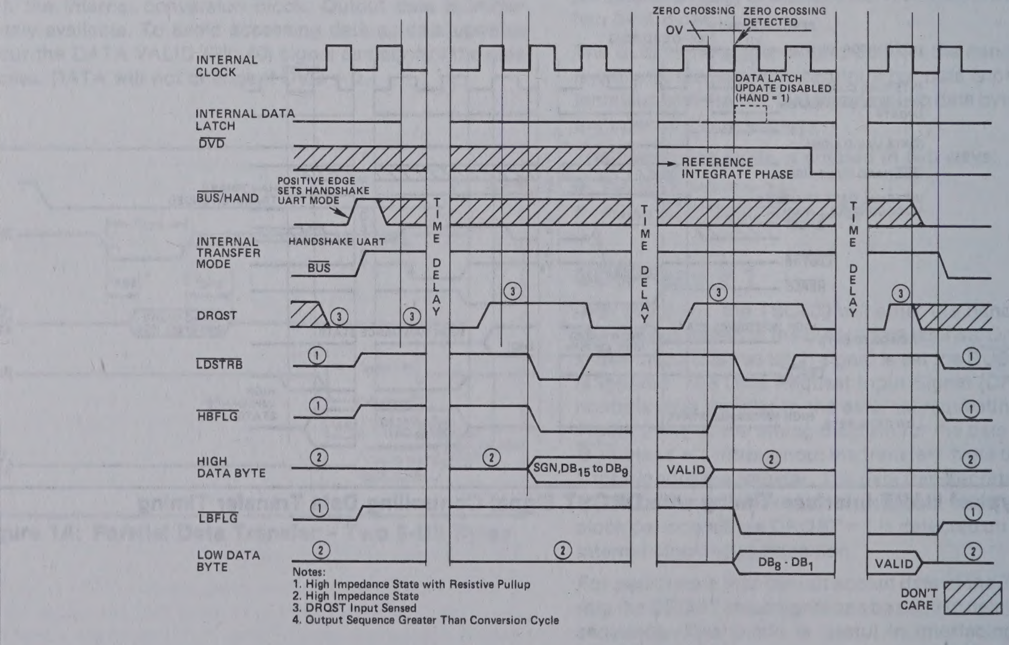
RDA = Receiver Data Available (Set high when character received & transferred to receiver buffer register)
TBMT = Transmitter Buffer Empty (Set high when transmitter buffer register available for loading with new data)
TDS = Transmitter Data Strobe (Low level input transfers data into transmitter register)
RDAR = Receiver Data Available Reset (Low lever resets RDA output to low level)

Figure 3B: Typical UART to TSC800 Connection

DRQST signal (TBMT) goes low halting the cycle with th SGN and DBN $_{15}$ - DB $_9$ data bits active. After the UART trans fers the received data to the transmitter register the DRQS input (TBMT) again goes high. On the first high to low interna clock transition the high byte data is disabled and one-ha clock period later $\overline{HBFLG}$ = 1. Concurrently $\overline{LDSTRB}$ = 0 an DB $_8$ - DB $_1$, become active. One clock period later $\overline{LDSTRB}$ 1 and the low data byte is clocked into the UART transmitte buffer register. DRQST goes low. When DRQST returns hig it will be sensed on the first TSC800 internal clock high to lo edge transition thus causing all outputs to be disabled. On half clock period later the internal handshake mode latch cleared and $\overline{LDSTRB}$ = $\overline{HBFLG}$ = $\overline{LBFLG}$ = 1. The output remain active as long as Hand = 1.

$\overline{BUS}$/Hand = ⎍ (Pulse)

The TSC800 outputs every conversion (except those com pleted during a handshake transfer) with Hand held hig Handshake output sequences on demand are possible b triggering the Hand control input with a low to high edg Figure 4 shows a typical data transfer. The output cycle controlled by the DRQST input signal. The complete tw byte data transfer can take any length of time. Conversion are made and the $\overline{DVD}$ and CONV/$\overline{STOP}$ inputs function no mally but new data will not be latched until the handshak mode is terminated.


ZERO CROSSING
ZERO CROSSING DETECTED
OV
INTERNAL CLOCK
DATA LATCH UPDATE DISABLED (HAND = 1)
INTERNAL DATA LATCH
DVD
REFERENCE INTEGRATE PHASE
POSITIVE EDGE SETS HANDSHAKE UART MODE
BUS/HAND
TIME DELAY
TIME DELAY
TIME DELAY
INTERNAL TRANSFER MODE
HANDSHAKE UART
BUS
DRQST
LDSTRB
HBFLG
HIGH DATA BYTE
SGN,DB15 to DB9
VALID
LBFLG
LOW DATA BYTE
DB8 · DB1
VALID
DON'T CARE
①
②
③

Notes:
1. High Impedance State with Resistive Pullup
2. High Impedance State
3. DRQST Input Sensed
4. Output Sequence Greater Than Conversion Cycle

Figure 4: Handshake Output on Command (DRQST Signal Controls Transfer)

Oscillator Control and Operation

OSC CON (Pin 24) configures the internal oscillator as a crystal or RC oscillator. OSC CON = 1 establishes the RC oscillator. R should be 50 kΩ or larger. The internal clock matches the frequency and phase of the BUF OSC (Pin 25) signal. In the crystal oscillator mode (OSC CON = 0) a ÷ 15 is between the buffered oscillator output and the internal clock. The internal oscillator may be over-driven by driving OSC 1 (Pin 23). The OSC CON pin controls whether the internal clock is divided by 15.

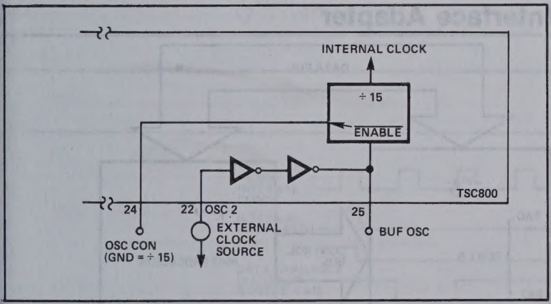
Oscillator Type	OSC CON (Pin 24)	Internal Clock Frequency	Signal Integration Time	Conversion Cycle Time
RC	V_S^+ or open	.45/RC	$16384\left(\frac{RC}{.45}\right)$	$\frac{RC}{.45}$ [65,536]
Crystal	Ground	$f_{XTAL} \div 15$	$16384\left(\frac{15}{f_{XTAL}}\right)$	$\frac{15}{f_{XTAL}}$ [65,536]

f_{XTAL} = Crystal Frequency

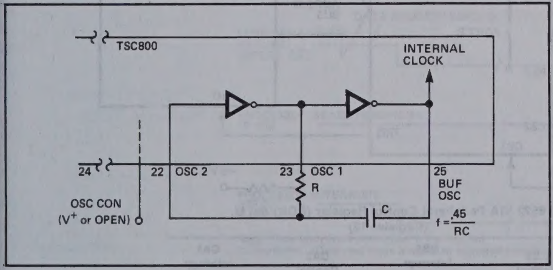
Typical Crystal Operation:

- $f_x = 2.4576$ mHz
- Internal Clock Frequency = 163.8 kHz
- Signal Integration Time = 100 msec
- Conversion Cycle Time = 400 msec (2.5 Conversions/Sec)

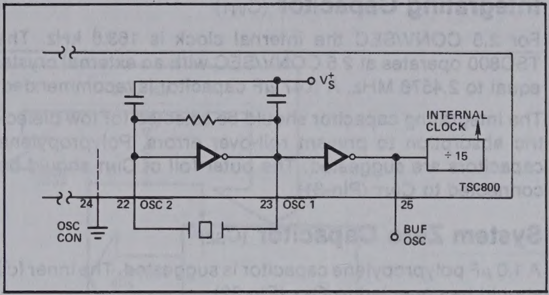
External Oscillator Control



Internal RC Oscillator Configuration



Internal Crystal Oscillator Configuration



Component Value Selection

Integrating Resistor (R_{INT})

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 20 μA drive current with minimal linearity error. R_{INT} is easily calculated for a 20 μA full scale current:

$$R_{INT}\ (\text{M}\ \Omega) = \frac{\text{Full-Scale Input Voltage (V)}}{20}$$

Full-Scale Input Voltage (V_{FS})	R_{INT}
3.2768	160 k Ω
4.0000	200 k Ω

Integrating Capacitor (C_{INT})

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.4 V of V_S^+ or V_S^- without saturating. With ± 5 V power supplies and analog common connected to supply ground a 3.5 V to 4.3 V swing is adequate.

Using the suggested 20 μA full-scale buffer output current the integrating capacitor is easily calculated:

$$C_{INT}\ (\mu\text{F}) = \frac{16.384\left(\frac{1}{f_{CLK}\ (\text{kHz})}\right)\ 20\ \mu\text{A}}{\text{Integrator Output Voltage Swing (V)}}$$

Where: f_{CLK} = Internal Clock Frequency

Component Value Selection (Cont.)

Integrating Capacitor (C_{INT})

For 2.5 CONV/SEC the internal clock is 163.8 kHz. The TSC800 operates at 2.5 CONV/SEC with an external crystal equal to 2.4576 MHz. A 0.47 μF capacitor is recommended.

The integrating capacitor should be selected for low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are suggested. The outer foil of C_{INT} should be connected to C_{INT} (Pin 31).

System Zero Capacitor (C_{SZ})

A 1.0 μF polypropylene capacitor is suggested. The inner foil should be conected to C_{AZ} (Pin 32).

Reference Capacitor (C_{REF})

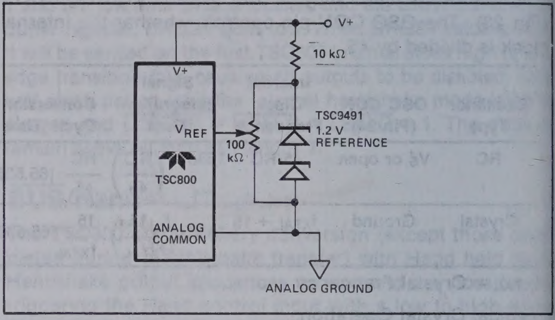
A 1.0 μF capacitor is suggested. Larger values may be used to limit roll-over errors. Low leakage capacitors such as polypropylene or Teflon® should be used.

Reference Voltage

The analog input required to generate the 32,768 full-scale count is $V_{INPUT} = 2\ V_{REF}$. The reference voltage source should be selected for temperature stability. The TSC800 provides 30 ppm resolution. With a 5 ppm/°C reference a 6° change will introduce a 1-bit absolute error. A stable reference must be used where ambient temperature is controlled and accurate absolute measurements are needed.

The reference voltage input must be a positive voltage with respect to analog common. Reference voltage circuits are shown below.

Reference Voltage Circuits

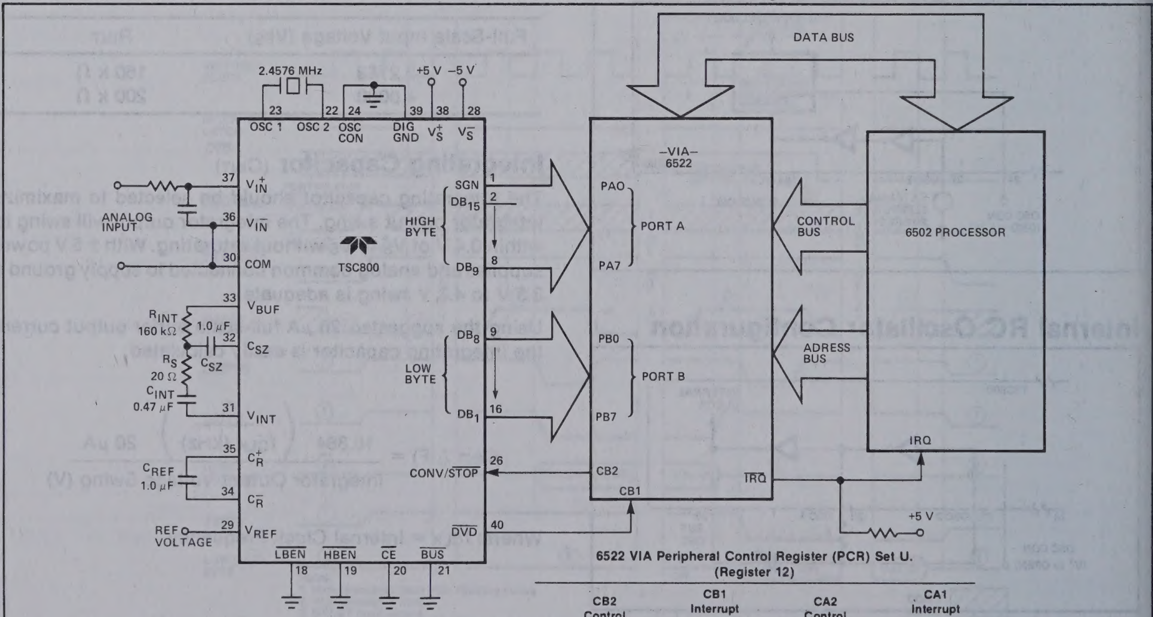

V+
10 kΩ
V+
V_{REF}
100 kΩ
TSC9491
1.2 V
REFERENCE
TSC800
ANALOG
COMMON
ANALOG GROUND

Delay Resistor (R_S)

The R_S, C_{INT} combination compensates for comparator delay time. With a 0.47 μF integrating capacitor a 20 Ω series resistor is suggested.

Applications Information

TSC800 Parallel Interface to 6522 Versatile Interface Adapter


2.4576 MHz
+5 V
−5 V
23
22
24
39
38
28
OSC 1
OSC 2
OSC CON
DIG GND
V_S^+
V_S^-
37
V_{IN}^+
ANALOG INPUT
36
V_{IN}^-
30
COM
33
V_{BUF}
R_{INT} 160 kΩ
1.0 μF
32
C_{SZ}
R_S 20 Ω
C_{SZ}
C_{INT} 0.47 μF
31
V_{INT}
35
C_R^+
C_{REF} 1.0 μF
34
C_R^-
REF VOLTAGE
29
V_{REF}
TSC800
SGN 1
DB_{15} 2
HIGH BYTE
DB_9 8
DB_8 9
LOW BYTE
DB_1 16
CONV/STOP 26
DVD 40
LBEN 18
HBEN 19
CE 20
BUS 21
DATA BUS
—VIA— 6522
PA0
PORT A
PA7
PB0
PORT B
PB7
CB2
CB1
IRQ
CONTROL BUS
ADRESS BUS
6502 PROCESSOR
IRQ
+5 V

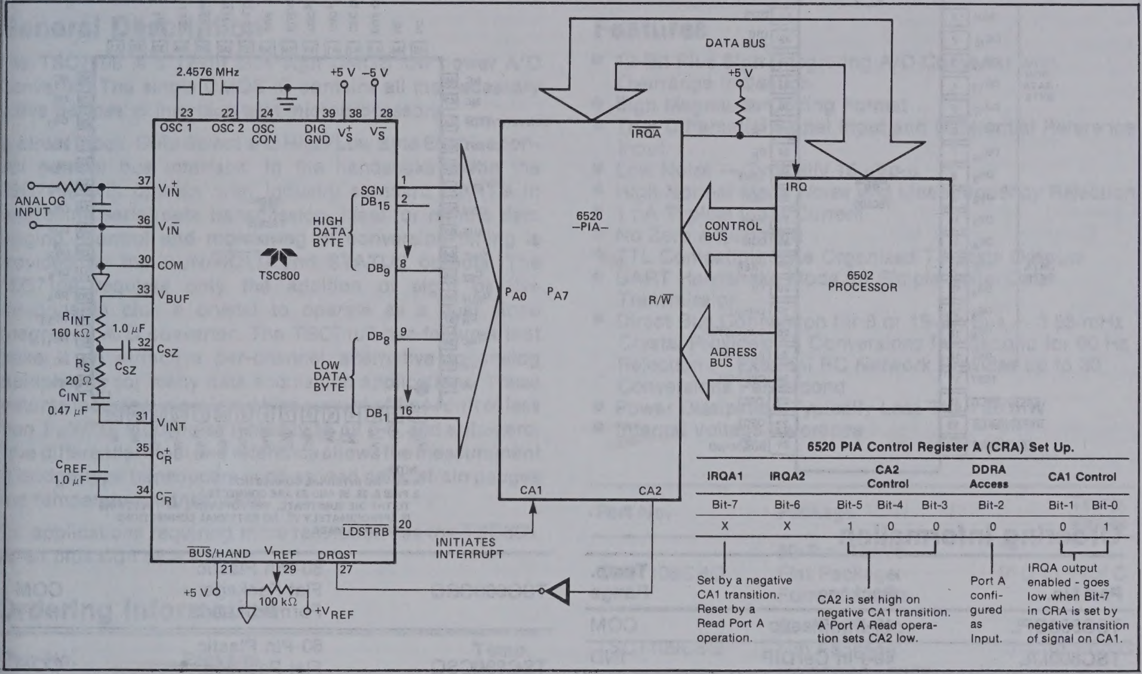
6522 VIA Peripheral Control Register (PCR) Set U.
(Register 12)

CB2 Control			CB1 Interrupt Control	CA2 Control			CA1 Interrupt Control
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1	1	0/1[1]0	—	—	—	—	

[1] May be programmed for convert on command or continuous conversions.

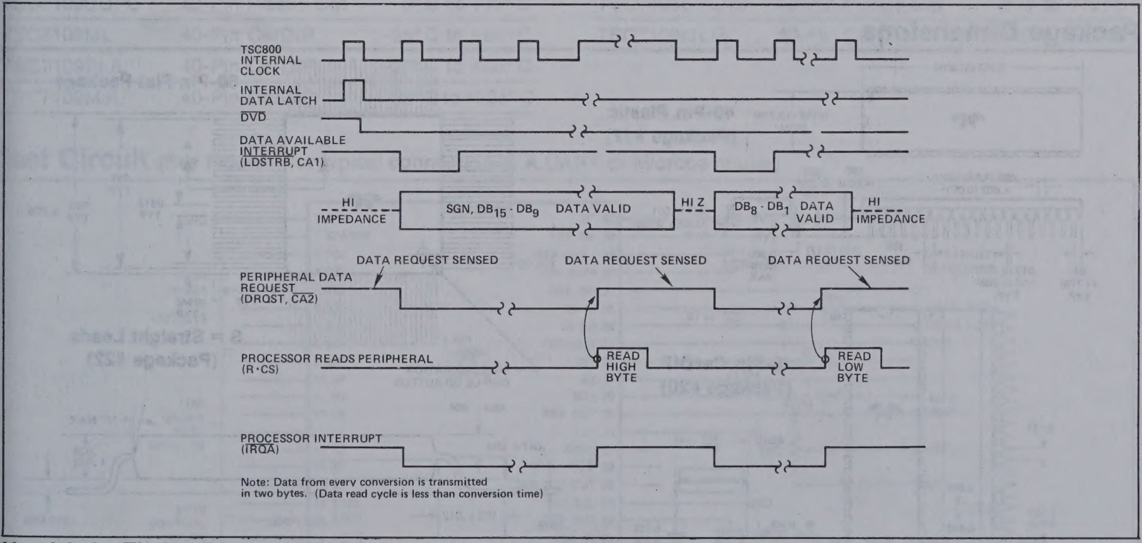
Applications Information (Cont.)

TSC800 Interface to 6520 VIA


2.4576 MHz
+5 V
–5 V
23
22
24
39
38
28
OSC 1
OSC 2
OSC CON
DIG GND
V_S^+
V_S^-
ANALOG INPUT
37
V_{IN}^+
36
V_{IN}^-
30
COM
33
V_{BUF}
R_{INT} 160 kΩ
1.0 µF
32
C_{SZ}
R_S 20 Ω
C_{SZ}
C_{INT} 0.47 µF
31
V_{INT}
35
C_R^+
C_{REF} 1.0 µF
34
C_R^-
TSC800
SGN
DB_{15}
1
2
HIGH DATA BYTE
DB_9
8
DB_8
9
LOW DATA BYTE
DB_1
16
20
LDSTRB
BUS/HAND
V_{REF}
DRQST
21
29
27
+5 V
100 kΩ
$+V_{REF}$
INITIATES INTERRUPT
P_{A0}
P_{A7}
6520 –PIA–
CA1
CA2
DATA BUS
+5 V
$\overline{IRQA}$
IRQ
CONTROL BUS
6502 PROCESSOR
$R/\overline{W}$
ADRESS BUS

6520 PIA Control Register A (CRA) Set Up.

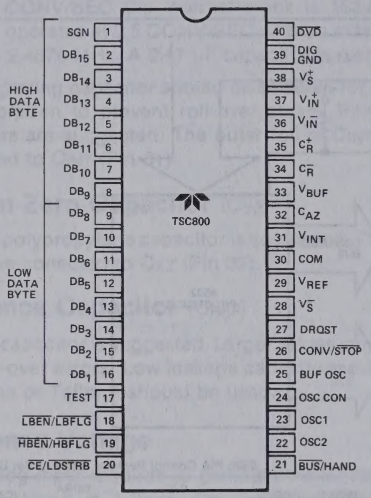
IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
X	X	1	0	0	0	0	1
Set by a negative CA1 transition. Reset by a Read Port A operation.		CA2 is set high on negative CA1 transition. A Port A Read operation sets CA2 low.			Port A configured as Input.	IRQA output enabled - goes low when Bit-7 in CRA is set by negative transition of signal on CA1.	

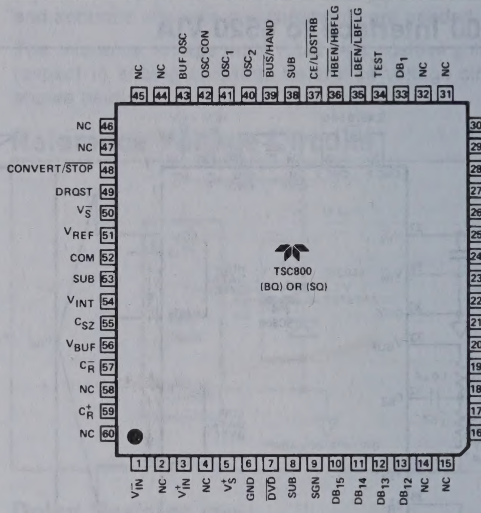

TSC800 INTERNAL CLOCK
INTERNAL DATA LATCH
$\overline{DVD}$
DATA AVAILABLE INTERRUPT ($\overline{LDSTRB}$, CA1)
HI IMPEDANCE
SGN, DB_{15} - DB_9
DATA VALID
HI Z
DB_8 - DB_1
DATA VALID
HI IMPEDANCE
DATA REQUEST SENSED
DATA REQUEST SENSED
DATA REQUEST SENSED
PERIPHERAL DATA REQUEST (DRQST, CA2)
PROCESSOR READS PERIPHERAL (R·CS)
READ HIGH BYTE
READ LOW BYTE
PROCESSOR INTERRUPT ($\overline{IRQA}$)

Note: Data from every conversion is transmitted in two bytes. (Data read cycle is less than conversion time)

Handshake Timing Diagram: TSC800 to 6520 Peripheral Interface Adapter

Pin Configuration and Ordering Information


SGN 1
DB15 2
DB14 3
DB13 4
DB12 5
DB11 6
DB10 7
DB9 8
DB8 9
DB7 10
DB6 11
DB5 12
DB4 13
DB3 14
DB2 15
DB1 16
TEST 17
LBEN/LBFLG 18
HBEN/HBFLG 19
CE/LDSTRB 20
HIGH DATA BYTE
LOW DATA BYTE
TSC800
40 DVD
39 DIG GND
38 V$_S^+$
37 V$_{IN}^+$
36 V$_{IN}^-$
35 C$_R^+$
34 C$_R^-$
33 V$_{BUF}$
32 C$_{AZ}$
31 V$_{INT}$
30 COM
29 V$_{REF}$
28 V$_S^-$
27 DRQST
26 CONV/STOP
25 BUF OSC
24 OSC CON
23 OSC1
22 OSC2
21 BUS/HAND

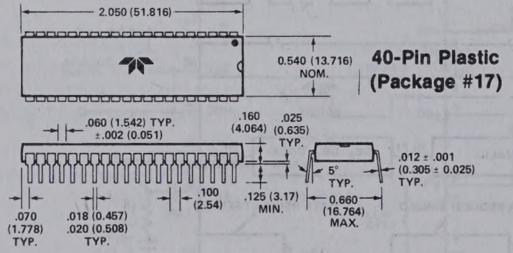

45 NC
44 NC
43 BUF OSC
42 OSC CON
41 OSC1
40 OSC2
39 BUS/HAND
38 SUB
37 CE/LDSTRB
36 HBEN/HBFLG
35 LBEN/LBFLG
34 TEST
33 DB1
32 NC
31 NC
46 NC
47 NC
48 CONVERT/STOP
49 DRQST
50 V$_S^-$
51 V$_{REF}$
52 COM
53 SUB
54 V$_{INT}$
55 C$_{SZ}$
56 V$_{BUF}$
57 C$_R^-$
58 NC
59 C$_R^+$
60 NC
30 NC
29 NC
28 DB2
27 DB3
26 DB4
25 DB5
24 DB6
23 SUB
22 DB7
21 DB8
20 DB9
19 DB10
18 DB11
17 NC
16 NC
1 V$_{IN}^-$
2 NC
3 V$_{IN}^+$
4 NC
5 V$_S^+$
6 GND
7 DVD
8 SUB
9 SGN
10 DB15
11 DB14
12 DB13
13 DB12
14 NC
15 NC
TSC800 (BQ) OR (SQ)

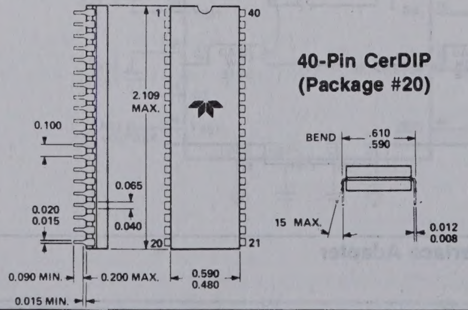
NOTE:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V⁺. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

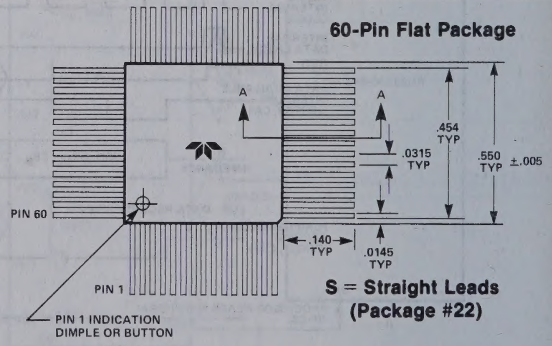
Ordering Information

Part No.	Package	Temp. Range
TSC800CPL	40-Pin Plastic	COM
TSC800IJL	40-Pin CerDIP	IND
TSC800MJL	40-Pin CerDIP	MIL
TSC800CBQ	60-Pin Plastic Flat Package: Formed Leads	COM
TSC800CSQ	60-Pin Plastic Flat Package: Unformed Leads	COM

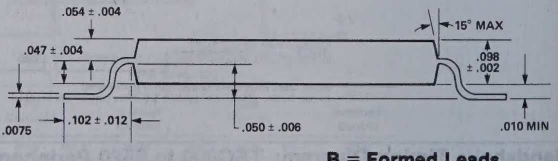
Package Dimensions


40-Pin Plastic (Package #17)
2.050 (51.816)
0.540 (13.716) NOM.
.060 (1.542) TYP. ±.002 (0.051)
.160 (4.064)
.025 (0.635) TYP.
5° TYP.
.012 ± .001 (0.305 ± 0.025) TYP.
.100 (2.54)
.125 (3.17) MIN.
0.660 (16.764) MAX.
.070 (1.778) TYP.
.018 (0.457) .020 (0.508) TYP.


40-Pin CerDIP (Package #20)
1
40
20
21
2.109 MAX.
0.100
0.065
0.020 0.015
0.040
0.090 MIN.
0.200 MAX.
0.590 0.480
0.015 MIN.
BEND
.610 .590
15 MAX.
0.012 0.008


60-Pin Flat Package

S = Straight Leads (Package #22)
A
A
.454 TYP
.0315 TYP
.550 TYP ±.005
PIN 60
.140 TYP
.0145 TYP
PIN 1
PIN 1 INDICATION DIMPLE OR BUTTON


B = Formed Leads (Package #21)
.054 ± .004
.047 ± .004
15° MAX
.098 ± .002
.0075
.102 ± .012
.050 ± .006
.010 MIN

TELEDYNE SEMICONDUCTOR

TSC7109
12-Bit Plus Sign Integrating A/D Converter
• BUS Compatible
• Serial Data Transmission w/UART

General Description

The TSC7109 is a 12-bit plus sign CMOS low power A/D Converter. The single CMOS IC contains all the necessary ctive devices to interface with microprocessors.

n direct mode, Chip Select and High/Low Byte Enables control parallel bus interface. In the handshake mode the TSC7109 will operate with industry standard UART's in controlling serial data transmission, ideal for remote data ogging. Control and monitoring of conversion timing is provided by the RUN/$\overline{\text{HOLD}}$ and STATUS outputs. The TSC7109 requires only the addition of eight passive components plus a crystal to operate as a dual slope ntegrating A/D converter. The TSC7109 has features that nake it an attractive per-channel alternative to analog nultiplexing for many data acquisition applications. These eatures include typical input bias current of 1 pA, drift of less han 1 μV/° C, input noise typically 15 μV p-p, and auto-zero. True differential input and reference allows the measurement of bridge-type transducers such as load cells, strain gauges and temperature transducers.

For applications requiring more resolution see the TSC800, 15-bit plus sign data sheet.

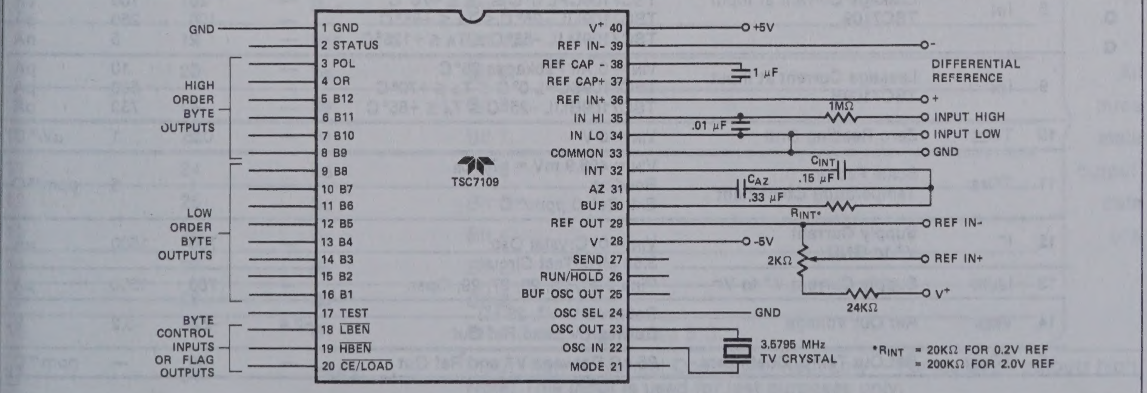
Features

- 12-Bit Plus Sign Integrating A/D Converter with Overrange Indication
- Sign Magnitude Coding Format
- True Differential Signal Input and Differential Reference Input
- Low Noise — Typically 15 μVp-p
- High Normal Mode Noise and Line Frequency Rejection
- 1 pA Typical Input Current
- No Zero Adjustment
- TTL Compatible Byte Organized Tri-State Outputs
- UART Handshake Mode for Simple Serial Data Transmission
- Direct Bus Connection for 8 or 16-Bit Bus — 3.58 mHz Crystal Provides 7.5 Conversions Per Second for 60 Hz Rejection — External RC Network Provides up to 30 Conversions Per Second
- Power Dissipation Typically Less Than 20 mW
- Internal Voltage Reference

Ordering Information

Part No.	Package	Temp. Range
TSC7109CPL	40-Pin Plastic Dip	0° C to + 70° C
TSC7109BCPL	40-Pin Plastic Dip	0° C to +70° C
TSC7109IJL	40-Pin CerDIP	-25° C to +85° C
TSC7109BIJL	40-Pin CerDIP	-25° C to +85° C
TSC7109MJL	40-Pin CerDIP	-55° C to +125° C
TSC7109CBQ	60-Pin Plastic Flat Package: Formed Leads	0° C to +70° C
TSC7109CSQ	60-Pin Plastic Flat Package: Unformed Leads	0° C to +70° C
Devices Available with 160 Hour, +125° C Burn-In		
TSC7109CPL/BI	40-Pin Plastic Dip	0° C to +70° C
TSC7109IJL/BI	40-Pin CerDIP	-25° C to +85° C

Test Circuit (See Figure 1 for typical connection to A UART or Microcomputer)


GND
HIGH ORDER BYTE OUTPUTS
LOW ORDER BYTE OUTPUTS
BYTE CONTROL INPUTS OR FLAG OUTPUTS
1 GND
2 STATUS
3 POL
4 OR
5 B12
6 B11
7 B10
8 B9
9 B8
10 B7
11 B6
12 B5
13 B4
14 B3
15 B2
16 B1
17 TEST
18 LBEN
19 HBEN
20 CE/LOAD
TSC7109
V+ 40
REF IN- 39
REF CAP - 38
REF CAP+ 37
REF IN+ 36
IN HI 35
IN LO 34
COMMON 33
INT 32
AZ 31
BUF 30
REF OUT 29
V- 28
SEND 27
RUN/HOLD 26
BUF OSC OUT 25
OSC SEL 24
OSC OUT 23
OSC IN 22
MODE 21
+5V
-
DIFFERENTIAL REFERENCE
+
1 μF
.01 μF
1MΩ
INPUT HIGH
INPUT LOW
GND
CINT .15 μF
CAZ .33 μF
RINT*
REF IN-
-5V
2KΩ
REF IN+
24KΩ
V+
GND
3.5795 MHz TV CRYSTAL
*RINT = 20KΩ FOR 0.2V REF
= 200KΩ FOR 2.0V REF

© 1983

Absolute Maximum Ratings

Positive Supply Voltage (GND to V^+)	+6.2 V
Negative Supply Voltage (GND to V^-)	-9 V
Analog Input Voltage (LOW or HIGH) (Note 1)	V^+ to V^-
Reference Input Voltage (LOW or HIGH) (Note 1)	V^+ to V^-
Digital Input Voltage (Pins 2-27) (Note 2)	GND -0.3 V
Power Dissipation (Note 3)	
Ceramic Package	1 W @ +85° C
Plastic Package	500 mW @ +70° C
Operating Temperature	
Ceramic Package (M)	$-55°C \leq T_A \leq +125°C$
(I)	$-25°C \leq T_A \leq +85°C$
Plastic Package (C)	$0°C \leq T_A \leq +70°C$
Storage Temperature	$-55°C \leq T_A \leq +125°C$
Lead Temperature (Soldering, 60 sec.)	+300° C

This device contains circuitry to protect the inputs from damage due to high static voltage or electric fields. It is advised that voltages great than those listed under absolute maximum ratings, may cause permanent damage to the devices. Normal precautions should be taken to avoid application of any voltage higher than maximum ratings.

Notes:

1. Input voltages may exceed the supply voltages if the input current is limited to ±100 μA.
2. Connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. Therefore, it is recommended that inputs from sources other than the same power supply should not be applied to the TSC7109 before its power supply is established. In multiple supply systems, the supply to the TSC7109 should be activated first.
3. This limit refers to that of the package and will not occur during the normal operation.
4. *HANDLING PRECAUTIONS:* These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conducting material. Use proper anti-static handling procedures. Do not connect in circuits under "power-on" conditions, as high transients may cause permanent damage.

Electrical Characteristics: All parameters with $V^+ = +5$ V, $V^- = -5$ V, GND = 0 V, $T_A = 25°C$, unless otherwise indicated.

Test circuit as shown on page 1.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7109 MIN	TSC7109 TYP	TSC7109 MAX	UNIT
ANALOG	1		Zero Input Reading	$V_{IN} = 0.0$ V Full-Scale = 409.6 mV	-0000_8	$\pm 0000_8$	$+0000_8$	Octal Reading
	2		Ratiometric Reading	$V_{IN} = V_{REF}$ $V_{REF} = 204.8$ mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
	3	NL	Non-Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 409.6 mV to 4.096 V Over Full Operating Temp. Range.	-1	±.2	+1	Counts
	4		Roll-Over Error (Difference in Reading for Equal Pos. and Neg. Inputs Near Full-Scale)	Full-Scale = 409.6 mV to 4.096 V Over Full Operating Temp. Range.	-1	±.2	+1	Counts
	5	CMRR	Input Common-Mode Rejection Ratio	V_{CM} ±1 V $V_{IN} = 0$ V Full-Scale = 409.6 mV	—	50	—	μV/V
	6	VCMR	Common-Mode Range	Input High, Input Low, Common	$V^- +1.5$	—	$V^+ -1.0$	V
	7		Noise (p-p value not Exceeded 95% of Time)	$V_{IN} = 0$ V Full-Scale = 409.6 mV	—	15	—	μV
	8	I_{IN}	Leakage Current at Input TSC7109	$V_{IN} = 0$ All Packages 25° C TSC7109CPL $0°C \leq T_A \leq +70°C$ TSC7109IJL $-25°C \leq T_A \leq +85°C$ TSC7109MJL $-55°C \leq T_A \leq +125°C$	— — — —	1 20 100 2	10 100 250 5	pA pA pA nA
	9	I_{IN}	Leakage Current at Input TSC7109B	$V_{IN} = 0$ All Packages 25° C TSC7109BCPL $0°C \leq T_A \leq +70°C$ TSC7109BIJL $-25°C \leq T_A \leq +85°C$	— — —	1 — —	10 500 750	pA pA pA
	10	TC_{ZS}	Zero Reading Drift	$V_{IN} = 0$ V	—	0.2	1	μV/° C
	11	TC_{FS}	Scale Factor Temperature Coefficient	$V_{IN} = 408.9$ mV = $>7770_8$ Reading Ext. Ref. 0 ppm/° C	—	1	5	ppm/° C
	12	I^+	Supply Current V^+ to GND	$V_{IN} = 0$, Crystal Osc. 3.58 MHz Test Circuit	—	700	1500	μA
	13	I_{SUPP}	Supply Current V^+ to V^-	Pins 2-21, 25, 26, 27, 29, Open	—	700	1500	μA
	14	V_{REF}	Ref Out Voltage	Referred to V^+, 25 kΩ Between V^+ and Ref Out	-2.4	-2.8	-3.2	V
	15	TC_{REF}	Ref Out Temp. Coefficient	25 kΩ Between V^+ and Ref Out	—	80	—	ppm/° C

lectrical Characteristics: All parameters with $V^+ = +5$ V, $V^- = -5$ V, GND = 0 V, $T_A = 25°$ C, unless otherwise indicated. est circuit as shown on page 1.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7109 MIN	TYP	MAX	UNIT
DIGITAL	16	V_{OH}	Output High Voltage	$I_{OUT} = 100\ \mu A$ Pins 2-16, 18, 19, 20	3.5	4.3	—	V
	17	V_{OL}	Output Low Voltage	$I_{OUT} = 1.6$ mA	—	0.2	0.4	V
	18		Output Leakage Current	Pins 3-16 High Impedance	—	±.01	±1	μA
	19		Control I/0 Pullup Current	Pins 18, 19, 20 $V_{OUT} = V^+$ -3 V MODE Input at GND	—	5	—	μA
	20		Control I/0 Loading	HBEN Pin 19 LBEN Pin 16	—	—	50	pF
	21	V_{IH}	Input High Voltage	Pins 18-21, 26, 27 referred to GND	2.5	—	—	V
	22	V_{IL}	Input Low Voltage	Pins 18-21, 26, 27 Referred to GND	—	—	1	V
	23		Input Pullup Current	Pins 26, 27 $V_{OUT} = V^+$ -3 V	—	5	—	μA
	24		Input Pullup Current	Pins 17, 24 $V_{OUT} = V^+$ -3 V	—	25	—	μA
	25		Input Pulldown Current	Pin 21, V_{OUT} = GND +3 V	—	5	—	μA
	26	O_{OH}	Oscillator Output High	$V_{OUT} = 2.5$ V	—	1	—	mA
		O_{OL}	Current Low	$V_{OUT} = 2.5$ V	—	1.5	—	mA
	27	BO_{OH}	Buffered Oscillator High	$V_{OUT} = 2.5$ V	—	2	—	mA
		BO_{OL}	Output Current Low	$V_{OUT} = 2.5$ V	—	5	—	mA
	28	t_W	MODE Input Pulse Width		50	—	—	ns

in Description

40-Pin DIP Pin Number Normal/(Reverse)	60-Pin Flat Package Pin Number	Name	Description	
1	9	GND	Digital Ground, 0 V, Ground Return for all digital logic.	
2	10	STATUS	Output High during integrate and deintegrate until data is latched. Output Low when analog section is in Auto-Zero configuration.	
3	11	POL	Polarity — High for Positive Input.	All three state output data bits
4	12	OR	Overrange — High if Overranged.	
5	13	B_{12}	Bit 12 (Most Significant Bit).	
6	18	B_{11}	Bit 11.	
7	19	B_{10}	Bit 10.	
8	20	B_9	Bit 9.	
9	21	B_8	Bit 8.	
10	22	B_7	Bit 7.	
11	24	B_6	Bit 6	
12	25	B_5	Bit 5.	
13	26	B_4	Bit 4.	
14	27	B_3	Bit 3.	
15	28	B_2	Bit 2.	
16	33	B_1	Bit 1 (Least Significant Bit).	
17	34	TEST	Input High — Normal Operation. Input Low — Forces all bit outputs high. Note: This input is used for test purposes only.	

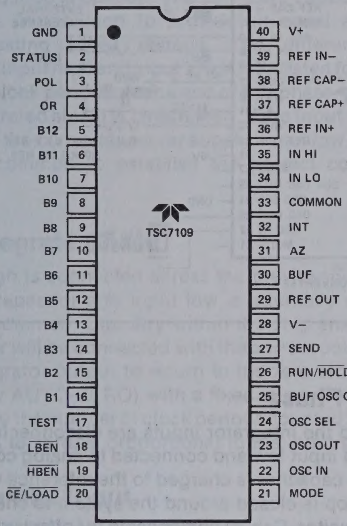
Pin Description (Cont.)

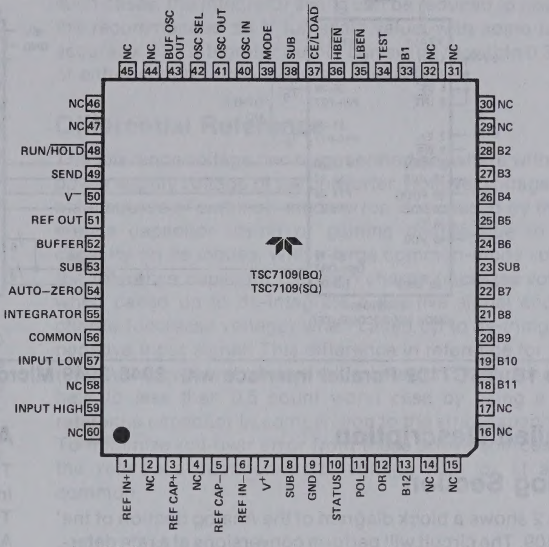
40-Pin DIP Pin Number Normal/(Reverse)	60-Pin Flat Package Pin Number	Name	Description
18	35	$\overline{\text{LBEN}}$	Low Byte Enable — With MODE (Pin 21) low, and $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20) low, taking this pin low activates low order byte outputs B1-B8. With MODE (Pin 21) high, this pin serves as low byte flag output used in handshake mode. See Figures 7, 8, 9.
19	36	$\overline{\text{HBEN}}$	High Byte Enable — With MODE (Pin 21) low, and $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20) low, taking this pin low activates high order byte outputs B9-B12, POL, OR. With MODE (Pin 21) high, this pin serves as high byte flag output used in handshake mode. See Figures 7, 8. 9.
20	37	$\overline{\text{CE}}/\overline{\text{LOAD}}$	Chip Enable Load — With MODE (Pin 21)low, $\overline{\text{CE}}/\overline{\text{LOAD}}$ serves as a master output enable. When high, B1-B12, POL, OR outputs are disabled. When MODE (Pin 21) low, a load strobe used in handshake mode. See Figures 7, 8, 9.
21	39	MODE	Input Low — Direct output mode where $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High — Causes immediate entry into handshake mode and output of data as in Figure 9. Input High — Enables $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversions completion.
22	40	OSC IN	Oscillator Input
23	41	OSC OUT	Oscillator Output
24	42	OSC SEL	Oscillator Select — Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator — clock will be same phase and duty cycle as BUF OSC OUT. Input low configures OSC IN, OSC OUT for crystal oscillator — clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	43	BUF OSC OUT	Buffered Oscillator Output.
26	48	RUN/$\overline{\text{HOLD}}$	Input High — Conversions continuously performed every 8192 clock pulses. Input Low — Conversion in progress completed, converter will stop in Auto-Zero seven counts before integrate.
27	49	SEND	Input — Used in handshake mode to indicate ability of an external device to accept data. Connect to V^+ if not used.
28	50	V^-	Analog Negative Supply — Nominally -5 V with respect to GND (Pin 1).
29	51	REF OUT	Reference Voltage Output — Nominally 2.8 V down from V^+ (Pin 40).
30	52	BUFFER	Buffer Amplifier Output.
31	54	AUTO-ZERO	Auto-Zero Node — Inside foil of C_{AZ}.
32	55	INTEGRATOR	Integrator Output — Outside foil of C_{INT}.
33	56	COMMON	Analog Common — System is Auto-Zeroed to COMMON.
34	57	INPUT LOW	Differential Input Low Side.
35	59	INPUT HIGH	Differential Input High Side.
36	1	REF IN +	Differential Reference Input Positive.
37	3	REF CAP +	Reference Capacitor Positive.
38	5	REF CAP -	Reference Capacitor Negative.
39	6	REF IN -	Differential Reference Input Negative.
40	7	V^+	Positive Supply Voltage — Nominally +5 V with respect to GND (Pin 1).

NOTE: All digital levels are positive true.

12-Bit Plus Sign Integrating A/D Converter
- **BUS Compatible**
- **Serial Data Transmission w/UART**

Pin Configuration


GND 1
STATUS 2
POL 3
OR 4
B12 5
B11 6
B10 7
B9 8
B8 9
B7 10
B6 11
B5 12
B4 13
B3 14
B2 15
B1 16
TEST 17
LBEN 18
HBEN 19
CE/LOAD 20
40 V+
39 REF IN−
38 REF CAP−
37 REF CAP+
36 REF IN+
35 IN HI
34 IN LO
33 COMMON
32 INT
31 AZ
30 BUF
29 REF OUT
28 V−
27 SEND
26 RUN/HOLD
25 BUF OSC OUT
24 OSC SEL
23 OSC OUT
22 OSC IN
21 MODE
TSC7109


45 NC
44 NC
43 BUF OSC OUT
42 OSC SEL
41 OSC OUT
40 OSC IN
39 MODE
38 SUB
37 CE/LOAD
36 HBEN
35 LBEN
34 TEST
33 B1
32 NC
31 NC
NC 46
NC 47
RUN/HOLD 48
SEND 49
V− 50
REF OUT 51
BUFFER 52
SUB 53
AUTO−ZERO 54
INTEGRATOR 55
COMMON 56
INPUT LOW 57
NC 58
INPUT HIGH 59
NC 60
30 NC
29 NC
28 B2
27 B3
26 B4
25 B5
24 B6
23 SUB
22 B7
21 B8
20 B9
19 B10
18 B11
17 NC
16 NC
1 REF IN+
2 NC
3 REF CAP+
4 NC
5 REF CAP−
6 REF IN−
7 V+
8 SUB
9 GND
10 STATUS
11 POL
12 OR
13 B12
14 NC
15 NC
TSC7109(BQ)
TSC7109(SQ)

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

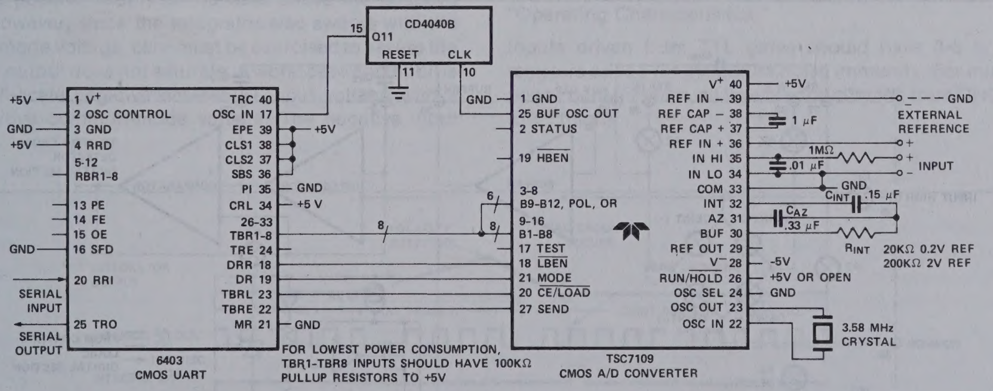

CD4040B
15 Q11
RESET 11
CLK 10
+5V 1 V+
2 OSC CONTROL
GND 3 GND
+5V 4 RRD
5-12 RBR1-8
13 PE
14 FE
15 OE
GND 16 SFD
20 RRI
SERIAL INPUT
25 TRO
SERIAL OUTPUT
TRC 40
OSC IN 17
EPE 39
CLS1 38
CLS2 37
SBS 36
PI 35
CRL 34
26-33 TBR1-8
TRE 24
DRR 18
DR 19
TBRL 23
TBRE 22
MR 21
+5V
GND
+5 V
GND
8
6
8
6403
CMOS UART
FOR LOWEST POWER CONSUMPTION, TBR1-TBR8 INPUTS SHOULD HAVE 100KΩ PULLUP RESISTORS TO +5V
GND
1 GND
25 BUF OSC OUT
2 STATUS
19 HBEN
3-8 B9-B12, POL, OR
9-16 B1-B8
17 TEST
18 LBEN
21 MODE
20 CE/LOAD
27 SEND
V+ 40
REF IN − 39
REF CAP − 38
REF CAP + 37
REF IN + 36
IN HI 35
IN LO 34
COM 33
INT 32
AZ 31
BUF 30
REF OUT 29
V− 28
RUN/HOLD 26
OSC SEL 24
OSC OUT 23
OSC IN 22
TSC7109
CMOS A/D CONVERTER
+5V
1 μF
GND
EXTERNAL REFERENCE
1MΩ
.01 μF
INPUT
GND
CINT .15 μF
CAZ .33 μF
RINT
20KΩ 0.2V REF
200KΩ 2V REF
−5V
+5V OR OPEN
GND
3.58 MHz CRYSTAL

Figure 1A: TSC7109 UART Interface. Send Any Word to UART to Transmit Latest Result.

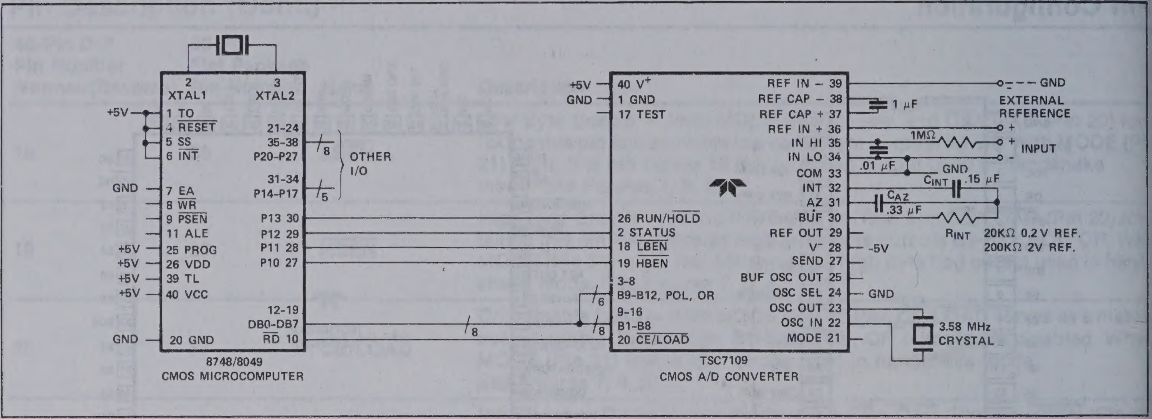

2 XTAL1
3 XTAL2
+5V
1 TO
4 RESET
5 SS
6 INT
21-24
35-38
P20-P27
8
OTHER I/O
31-34
P14-P17
5
GND
7 EA
8 WR
9 PSEN
11 ALE
25 PROG
26 VDD
39 TL
40 VCC
P13 30
P12 29
P11 28
P10 27
12-19
DB0-DB7
RD 10
20 GND
8748/8049
CMOS MICROCOMPUTER
+5V
GND
40 V+
1 GND
17 TEST
26 RUN/HOLD
2 STATUS
18 LBEN
19 HBEN
3-8
B9-B12, POL, OR
9-16
B1-B8
20 CE/LOAD
6
8
REF IN – 39
REF CAP – 38
REF CAP + 37
REF IN + 36
IN HI 35
IN LO 34
COM 33
INT 32
AZ 31
BUF 30
REF OUT 29
V⁻ 28
SEND 27
BUF OSC OUT 25
OSC SEL 24
OSC OUT 23
OSC IN 22
MODE 21
TSC7109
CMOS A/D CONVERTER
1 μF
.01 μF
1MΩ
GND
EXTERNAL REFERENCE
+
–
INPUT
CINT .15 μF
CAZ .33 μF
RINT 20KΩ 0.2 V REF. 200KΩ 2V REF.
-5V
GND
3.58 MHz CRYSTAL

Figure 1B: TSC7109 Parallel Interface with 8048/8049 Microcomputer

Detailed Description

Analog Section

Figure 2 shows a block diagram of the Analog Section of the TSC7109. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle), when the RUN/$\overline{\text{HOLD}}$ input is left open or connected to V$^+$. Each measurement cycle is divided into three phases as shown in Figure 3. They are: (1) Auto-Zero (AZ), (2) Signal Integrate (INT), (3) Reference Deintegrate (DE).

Auto-Zero Phase

The buffer and the integrator inputs are disconnected from input high and input low and connected to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltage in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

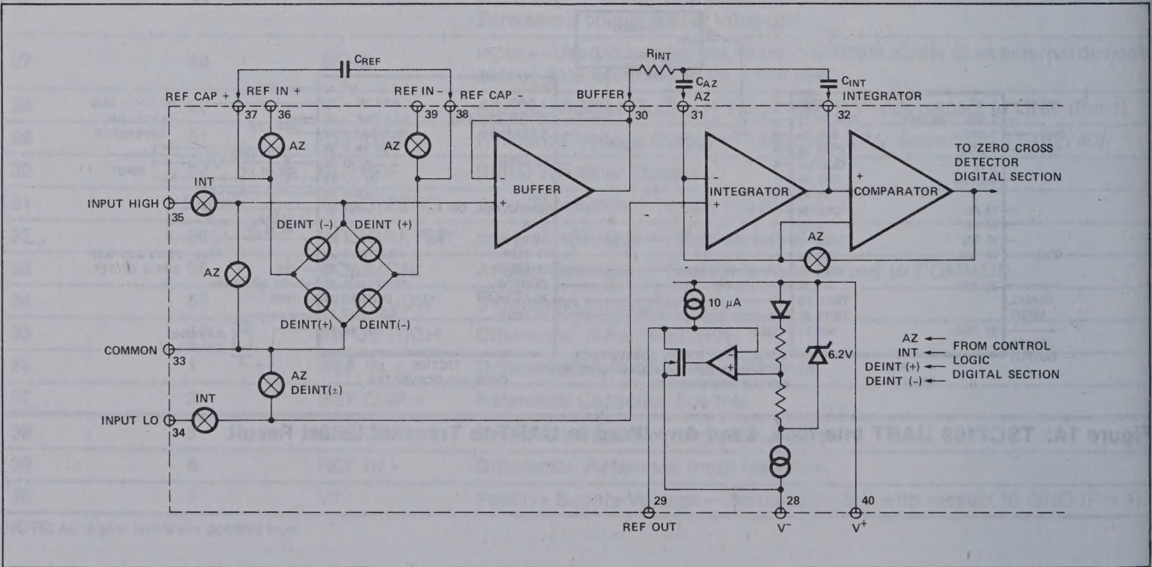

CREF
RINT
CAZ
CINT
REF CAP +
REF IN +
REF IN –
REF CAP –
BUFFER
AZ
INTEGRATOR
37
36
39
38
30
31
32
AZ
AZ
INT
INPUT HIGH
35
BUFFER
INTEGRATOR
COMPARATOR
TO ZERO CROSS DETECTOR DIGITAL SECTION
DEINT (–)
DEINT (+)
AZ
AZ
10 μA
DEINT(+)
DEINT(–)
COMMON
33
AZ DEINT(±)
6.2V
AZ
INT
DEINT (+)
DEINT (–)
FROM CONTROL LOGIC DIGITAL SECTION
INT
INPUT LO
34
29
28
40
REF OUT
V⁻
V⁺

Figure 2: Analog Section

ignal Integrate Phase

he buffer and integrator inputs are removed from OMMON and connected to input high and input low. The uto-zero loop is opened. The auto-zero capacitor is placed series in the loop to provide an equal and opposite ompensating offset voltage. The differential voltage etween input high and input low is integrated for a fixed time f 2048 clock periods. At the end of this phase, the polarity of e integrated signal is determined. If the input signal has no eturn to the converter power supply, input low can be tied to nalog common to establish the correct common-mode oltage.

e-Integrate Phase

put high is connected across the previously charged reference capacitor and input low is internally connected to nalog common. Circuitry within the chip ensures that the apacitor will be connected with the correct polarity to cause e integrator output to return to the zero crossing (established by AUTO-ZERO) with a fixed slope. The time, represented by the number of clock periods counted for the output return to zero, is proportional to the input signal.

ifferential Input

he TSC7109 has been optimized for operation with analog-ommon near digital ground. With +5 V and -5 V power suplies, a full ±4 V full-scale integrator swing maximizes the nalog section's performance.

typical CMRR of 86 dB is achieved for input differential volages anywhere within the common-mode range of 0.5 volts elow the positive supply to 1.0 volts above the negative upply. However, since the integrator also swings with the ommon-mode voltage, care must be exercised to assure the ntegrator output does not saturate. A worst case condition is ear a full-scale negative differential input voltage with a arge positive common-mode voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. In such cases, the integrator swing can be reduced to less than the recommended ±4 V full-scale value, with some loss of accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity.

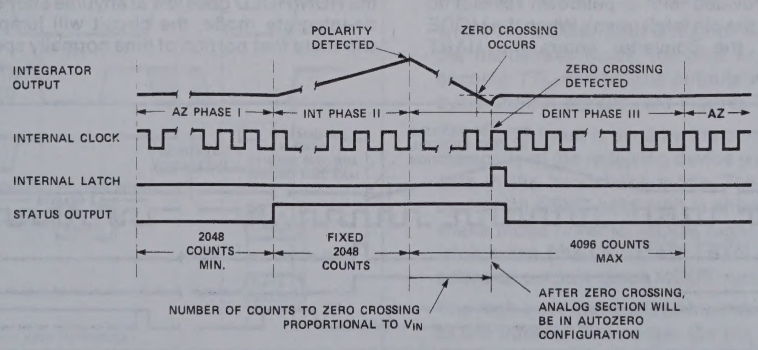
Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. Rollover voltage is the main source of common-mode error. It is caused by the reference capacitor losing or gaining charge due to stray capacity on its modes. With a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal and lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (-) input voltage will cause a roll-over error. This error can be held to less than 0.5 count worst case by using a large reference capacitor in comparision to the stray capacitance. To minimize roll-over error from these above sources keep the reference common-mode voltage near or at analog common.

Digital Section

The digital section is shown in block diagram Figure 4 and includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, UART handshake logic, polarity, overrange and control logic. Logic levels are referred to as "low"or "high". The actual logic levels are defined in Table 1 "Operating Characteristics."

Inputs driven from TTL gates should have 3-5 k pullup resistors added for maximum noise immunity. For minimum power consumption, all inputs should swing from GND (low) to V$^+$ (high).



igure 3: Conversion Timing (RUN/$\overline{\text{HOLD}}$ Pin High)

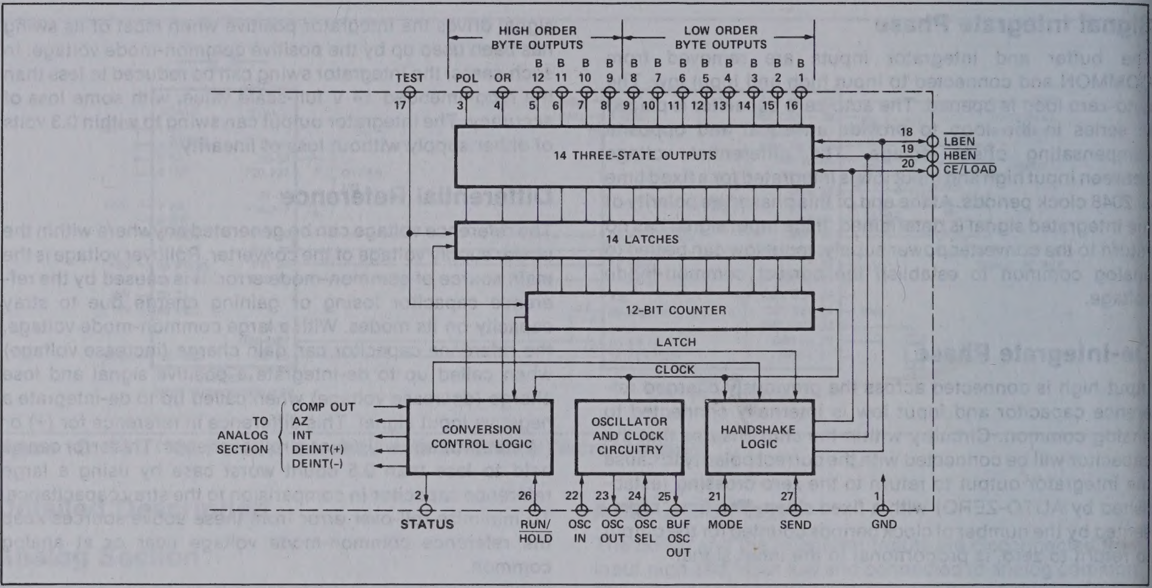

HIGH ORDER BYTE OUTPUTS
LOW ORDER BYTE OUTPUTS
TEST
POL
OR
B 12
B 11
B 10
B 9
B 8
B 7
B 6
B 5
B 4
B 3
B 2
B 1
17
3
4
5
6
7
8
9
10
11
12
13
14
15
16
14 THREE-STATE OUTPUTS
18
19
20
LBEN
HBEN
CE/LOAD
14 LATCHES
12-BIT COUNTER
LATCH
CLOCK
TO ANALOG SECTION
COMP OUT
AZ
INT
DEINT(+)
DEINT(-)
CONVERSION CONTROL LOGIC
OSCILLATOR AND CLOCK CIRCUITRY
HANDSHAKE LOGIC
2
26
22
23
24
25
21
27
1
STATUS
RUN/HOLD
OSC IN
OSC OUT
OSC SEL
BUF OSC OUT
MODE
SEND
GND

Figure 4: Digital Section

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3. The signal may be used as a "data valid" flag to drive interrupts, or for monitoring the status of the converter. (Data will not change while STATUS is low).

MODE Input

The output mode of the converter is controlled by the MODE input. The converter is in its "Direct" output mode, when the MODE pin is low or left open. The output data is directly accessible under the control of the chip and byte enable inputs (this input is provided with a pulldown resistor to ensure a low level when the pin is left open). When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is kept high, the converter will output data in the handshake mode at the end of every conversion cycle with MODE = 0 (Direct BUS Transfer) the send input should be tied to V^+. (See Handshake Mode Section).

RUN/$\overline{\text{HOLD}}$ Input

With RUN/$\overline{\text{HOLD}}$ high or open, the circuit operates normally as a dual slope A/D as shown in Figure 3. Conversion cycles operate continuously with the output latches updated after zero crossing in the de-integrate mode. An internal pullup resistor is provided to insure a high level with an open input.

The RUN/$\overline{\text{HOLD}}$ may be used to shorten conversion time. If the RUN/$\overline{\text{HOLD}}$ goes low at anytime after zero crossing in the de-integrate mode, the circuit will jump to auto-zero and eliminate that portion of time normally spent in de-integrate.

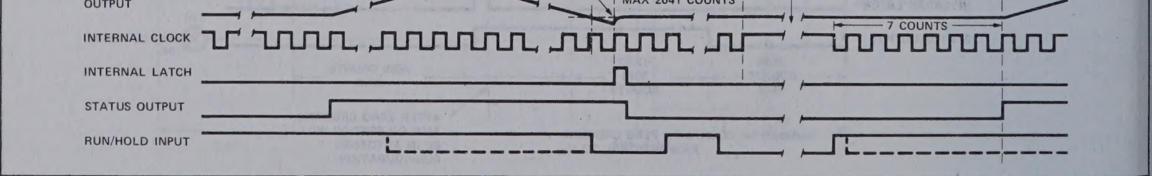

DEINT TERMINATED AT ZERO CROSSING DETECTION
AUTOZERO PHASE I MIN 1790 COUNTS MAX 2041 COUNTS
STATIC IN HOLD STATE
INT PHASE II
7 COUNTS
INTEGRATOR OUTPUT
INTERNAL CLOCK
INTERNAL LATCH
STATUS OUTPUT
RUN/HOLD INPUT

Figure 5: TSC7109 RUN/$\overline{\text{HOLD}}$ Operation

f RUN/$\overline{\text{HOLD}}$ stays or goes low the conversion will complete with minimum time in de-integrate. It will stay in auto-zero for he minimum time and wait in auto-zero for a high in the RUN/$\overline{\text{HOLD}}$ input. As shown in Figure 5, the STATUS output will go high seven clock periods after RUN/$\overline{\text{HOLD}}$ is changed o high, and the converter will begin the integrate phase of he next conversion.

The RUN/$\overline{\text{HOLD}}$ input allows controlled conversion nterface. The converter may be held at idle in auto-zero with RUN/HOLD low. The conversion is started when RUN/$\overline{\text{HOLD}}$ goes high and the new data is valid when the STATUS output goes low (or is transferred to the UART — see Handshake Mode.) RUN/$\overline{\text{HOLD}}$ may now go low, terminating de-ntegrate and ensuring a minimum auto-zero time before stopping to wait for the next conversion. Conversion time can be minimized by ensuring RUN/$\overline{\text{HOLD}}$ goes low during de-ntegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/$\overline{\text{HOLD}}$ input can be provided by connecting it to the Buffered Oscillator output. In this mode, the input value measured determines the conversion time.

Direct Mode

The data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and overrange high order byte) are accessible under control of the byte and chip enable terminals as inputs with the MODE pin at a low level. These three nputs are all active low. Internal pullup resistors are provided for an inactive high level when left open. When the chip enable input is low, a byte enable input low will allow the outputs of that byte to become active. A variety of parallel data accessing techniques may be used, as shown in the section entitled "Interfacing." (See Figure 6 and Table 3)

The access of data should be synchronized with the conversion cycle by monitoring the STATUS output. This will prevent accessing the data while it is being updated and eliminate the acquisition of erroneous data.

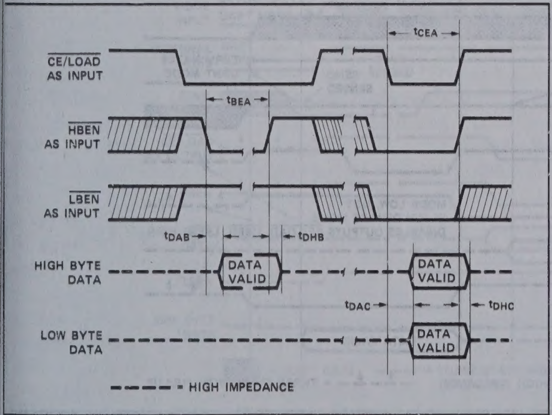


Figure 6: TSC7109 Direct Mode Output Timing

Symbol	Description	Min.	Typ.	Max.	Units
t_{BEA}	Byte Enable Width	350	220		ns
t_{DAB}	Data Access Time from Byte Enable		150	350	ns
t_{DHB}	Data Hold Time from Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	400	260		ns
t_{DAC}	Data Access Time from Chip Enable		260	400	ns
t_{DHC}	Data Hold Time from Chip Enable		240	400	ns

Table 3. TSC7109 Direct Mode Timing Requirements

Handshake Mode

An alternative means of interfacing the TSC7109 to digital systems is provided when the handshake output mode of the TSC7109 becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode allows a direct interface between the TSC7109 and industry-standard UART's with no external logic required. The TSC7109 provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form when triggered into the handshake mode. The cost of designing remote data acquisition stations is reduced using serial data transmission to minimize the number of lines to the central controlling processor.

The MODE pin controls the handshake mode. When the MODE terminal is held high, the TSC7109 will enter the handshake mode after new data has been stored in the output latches at the end of every conversion performed (see Figures 7 and 8). Entry into the handshake mode may be triggered on demand by the MODE terminal. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. The MODE input is ignored in the handshake mode, and until the converter completes the output cycle and clears the handshake mode data updating will be inhibited (see Figure 9).

When the MODE input is high or when the converter enters the handshake mode, the chip and byte enable terminals become TTL-compatible outputs which provide the output cycle control signals (see Figures 7,8 and 9).

The SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data in the handshake mode. The sequence of the output cycle with SEND held high is shown in Figure 7. The handshake mode (internal MODE high) is entered after the data latch pulse (the $\overline{\text{CE/LOAD}}$, $\overline{\text{LBEN}}$ and $\overline{\text{HBEN}}$ terminals are active as outputs since MODE remains high).

The high level at the SEND input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled and the $\overline{\text{CE/LOAD}}$ and the $\overline{\text{HBEN}}$

outputs assume a low level. The CE/LOAD output remains low for one full internal clock period only; the data outputs remain active for 1-1/2 internal clock periods; and the high byte enable remains low for two clock periods. The CE/LOAD output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using CE/LOAD and LBEN while the low order byte outputs (bits 1 through 8) are activated. When both bytes are sent the handshake mode is terminated. The typical UART interfacing timing is shown in Figure 8. The SEND input is used to delay portions of the sequence, or handshake to ensure correct data transfer. This timing diagram shows an industry-standard HD6402 or CDP1854 CMOS UART to interfacing serial data channels. The SEND input to the TSC7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the CE/LOAD terminal of the TSC7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The eight transmitter Buffer Register inputs accept the parallel data outputs. With the UART Transmitter Buffer Register empty, the SEND input will be high when the handshake mode is entered after new data is stored. The high order byte outputs become active and the CE/LOAD and HBEN terminals will go low after SEND is sensed. When CE/LOAD goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will go low, which halts the output cycle with the HBEN output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. The high order byte outputs are disabled on the next TSC7109 internal clock high to low edge, and one-half internal clock later, the HBEN output returns high. The CE/LOAD and LBEN outputs go low at the same time as the low order byte outputs become active. When the CE/LOAD returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. The next TSC7109 internal clock high to low edge will sense when TBRE returns to a high, disabling the data outputs. One-half internal clock later, the handshake mode is cleared, and the CE/LOAD, HBEN and LBEN terminals return high and stay active, if MODE still remains high.

Handshake output sequences may be performed on demand by triggering the converter into handshake mode with a low to high edge on the MODE input. A handshake output sequence triggered is shown in Figure 9. The SEND input is low when the converter enters handshake mode. The whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte.

This diagram also shows that the output sequence takes longer than a conversion cycle. New data will not be latched when the handshake mode is still in progress and is therefore lost.

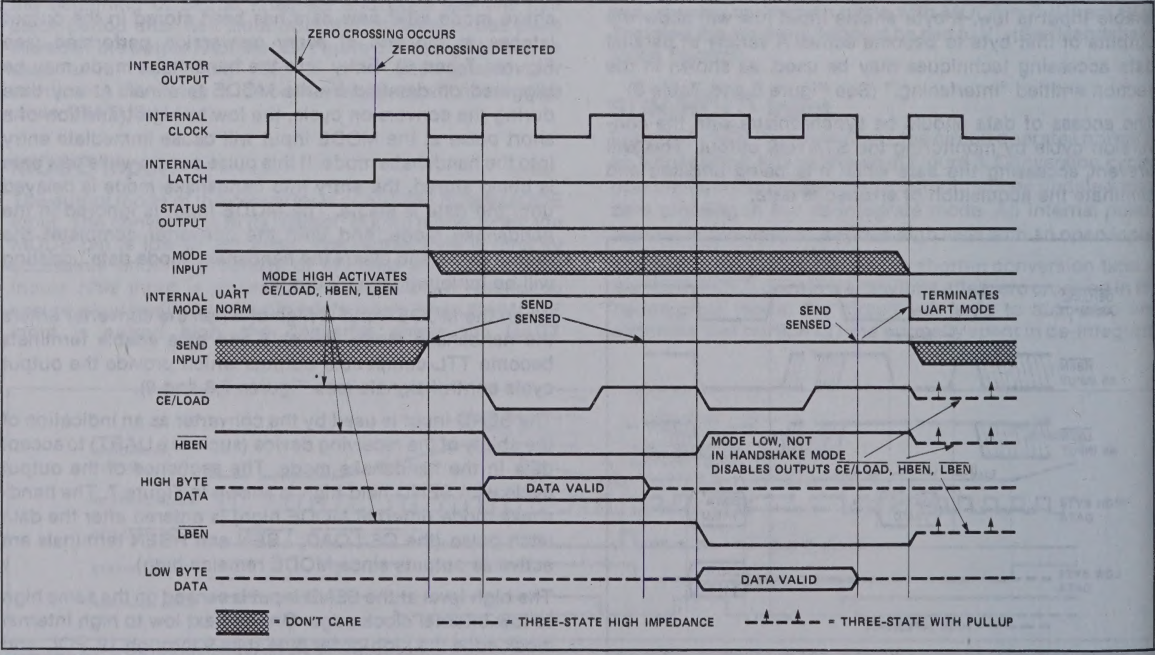
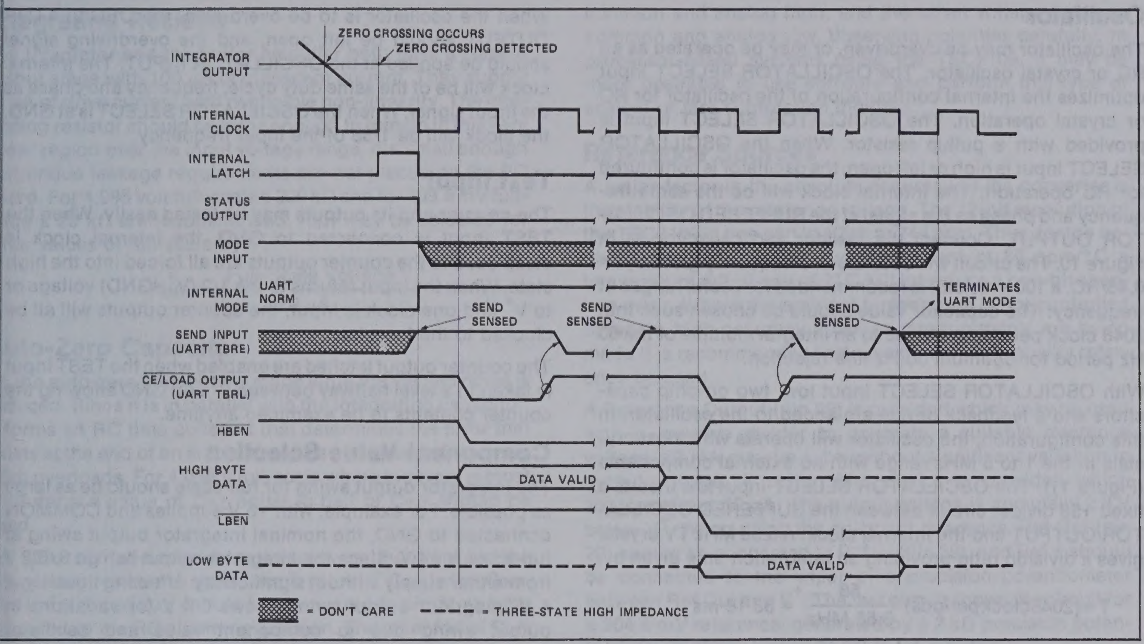

ZERO CROSSING OCCURS
ZERO CROSSING DETECTED
INTEGRATOR OUTPUT
INTERNAL CLOCK
INTERNAL LATCH
STATUS OUTPUT
MODE INPUT
MODE HIGH ACTIVATES CE/LOAD, HBEN, LBEN
INTERNAL MODE
UART
NORM
SEND SENSED
SEND SENSED
TERMINATES UART MODE
SEND INPUT
CE/LOAD
HBEN
MODE LOW, NOT IN HANDSHAKE MODE DISABLES OUTPUTS CE/LOAD, HBEN, LBEN
HIGH BYTE DATA
DATA VALID
LBEN
LOW BYTE DATA
DATA VALID
▨ = DON'T CARE
= THREE-STATE HIGH IMPEDANCE
= THREE-STATE WITH PULLUP

Figure 7: TSC7109 Handshake with Send Input Held Positive


ZERO CROSSING OCCURS
ZERO CROSSING DETECTED
INTEGRATOR OUTPUT
INTERNAL CLOCK
INTERNAL LATCH
STATUS OUTPUT
MODE INPUT
INTERNAL MODE
UART
NORM
SEND SENSED
SEND SENSED
SEND SENSED
TERMINATES UART MODE
SEND INPUT (UART TBRE)
CE/LOAD OUTPUT (UART TBRL)
HBEN
HIGH BYTE DATA
DATA VALID
LBEN
LOW BYTE DATA
DATA VALID
▨ = DON'T CARE
– – – – = THREE-STATE HIGH IMPEDANCE

igure 8: TSC7109 Handshake — Typical UART Interface Timing

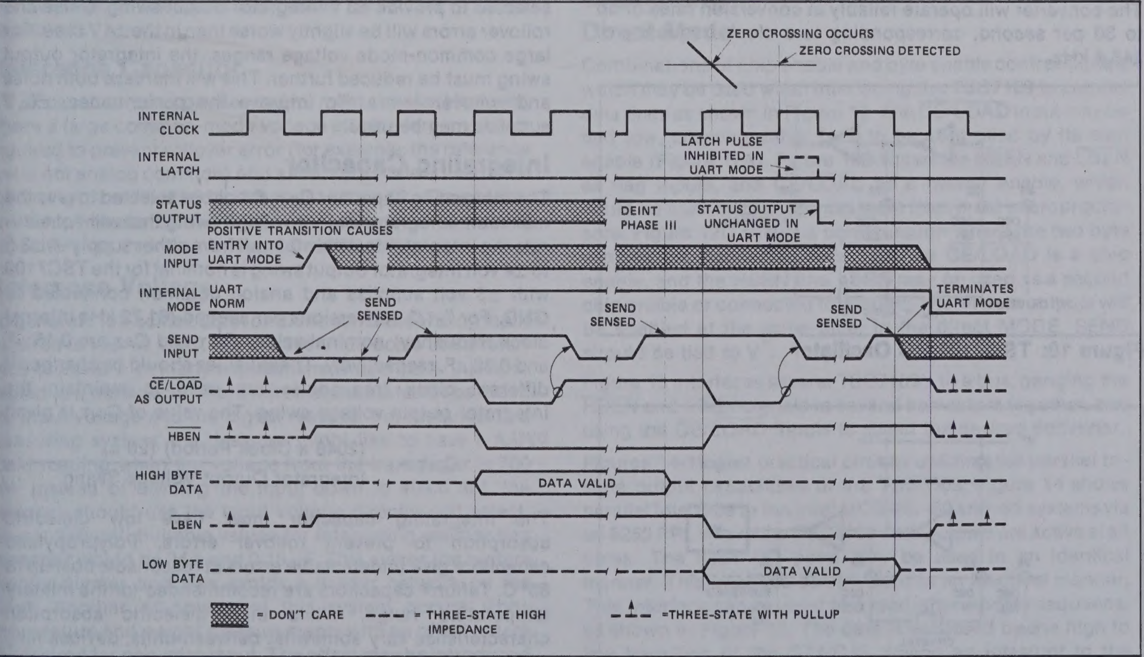

ZERO CROSSING OCCURS
ZERO CROSSING DETECTED
INTERNAL CLOCK
INTERNAL LATCH
LATCH PULSE INHIBITED IN UART MODE
STATUS OUTPUT
DEINT PHASE III
STATUS OUTPUT UNCHANGED IN UART MODE
POSITIVE TRANSITION CAUSES ENTRY INTO UART MODE
MODE INPUT
INTERNAL MODE
UART
NORM
SEND SENSED
SEND SENSED
SEND SENSED
TERMINATES UART MODE
SEND INPUT
CE/LOAD AS OUTPUT
HBEN
HIGH BYTE DATA
DATA VALID
LBEN
LOW BYTE DATA
DATA VALID
▨ = DON'T CARE
– – – = THREE-STATE HIGH IMPEDANCE
=THREE-STATE WITH PULLUP

Figure 9: TSC7109 Handshake Triggered by Mode Input

Oscillator

The oscillator may be overdriven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input optimizes the internal configuration of the oscillator for RC or crystal operation. The OSCILLATOR SELECT input is provided with a pullup resistor. When the OSCILLATOR SELECT input is high or left open, the oscillator is configured for RC operation. The internal clock will be the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. Connect the resistor and capacitor as in Figure 10. The circuit will oscillate at a frequency given by $f = 0.45/RC$. a 100 k resistor is recommended for useful ranges of frequency. The capacitor value should be chosen such that 2048 clock periods are close to an integral multiple of the 60 Hz period for optimum 60 Hz line rejection.

With OSCILLATOR SELECT input low, two on-chip capacitors and a feedback device are added to the oscillator. In this configuration, the oscillator will operate with most crystals in the 1 to 5 MHz range with no external components (Figure 11). The OSCILLATOR SELECT input low inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. A 3.58 MHz TV crystal gives a division ratio providing an integration time given by:

$$T = (2048 \text{ clock periods}) \frac{58}{3.58 \text{ MHz}} = 33.18 \text{ ms}$$

The error is less than one percent from two 60 Hz periods or 33.33 ms which will give better than 40 dB, 60 Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, corresponding to a clock frequency of 245.8 kHz.

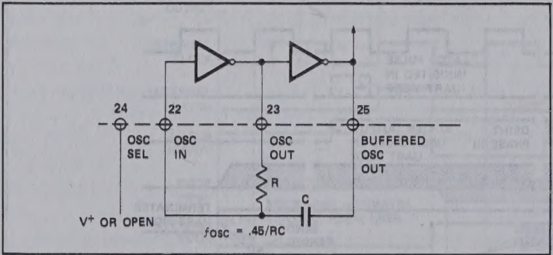


Figure 10: TSC7109 RC Oscillator

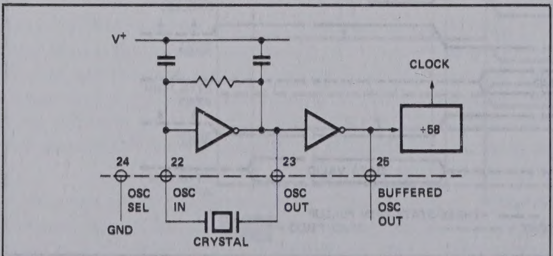


Figure 11: TSC7109 Crystal Oscillator

When the oscillator is to be overdriven, the OSCILLATOR OUTPUT should be left open, and the overdriving signal should be applied at the OSCILLATOR INPUT. The internal clock will be of the same duty cycle, frequency and phase as the input signal. When the OSCILLATOR SELECT is at GND, the clock will be 1/58 of the input frequency.

Test Input

The counter and its outputs may be tested easily. When the TEST input is connected to GND, the internal clock is disabled, and the counter outputs are all forced into the high state. When the input returns to the 1/2 (V^+ -GND) voltage or to V^+ and one clock is input, the counter outputs will all be clocked to the low state.

The counter output latched are enabled when the TEST input is taken to a level halfway between V^+ and GND allowing the counter contents to be examined anytime.

Component Value Selection

The integrator output swing for full-scale should be as large as possible. For example, with +5 V supplies and COMMON connected to GND, the nominal integrator output swing at full-scale is ±4 V. Since the integrator output can go to 0.3 V from either supply without significantly affecting linearity, a 4 V integrator output swing allows 0.7 V for variations in output swing due to component value and oscillator tolerances. With ±5 V supplies and a common-mode voltage range of ±1 V required, the component values should be selected to provide ±3 V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4 V case. For large common-mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, ±6 V supplies may be used.

Integrating Capacitor

The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing that will not saturate the integrator to within 0.3 volt from either supply. A ±3.5 to ±4 volt integrator output swing is nominal for the TSC7109 with ±5 volt supplies and analog common connected to GND. For 7-1/2 conversions per second (61.72 kHz internal clock frequency) nominal values C_{INT} and C_{AZ} are 0.15 μF and 0.33 μF, respectively. These values should be changed if different clock frequencies are used to maintain the integrator output voltage swing. The value of C_{INT} is given by:

$$C_{INT} = \frac{(2048 \times \text{Clock Period})\ (20\ \mu)}{\text{Integrator Output Voltage Swing}}$$

The integrating capacitor must have low dielectric absorption to prevent rollover errors. Polypropylene capacitors give undetectable errors at reasonable cost up to 85° C. Teflon® capacitors are recommended for the military temperature range. While their dielectric absorption characteristics vary somewhat between units, devices may be selected to less than 0.5 count of error due to dielectric absorption.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 100 μA of quiescent current. They supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 4.095 volt full-scale a 200 kΩ and for 409.6 mV full-scale a 20 kΩ are recommended. R_{INT} may be selected for other values of full-scale by:

$$R_{INT} = \frac{\text{Full-Scale Voltage}}{20\ \mu\text{A}}$$

Auto-Zero Capacitor

As the auto-zero capacitor is made large the system noise is reduced. Since it is in parallel with the integrating capacitor, it forms an RC time constant that determines the error that exists at the end of an auto-zero cycle and speed of recovery from overloads. For 4.096 V full-scale where recovery is most important, a value of C_{AZ} equal to half of C_{INT} should be used.

For 409.6 mV full-scale where noise is very important and the integrating resistor is small, use a value of C_{AZ} twice C_{INT}. The inner foil of C_{AZ} should be connected to pin 31 and the outer foil to the RC summing junction. The inner foil of C_{INT} should be connected to the RC summing junction and the outer foil to pin 32 for best rejection of the stray pickup. For low leakage at temperatures above 85°C use Teflon® capacitors.

Reference Capacitor

A 1 μF capacitor is recommended for most circuits. However, where a large common-mode voltage exists a larger value is required to prevent rollover error (for example: the reference low is not analog common) and a 409.6 mV scale is used. The rollover error will be held to 0.5 count with a 10 μF capacitor. For temperatures above 80°C use Teflon® or equivalent capacitors for their low leakage characteristics.

Reference Voltage

To generate full-scale output of 4096 counts the analog input required is $V_{IN} = 2\ V_{REF}$. For a 4.096 V full-scale use a reference of 2.048 V. In many applications where the A/D is connected to a transducer, there will exist a scale factor between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage from the transducer is 700 mV. Instead of dividing the input down to 409.6 mV, the designer should use the input voltage directly and select $V_{REF} = 350$ mV. Suitable values for integrating resistor and capacitor would be 34 k and 0.15 μF. This makes the system slightly quieter and also avoids a divider network on the input. Another advantage of this system occurs when temperature and weight measurements with an offset or tare are desired for non-zero input. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. In processor-based systems using the TSC7109, it may be more desirable to use software and perform this type of scaling or tare subtraction digitally.

Reference Sources

A major factor in the absolute accuracy of the converter is the stability of the reference voltage. The 12-bit resolution of the TSC7109 is one part in 4096, or 244 ppm. Thus, for the on-board reference temperature coefficient of 80 ppm/°C a temperature difference of 3°C will introduce a one-bit absolute error. Where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made it is recommended that an external high-quality reference be used.

A Reference Output (pin 29) is provided which may be used with a resistive divider to generate a suitable reference voltage. 20 mA may be sunk without significant variation in output voltage. A pullup bias device is provided which sources about 10 μA. The output voltage is nominally 2.8 V below V^+. When using the on-board reference, Ref Out (pin 29) should be connected to Ref — (Pin 39), and Ref + should be connected to the wiper of a precision potentiometer between Ref Out and V^+. The test circuit shows the circuit for a 204.8 mV reference, generated by a 2 kΩ precision potentiometer in series with a 24 kΩ fixed resistor.

8

Interfacing

Direct Mode

Combinations of chip enable and byte enable control signals which may be used when interfacing the TSC7109 to parallel data lines as shown in Figure 12. The $\overline{\text{CE}}/\overline{\text{LOAD}}$ input may be tied low, allowing either byte to be controlled by its own enable (Figure 12A). Figure 12B shows the $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ as flag inputs, and $\overline{\text{CE}}/\overline{\text{LOAD}}$ as a master enable, which could be the READ strobe available from most microprocessors. Figure 12C shows a configuration where the two byte enables are connected together. The $\overline{\text{CE}}/\overline{\text{LOAD}}$ is a chip enable, and the $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ may be used as a second chip enable or connected to ground. The 14 data outputs will be enabled at the same time. In the direct MODE, SEND should be tied to V^+.

Figure 13 interfaces several TSC7109's to a bus, ganging the $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ signals to several converters together, and using the $\overline{\text{CE}}/\overline{\text{LOAD}}$ inputs to select the desired converter.

Figures 14-19 give practical circuits utilizing the parallel tri-state output capabilities of the TSC7109. Figure 14 shows parallel interface to the intel MCS-48, -80 and -85 systems via an 8255 PPI, where the TSC7109 data outputs are active at all times. The 8155 I/O ports may be used in an identical manner. This interface can be used in an identical manner. This interface can be used in a read-after-update sequence, as shown in Figure 15. The data is accessed by the high to low transition of the STATUS driving an interrupt to the microprocessor.

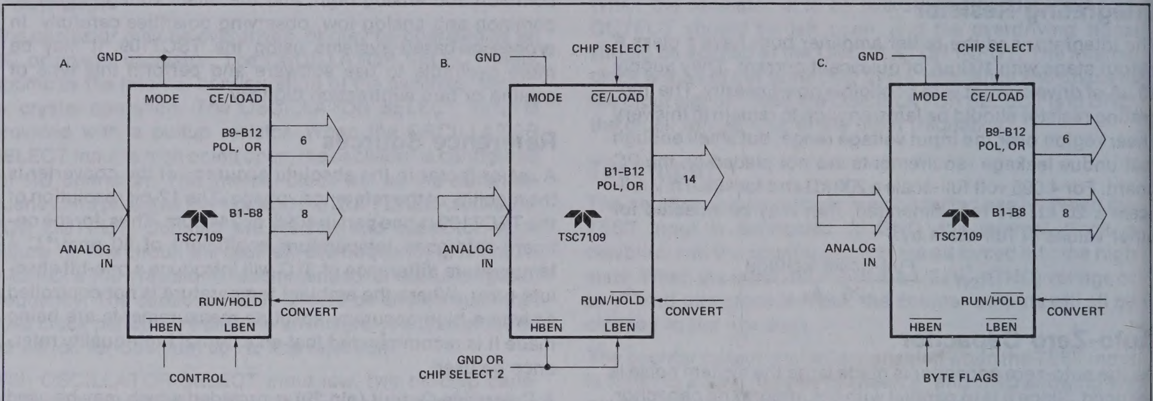

A.
GND
MODE
CE/LOAD
B9-B12
POL, OR
6
B1-B8
8
TSC7109
ANALOG
IN
RUN/HOLD
CONVERT
HBEN
LBEN
CONTROL
B.
GND
CHIP SELECT 1
MODE
CE/LOAD
B1-B12
POL, OR
14
TSC7109
ANALOG
IN
RUN/HOLD
CONVERT
HBEN
LBEN
GND OR
CHIP SELECT 2
C.
GND
CHIP SELECT
MODE
CE/LOAD
B9-B12
POL, OR
6
B1-B8
8
TSC7109
ANALOG
IN
RUN/HOLD
CONVERT
HBEN
LBEN
BYTE FLAGS

Figure 12: Direct Mode Chip and Byte Enable Combinations

The RUN/HOLD input is also used to initiate conversions under software control. Figure 16 gives an interface to Motorola MC6800 or MOS technology MCS650X systems.

An interrupt is generated through the control Resistor B, CB1 line from the high to low transition of the STATUS output. The RUN/HOLD pin is controlled by CB2 through Control Register B, allowing software control of conversions.

Direct interfacing to most microprocessor busses is easily accomplished through the tri-state output of the TSC7109.

Figures 1B, 17 and 18 are typical connection diagrams. To be sure that requirements for setup and hold times, minimum pulse widths, and the drive limitations on long busses are met, it is necessary to carefully consider the system timing in this type of interface. This type of interface is used when the memory peripheral address density is low providing simply address decoding. Interrupt handling can be simplified by using an interface to reduce the component count.

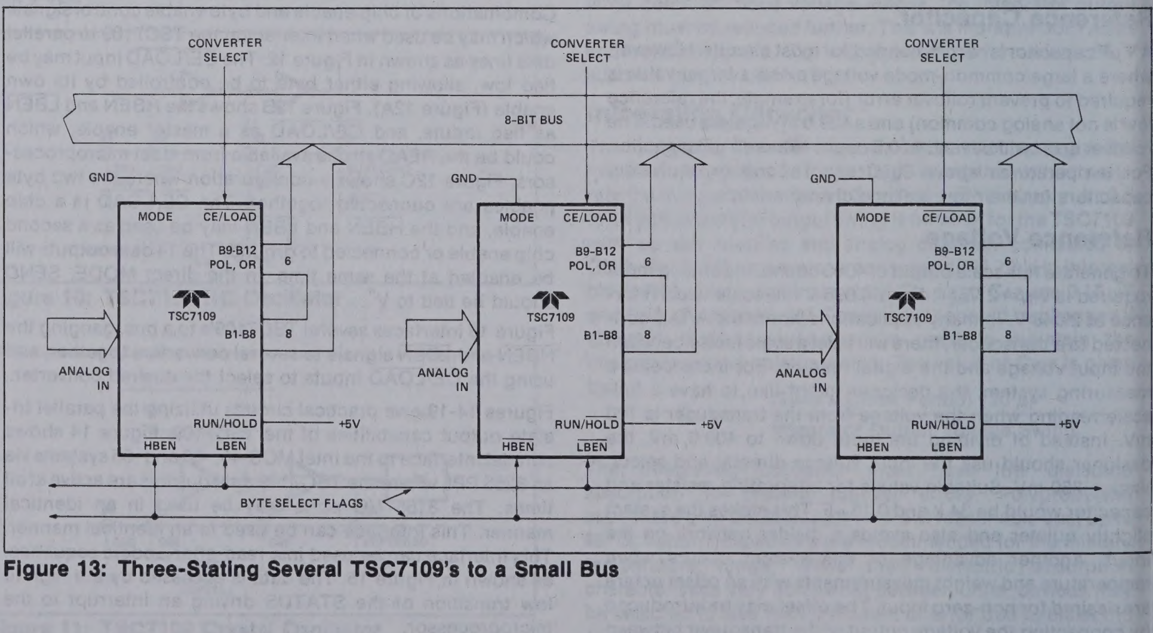

CONVERTER
SELECT
CONVERTER
SELECT
CONVERTER
SELECT
8-BIT BUS
GND
MODE
CE/LOAD
B9-B12
POL, OR
6
TSC7109
B1-B8
8
ANALOG
IN
RUN/HOLD
+5V
HBEN
LBEN
GND
MODE
CE/LOAD
B9-B12
POL, OR
6
TSC7109
B1-B8
8
ANALOG
IN
RUN/HOLD
+5V
HBEN
LBEN
GND
MODE
CE/LOAD
B9-B12
POL, OR
6
TSC7109
B1-B8
8
ANALOG
IN
RUN/HOLD
+5V
HBEN
LBEN
BYTE SELECT FLAGS

Figure 13: Three-Stating Several TSC7109's to a Small Bus

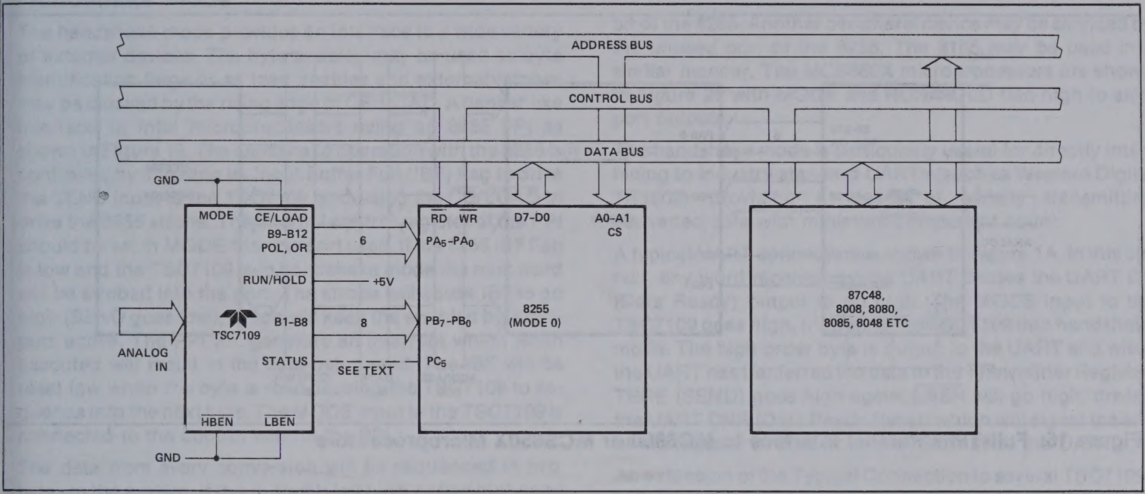

ADDRESS BUS
CONTROL BUS
DATA BUS
GND
MODE
CE/LOAD
B9-B12
POL, OR
6
RUN/HOLD
+5V
TSC7109
B1-B8
8
ANALOG IN
STATUS
SEE TEXT
HBEN
LBEN
GND
RD
WR
D7-D0
A0-A1
CS
PA5-PA0
8255
(MODE 0)
PB7-PB0
PC5
87C48,
8008, 8080,
8085, 8048 ETC

Figure 14: Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputer Systems

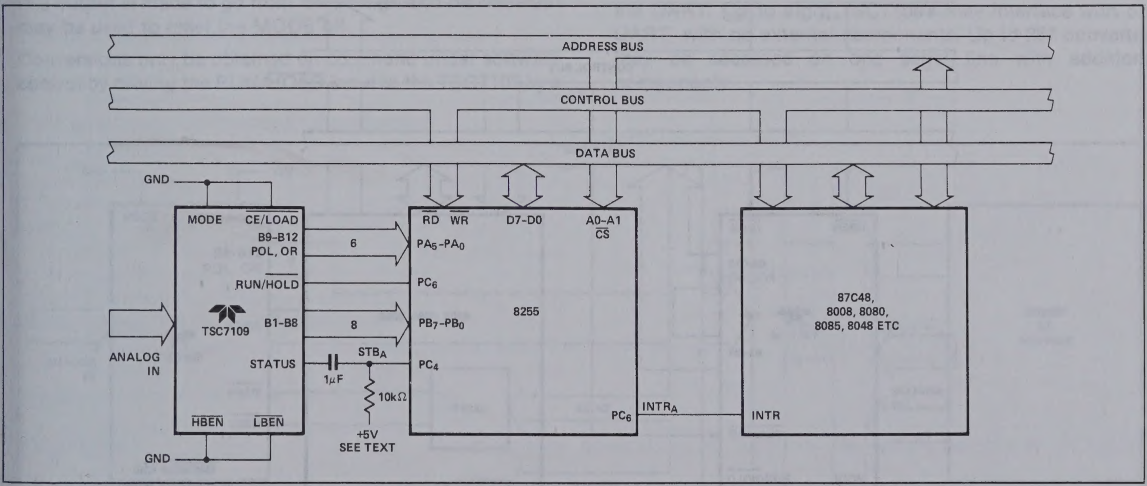

ADDRESS BUS
CONTROL BUS
DATA BUS
GND
MODE
CE/LOAD
B9-B12
POL, OR
6
RUN/HOLD
TSC7109
B1-B8
8
ANALOG IN
STATUS
STBA
1µF
10kΩ
+5V
SEE TEXT
HBEN
LBEN
GND
RD
WR
D7-D0
A0-A1
CS
PA5-PA0
PC6
8255
PB7-PB0
PC4
PC6
INTRA
INTR
87C48,
8008, 8080,
8085, 8048 ETC

Figure 15: Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputers with Interrupt

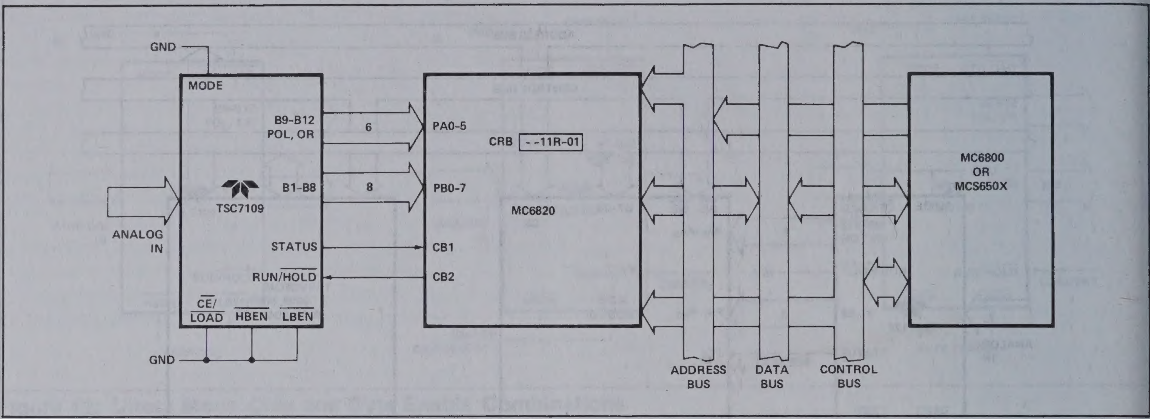

GND
MODE
B9-B12
POL, OR
6
PA0-5
CRB
--11R-01
TSC7109
B1-B8
8
PB0-7
MC6820
MC6800
OR
MCS650X
ANALOG
IN
STATUS
CB1
RUN/HOLD
CB2
CE/
LOAD
HBEN
LBEN
GND
ADDRESS
BUS
DATA
BUS
CONTROL
BUS

Figure 16: Full-Time Parallel Interface to MC6800 or MCS650X Microprocessors

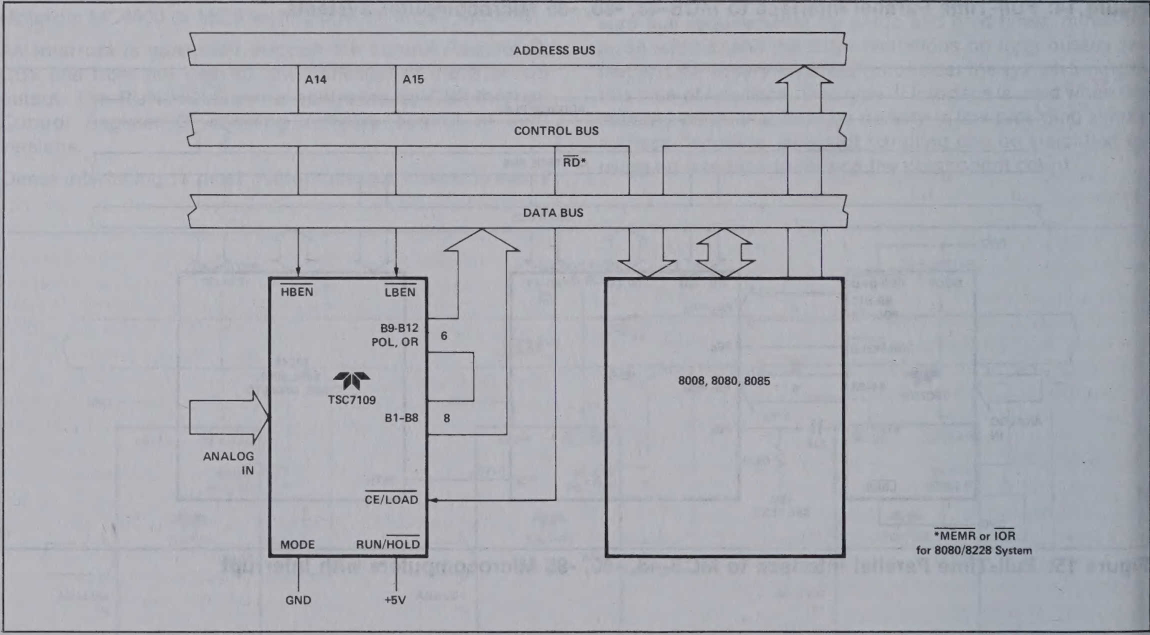

ADDRESS BUS
A14
A15
CONTROL BUS
RD*
DATA BUS
HBEN
LBEN
B9-B12
POL, OR
6
TSC7109
B1-B8
8
8008, 8080, 8085
ANALOG
IN
CE/LOAD
MODE
RUN/HOLD
GND
+5V
*MEMR or IOR
for 8080/8228 System

Figure 17: Direct Interface — TSC7109 to 8080/8085

Handshake Mode

The handshake mode provides an interface to a wide variety of external devices. The byte enables may be used as byte identification flags or as load enables and external latches may be clocked by the rising edge of CE/$\overline{\text{LOAD}}$. A handshake interface to Intel microprocessors using an 8255 PPI as shown in Figure 19. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the TSC7109, and using the CE/$\overline{\text{LOAD}}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 8255 IBF flag is low and the TSC7109 is in handshake mode the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. The IBF will be reset low when the byte is read causing the TSC7109 to sequence into the next byte. The MODE input to the TSC7109 is connected to the control line on the PPI.

The data from every conversion will be sequenced in two bytes in the system, if this output is left high, or tied high separately. (The data access must take less time than a conversion). The output sequence can be obtained on demand if this output is made to go from low to high and the interrupt may be used to reset the MODE bit.

Conversions may be obtained on command under software control by driving the RUN/$\overline{\text{HOLD}}$ input to the TSC7109 by a bit of the 8255. Another peripheral device may be serviced by the unused port of the 8255. The 8155 may be used in a similar manner. The MCS650X microprocessors are shown in Figure 20 with MODE and RUN/$\overline{\text{HOLD}}$ tied high to save port outputs.

The handshake mode is particularly useful for directly interfacing to industry standard UARTs (such as Western Digital TR1602) providing a means of serially transmitting converted data with minimum component count.

A typical UART connection is shown in Figure 1A. In this circuit, any word received by the UART causes the UART DR (Data Ready) output to go high. The MODE input to the TSC7109 goes high, triggering the TSC7109 into handshake mode. The high order byte is output to the UART and when the UART has tranferred the data to the Transmitter Register, TBRE (SEND) goes high again, $\overline{\text{LBEN}}$ will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the TSC7109 to the UART.

An extension of the Typical Connection to several TSC7109's with one UART is shown in Figure 21. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. Up to eight TSC7109's may interface with one UART, with no external components. Up to 256 converters may be accessed on one serial line with additional components.

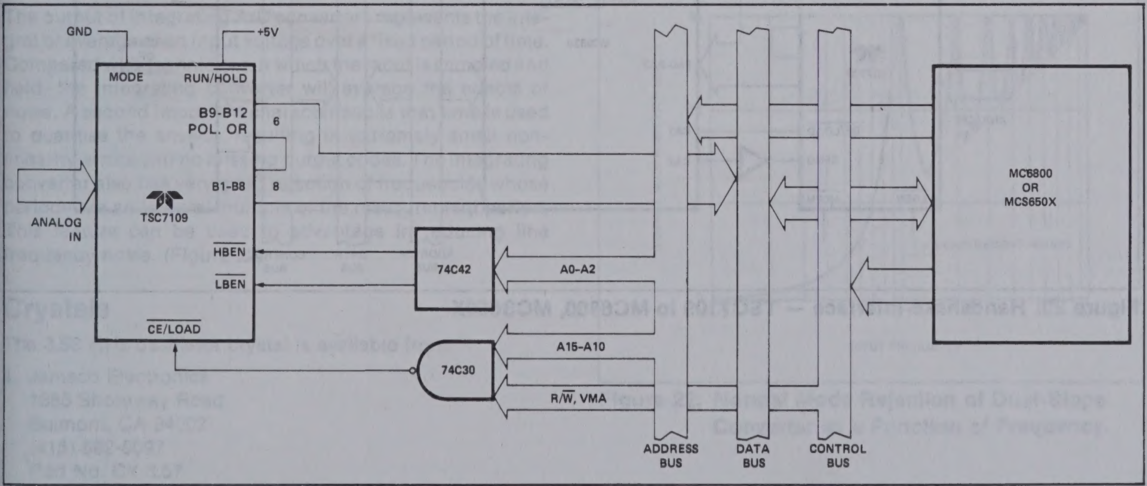


Figure 18: Direct TSC7109 — MC6800 Bus Interface

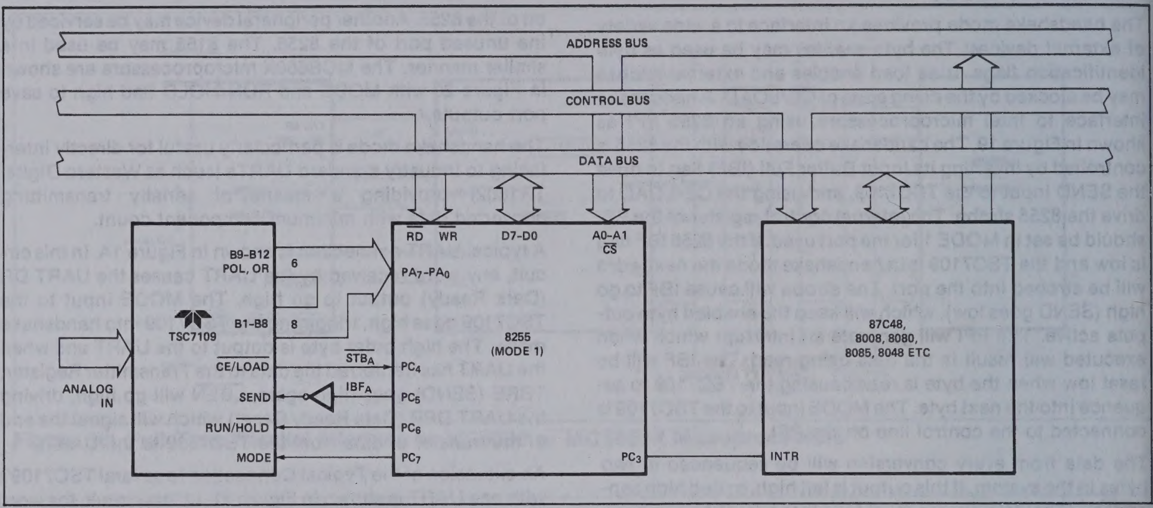

ADDRESS BUS
CONTROL BUS
DATA BUS
B9-B12
POL, OR
6
TSC7109
B1-B8
8
CE/LOAD
ANALOG IN
SEND
RUN/HOLD
MODE
STB_A
IBF_A
$\overline{RD}$
$\overline{WR}$
D7-D0
A0-A1
$\overline{CS}$
PA_7-PA_0
8255
(MODE 1)
PC_4
PC_5
PC_6
PC_7
PC_3
INTR
87C48,
8008, 8080,
8085, 8048 ETC

Figure 19: Handshake Interface — TSC7109 to MCS-48, -80, -85

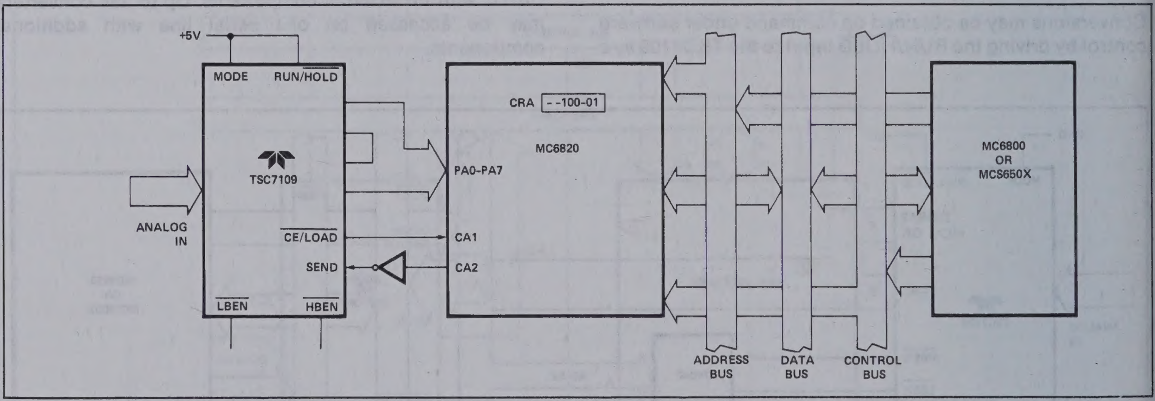

+5V
MODE
$\overline{RUN/HOLD}$
TSC7109
ANALOG IN
$\overline{CE/LOAD}$
SEND
$\overline{LBEN}$
$\overline{HBEN}$
CRA
- -100-01
MC6820
PA0-PA7
CA1
CA2
MC6800
OR
MCS650X
ADDRESS BUS
DATA BUS
CONTROL BUS

Figure 20: Handshake Interface — TSC7109 to MC6800, MCS650X

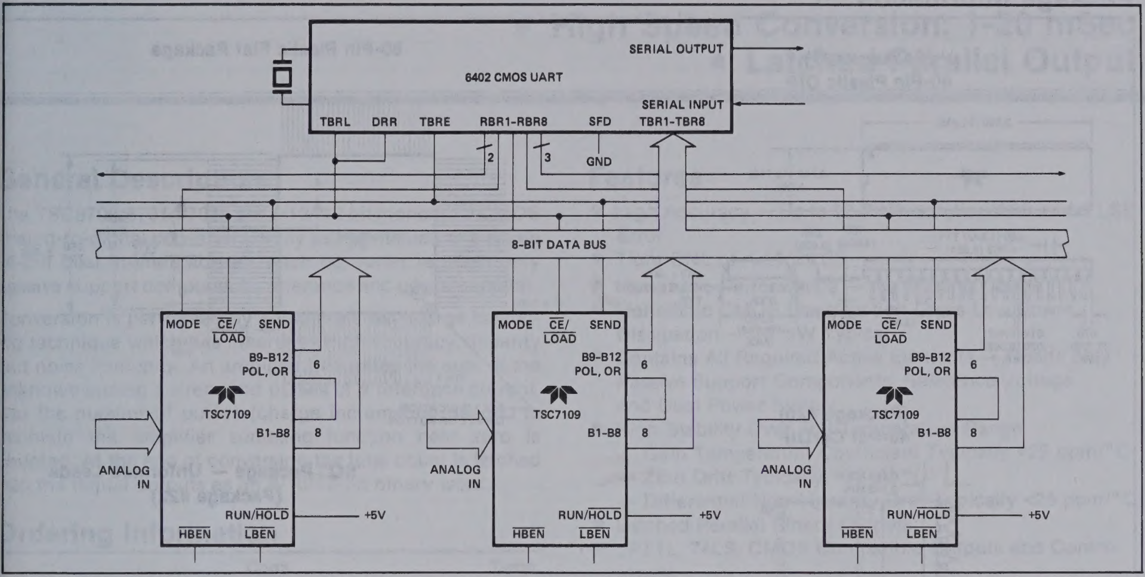

6402 CMOS UART
SERIAL OUTPUT
SERIAL INPUT
TBRL
DRR
TBRE
RBR1-RBR8
SFD
TBR1-TBR8
2
3
GND
8-BIT DATA BUS
MODE
CE/LOAD
SEND
B9-B12
POL, OR
6
TSC7109
B1-B8
8
ANALOG IN
RUN/HOLD
+5V
HBEN
LBEN

Figure 21: Handshake Interface for Multiplexed Converters

Integrating Converter Features

The output of Integrating A/D converters represents the integral or average of an input voltage over a fixed period of time. Compared with techniques in which the input is sampled and held, the integrating converter will average the effects of noise. A second important characteristic is that time is used to quantise the answer, resulting in extremely small nonlinearity errors and no missing output codes. The integrating converter also has very good rejection of frequencies whose periods are an integral multiple of the measurement period. This feature can be used to advantage in reducing line frequency noise. (Figure 22)

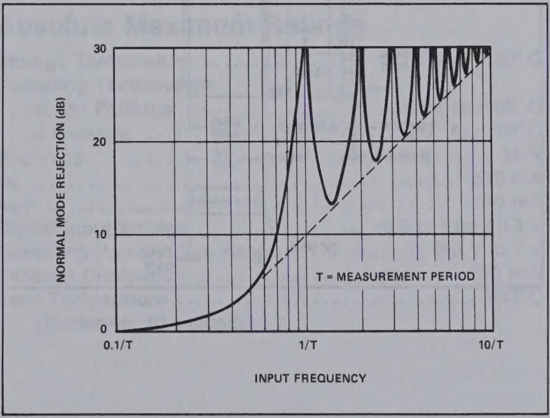


Figure 22: Normal Mode Rejection of Dual-Slope Converter as a Function of Frequency.

Crystals

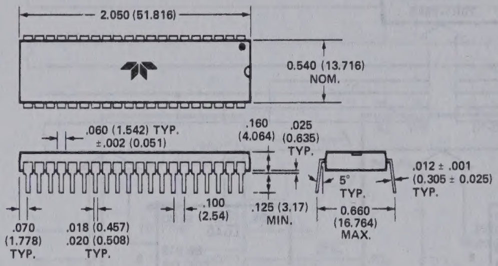
The 3.58 mHz oscillator crystal is available from:

1. Jameco Electronics
   1355 Shoreway Road
   Belmont, CA 94002
   (415) 592-8097
   Part No. CY 3.57

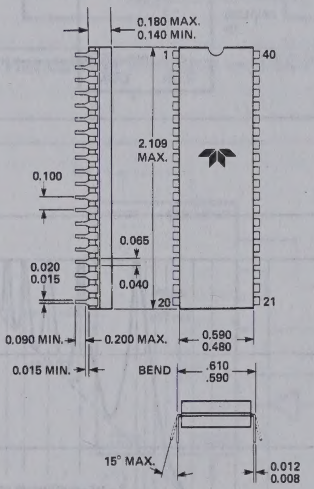
2. DIGI-KEY Corp.
   Highway 32 South
   P.O. Box 677
   Thief River Falls, MN 56701-9988
   1-800-344-4539
   Part No. X0005

Package Information

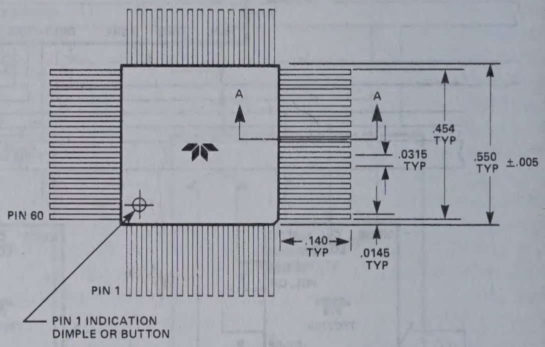
(Package #17)
40-Pin Plastic DIP


2.050 (51.816)
0.540 (13.716)
NOM.
.060 (1.542) TYP.
±.002 (0.051)
.160
(4.064)
.025
(0.635)
TYP.
5°
TYP.
.012 ± .001
(0.305 ± 0.025)
TYP.
.070
(1.778)
TYP.
.018 (0.457)
.020 (0.508)
TYP.
.100
(2.54)
.125 (3.17)
MIN.
0.660
(16.764)
MAX.

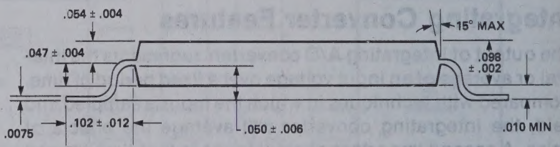
(Package #20)
40-Pin CerDIP


0.180 MAX.
0.140 MIN.
1
40
2.109
MAX.
0.100
0.065
0.020
0.015
0.040
20
21
0.090 MIN.
0.200 MAX.
0.590
0.480
0.015 MIN.
BEND
.610
.590
15° MAX.
0.012
0.008

60-Pin Plastic Flat Package


A
A
.454
TYP
.0315
TYP
.550
TYP
±.005
PIN 60
.140
TYP
.0145
TYP
PIN 1
PIN 1 INDICATION
DIMPLE OR BUTTON

"SQ" Package — Unformed Leads
(Package #22)


.054 ± .004
15° MAX
.047 ± .004
.098
± .002
.0075
.102 ± .012
.050 ± .006
.010 MIN

"BQ" Package — Formed Leads
(Package #21)

TELEDYNE SEMICONDUCTOR

TSC8700 (8-Bit)
TSC8701(10-Bit)
TSC8702(12-Bit)
Binary Output ADCs

- **High Speed Conversion: 1-20 mSec**
- **Latched Parallel Output**

General Description

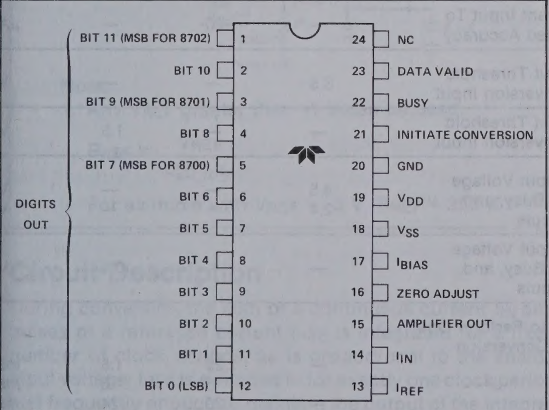
The TSC8700/8701/8702s are 8/10/ 12 bit monolithic CMOS analog-to-digital converters. Fully self-contained in a single 24-pin dual in-line package, each converter requires only passive support components, reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero is counted. At the end of conversion the total count is latched into the digital outputs as an 8/10/12-bit binary word.

Ordering Information

Part No.	Resolution	Conv. Time	Package	Temp. Range
TSC8700CJ	8-Bit	1.25 mSec	24-Pin Plastic Dip	0° C to +70° C
TSC8700CL	8-Bit	1.25 mSec	24-Pin CerDIP	-40° C to +85° C
TSC8701CL	10-Bit	5.0 mSec	24-Pin CerDIP	-40° C to +85° C
TSC8702CN	12-Bit	20 mSec	24-Pin Ceramic	-40° C to +85° C

Pin Configuration



Note:
Do not make connections to pin 1, 2, 3 or 4 on 8700; pin 1 or 2 on 8701. These pins are internally connected.

Features

- High Accuracy — Up to 12-Bit Resolution With < ±1/2 LSB Error
- Tight DNL of < ±1/2 LSB
- Monotonic Performance — No Missing Codes
- Monolithic CMOS Construction Gives Low Power Dissipation — 20 mW Typical
- Contains All Required Active Elements — Needs only Passive Support Components, Reference Voltage and Dual Power Supply
- High Stability Over Full Temperature Range
  - Gain Temperature Coefficient Typically <25 ppm/° C
  - Zero Drift Typically <30 μV/° C
  - Differential Non-Linearity Drift Typically <25 ppm/° C
- Latched Parallel Binary Outputs
- LPTTL, 74LS, CMOS Compatible Outputs and Control Inputs
- Strobed or Free Running Conversion
- Infinite Input Range — Any Positive Voltage Can Be Applied Via a Scaling Resistor

Absolute Maximum Ratings

Storage Temperature	-65° C to + 150° C
Operating Temperature	
(L, N) Package	-40° C to + 85° C
J Package	0° to + 70° C
$V_{DD} - V_{SS}$	18 V
I_{IN}	±10 mA
I_{REF}	±10 mA
Digital Input Voltage	-0.3 to V_{DD} +0.3 V
Operating V_{DD} and V_{SS} Range	3.5 V to 7 V
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300° C

Handling Precautions

The 8700 series are CMOS devices must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

© 1983

Electrical Characteristics: Unless otherwise specified, V_{DD} = +5 V, V_{SS} = -5 V, V_{GND} = 0, V_{REF} = -6.4 V, R_{BIAS} = 100 kΩ, test circuit shown. T_A = 25° C unless Full Temperature Range is specified (-40° C to +85° C for N and L package, 0° to 70° C for J package).

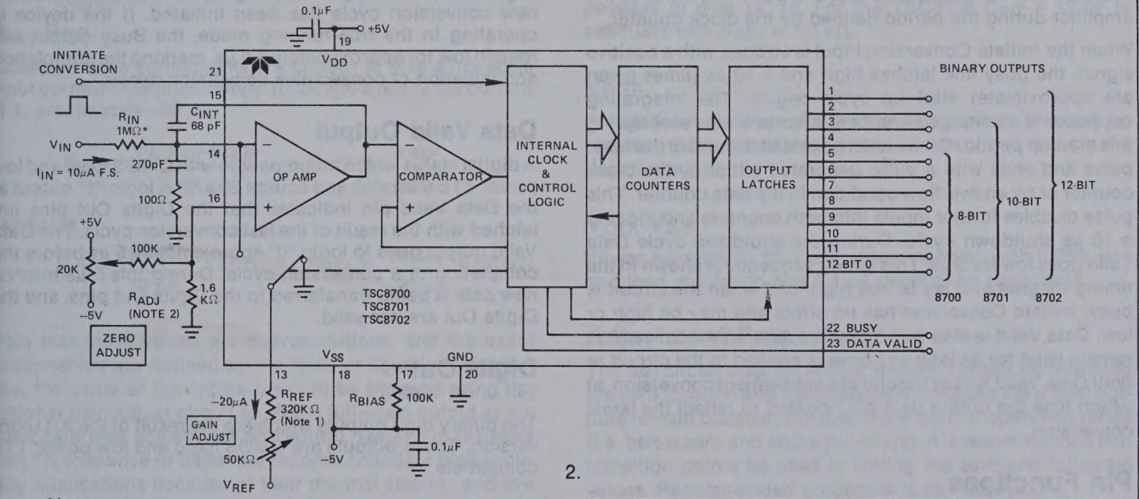
PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	MAX	UNITS
Accuracy						
Resolution Accuracy		Binary Word Length Of Digital Output				
		TSC8700	8	—	—	Bits
		TSC8701	10	—	—	Bits
		TSC8702	12	—	—	Bits
Relative Accuracy		Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	—	±1/2	LSB
Differential Non-Linearity		Deviation From 1 LSB Between Transition Points	—	±1/4	±1/2	LSB
Differential Non-Linearity Temperature Drift	Full Temperature Range	Variation in Differential Non-Linearity Due To Temperature Change	—	±2.5	±5	ppm/° C
Gain Variance		Variation From Exact A (Compensate By Trimming R_{IN} or R_{REF})	—	±2	+5 -3	% of Nominal
Gain Temperature Drift	Full Temperature Range	Variation In A Due To Temperature Change	—	±25	±75	ppm/° C
Zero Offset (TSC8700)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.6 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.6 kΩ	—	—	±80	mV
Zero Offset (TSC8700)	I_{IN} = 0 C_{INT} = 33 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 33 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	mV
Zero Offset (TSC8701) (TSC8702)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	mV
Zero Temperature Drift	Full Temperature Range	Variation in Zero Offest Due to Temperature Change	—	±30	±50	μV/° C
Analog Inputs						
I_{IN} Full-Scale		Full-Scale Analog Input Current To Achieve Specified Accuracy	—	10	—	μA
I_{REF} (Note 1)		Reference Current Input To Achieve Specified Accuracy	—	-20	—	μA
Digital Inputs						
$V_{IN}^{(1)}$	Full Temperature Range	Logical "1" Input Threshold For Initiate Conversion Input	3.5	—	—	V
$V_{IN}^{(0)}$	Full Temperature Range	Logical "0" Input Threshold For Initiate Conversion Input	—	—	1.5	V
Digital Outputs						
$V_{OUT}^{(1)}$	Full Temp. Range I_{OUT} = -10 μA I_{OUT} = -360 μA	Logical "1" Output Voltage For Digits Out, Busy, and Data Valid Outputs	4.5 2.4	— —	— —	V V
$V_{OUT}^{(0)}$	Full Temp. Range V_{DD} = 4.75 V I_{OUT} = 360 μA	Logical "0" Output Voltage For Digits Out, Busy, and Data Valid Outputs	—	—	0.4	V
Dynamic						
Conversion Time	Full Temp. Range	Time Required to Perform One Complete A/D Conversion				
		TSC8700	—	1.25	1.8	ms
		TSC8701	—	5	6	ms
		TSC8702	—	20	24	ms
Conversion Rate in Free-Run Mode	$V_{INT\ CONV}$ = + 5 V	TSC8700	555	800	—	Conv'ns per Second
		TSC8701	167	200	—	
		TSC8702	42	50	—	

Electrical Characteristics (Cont.)

PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	MAX	UNITS
Minimum Pulse Width for Initiate Conversion	Full Temp. Range		500	—	—	ns
Supply Current						
I_{DD} Quiescent (L/N Package) (J Package)	Full Temp. Range $V_{INIT\ CONV}$ = 0V	Current Required From Positive Supply During Operation	— —	1.4 1.4	2.5 5.0	mA mA
I_{SS} Quiescent (L/N Package) (J Package)	Full Temp. Range $V_{INIT\ CONV}$ = 0V	Current Required From Negative Supply During Operation	— —	-1.4 -1.4	-2.5 -5.0	mA mA
Supply Sensitivity	$V_{DD} \pm 1V$, $V_{SS} \pm 1.V$	Change in Full-Scale Gain vs Supply Voltage Change	—	±0.5	±1.0	%/V
	$\lvert V_{DD}\rvert = \lvert V_{SS}\rvert = 5\ V \pm 1$	Change in Full-Scale Gain vs Supply Voltage Change for Tracking Supplies	—	±0.05	±0.1	%/V

NOTE:
I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

Test Circuit


0.1µF
+5V
19
VDD
INITIATE CONVERSION
21
15
CINT 68 pF
RIN 1MΩ*
VIN
IIN = 10µA F.S.
270pF
14
100Ω
16
OP AMP
COMPARATOR
INTERNAL CLOCK & CONTROL LOGIC
DATA COUNTERS
OUTPUT LATCHES
BINARY OUTPUTS
1
2
3
4
5
6
7
8
9
10
11
12 BIT 0
8-BIT
10-BIT
12-BIT
8700
8701
8702
22 BUSY
23 DATA VALID
+5V
100K
20K
1.6 KΩ
RADJ (NOTE 2)
-5V
ZERO ADJUST
TSC8700
TSC8701
TSC8702
VSS
GND
13
18
17
20
-20µA
RREF 320KΩ (Note 1)
RBIAS
100K
GAIN ADJUST
50KΩ
-5V
0.1µF
VREF

Note:
1. Any V_{REF} greater than -1 V can be used.

$$R_{REF} = \frac{V_{REF}}{-20\ \mu A}$$

For example with V_{REF} = -5 V, R_{REF} = 250 K.

2.

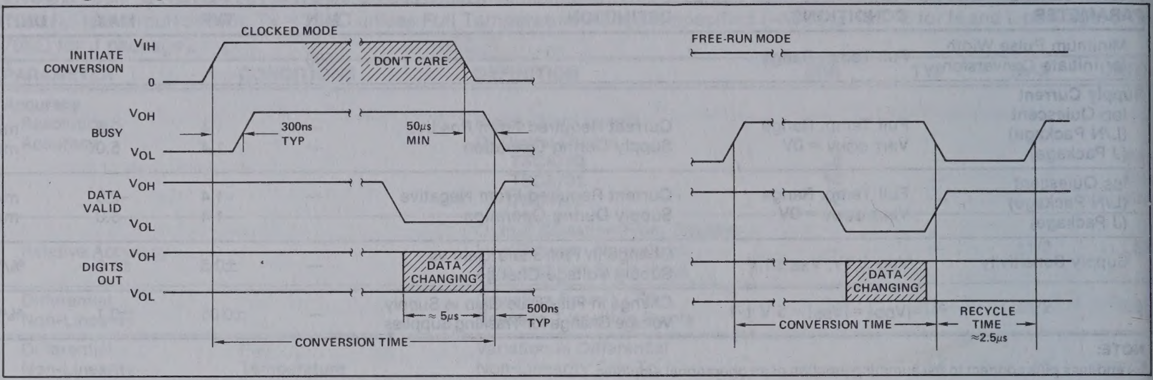
Part No.	R_{ADJ}	C_{INT}	Zero Offset Spec
TSC8700	1.6 kΩ	68 pF	±80 mV
TSC8700	1.0 kΩ	33 pF	±50 mV
TSC8701/8702	1.0 kΩ	68 pF	±50 mV

Circuit Description

During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the output of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in Binary) is latched into the outputs at the end of conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine.

Timing Diagrams (Rise, fall times = 200 ns typ., C_L = 50 pF)



The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10 µs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 µs shutdown cycle. During the shutdown cycle Data Valid goes low for 5 µs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate Conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

Pin Functions

Initiate Conversion Input

Accepts CMOS and most 5 V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500 µA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5 µs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low power TTL (can sink and source 50 µA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5 µs before the completion of a conversion cycle. During this 5 µs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out

(Bit 0, Bit 1, etc.)

The binary digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

Applications Information

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital Counts} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

A = 528 for 8700
A = 2064 for 8701
A = 8208 for 8702

where Digital Counts is the value of the binary output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

Analog Input	Digital Output MSB ... LSB
$V_{IN} \geq$ Full-Scale	1 . . . 111 . . . 1
= Full-Scale −1 LSB	1 . . . 111 . . . 1
= 1 LSB	0 . . . 000 . . . 1
≤ 0	0 . . . 000 . . . 0

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection

Obtaining a high accuracy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1 µF or larger right at the device pins.

R_{IN}, R_{EF}

Values of these components are chosen to give a full-scale input current of approximately 10 µA and a reference current of approximately −20 µA.

$$R_{IN} \cong \frac{V_{IN}\ \text{Full-Scale}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}$$

Examples:

$$R_{IN} \cong \frac{10\ V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4\ V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} Full-Scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS}

Specifications for the TSC87XX are based on R_{BIAS} = 100 kΩ ±10% unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20 k the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When R_{BIAS} = 1 MΩ the conversion time will be six times longer, and the supply current is now reduced to .5 mA). For details of this relationship refer to AN 9 typical performance curves.

R_{DAMP}

Exact value not critical but should have a nominal value of 100 Ω ±10%. Locate close to pin 14.

C_{DAMP}

Exact value not critical but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT}

Exact value not critical but should have a nominal value of 68 pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15. For the TSC8700 C_{INT} = 33 pF is adequate with R_{ADJ} = 1.0 kΩ.

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of ±5 V are recommended, with 0.05% line and load regulation and 0.1 µF decoupling capacitors.

Adjustment Procedure

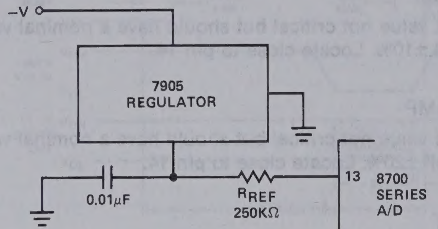
The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full-scale), it is recommended that transition points be used in setting the zero and full-scale values. Recommended procedure is as follows:

- Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
- Set V_{IN} to +1/2 LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
- For full-scale adjustment, set V_{IN} to the full-scale value less 1 1/2 LSB and trim the gain adjust circuit for a 111 . . . 110 to 111 . . . 111 transition.

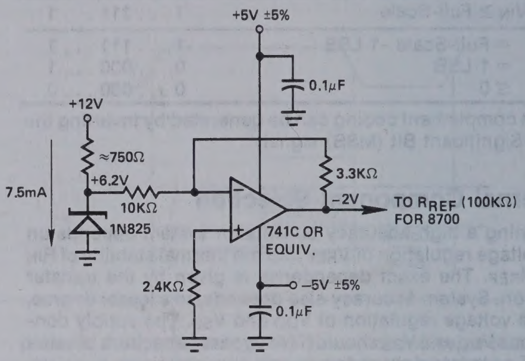
If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

Typical Circuits

Reference Voltage Supply

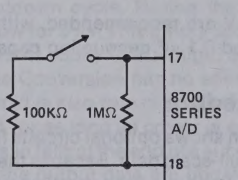

–V
7905
REGULATOR
0.01μF
R_{REF}
250KΩ
13
8700
SERIES
A/D

-5 V Reference

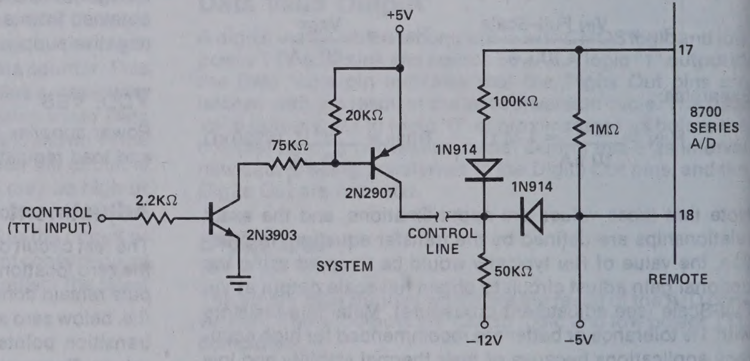

+5V ±5%
0.1μF
+12V
≈750Ω
7.5mA
+6.2V
10KΩ
1N825
3.3KΩ
–2V
TO R_{REF} (100KΩ)
FOR 8700
741C OR
EQUIV.
2.4KΩ
–5V ±5%
0.1μF

-2 V Reference for 8700 Using Voltages Derived From 8080A μP

Power Reduction (Reduces Power Consumption to Approximately 500 μA).

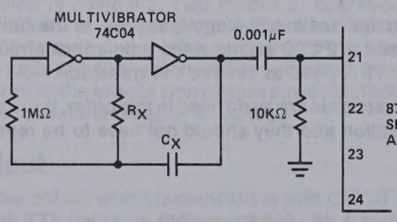

17
100KΩ
1MΩ
8700
SERIES
A/D
18

Switch Controlled - Relay
Could be Substituted for Switch


+5V
17
20KΩ
100KΩ
8700
SERIES
A/D
1MΩ
75KΩ
1N914
2N2907
1N914
CONTROL
(TTL INPUT)
2.2KΩ
18
2N3903
CONTROL
LINE
SYSTEM
50KΩ
REMOTE
–12V
–5V

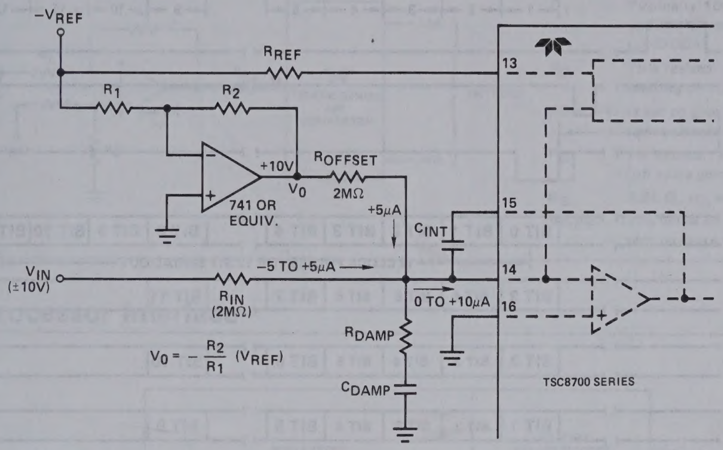
TTL System-Controlled — Trades Off Additional Power Consumption at System for Reduced Usage at Remote A/D

Free-Running Conversion Rate Control


MULTIVIBRATOR
74C04
0.001μF
21
1MΩ
R_X
10KΩ
22
8700
SERIES
A/D
C_X
23
24

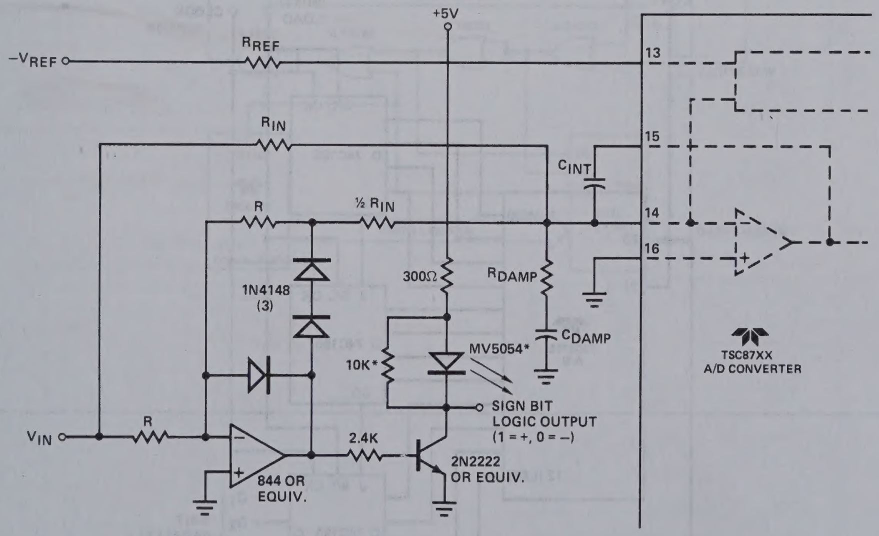
Multivibrator circuit at Pin 21 (Initiate Conversion) strobes converter at rates slower than the normal free-run mode. ($\tau = R_XC_X$)

Bipolar Operation


$-V_{REF}$
R_{REF}
R_1
R_2
+10V
R_{OFFSET}
V_0
2MΩ
741 OR EQUIV.
+5μA
C_{INT}
V_{IN} (±10V)
−5 TO +5μA
R_{IN} (2MΩ)
0 TO +10μA
R_{DAMP}
$V_0 = -\frac{R_2}{R_1}(V_{REF})$
C_{DAMP}
13
15
14
16
TSC8700 SERIES

Two's complement coding may be generated by inverting the MSB output.

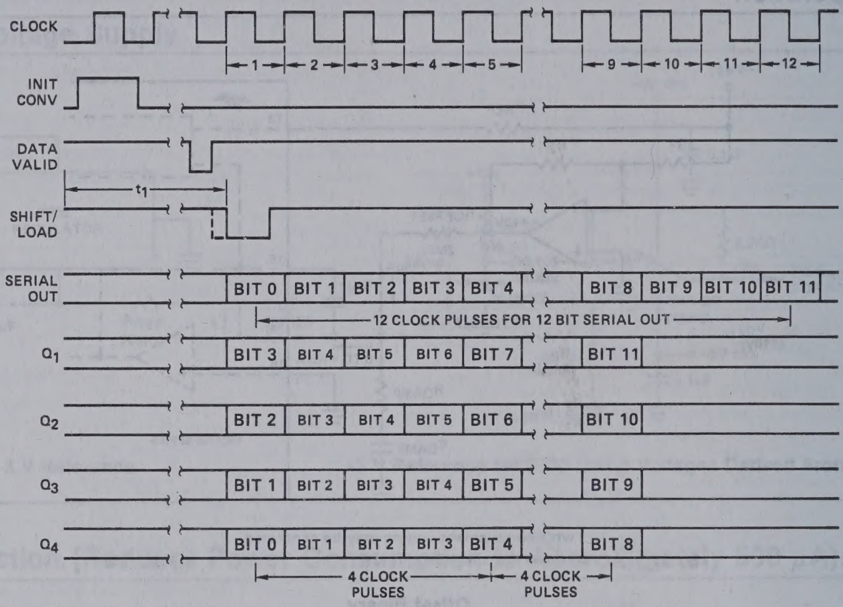
Offset Binary


+5V
$-V_{REF}$
R_{REF}
R_{IN}
R
½ R_{IN}
C_{INT}
1N4148 (3)
300Ω
R_{DAMP}
C_{DAMP}
10K*
MV5054*
SIGN BIT LOGIC OUTPUT (1 = +, 0 = −)
V_{IN}
R
2.4K
2N2222 OR EQUIV.
844 OR EQUIV.
13
15
14
16
TSC87XX A/D CONVERTER

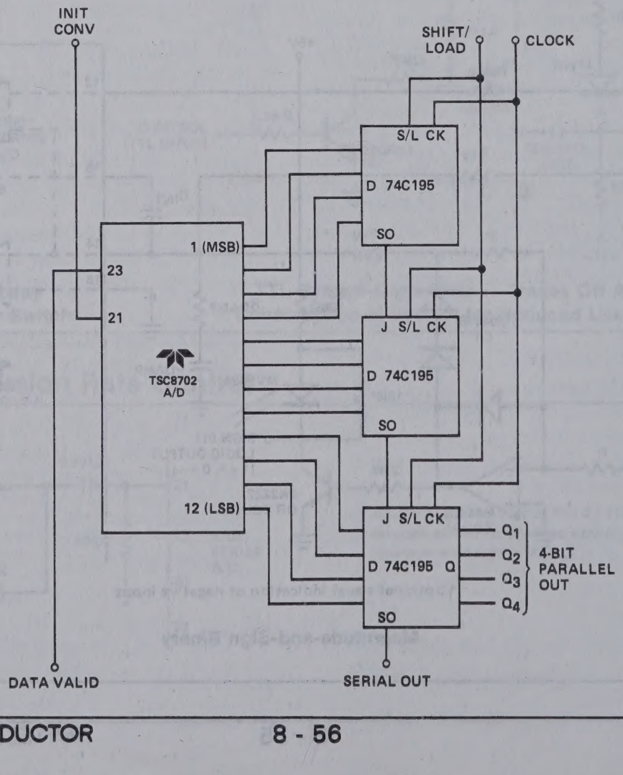
*Optional visual indication of negative input

Magnitude-and-Sign Binary

12-Bit Serial or 3 x 4-Bit Parallel Output Format


CLOCK
1
2
3
4
5
9
10
11
12
INIT CONV
DATA VALID
t1
SHIFT/ LOAD
SERIAL OUT
BIT 0
BIT 1
BIT 2
BIT 3
BIT 4
BIT 8
BIT 9
BIT 10
BIT 11
12 CLOCK PULSES FOR 12 BIT SERIAL OUT
Q1
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 11
Q2
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 10
Q3
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 9
Q4
BIT 0
BIT 1
BIT 2
BIT 3
BIT 4
BIT 8
4 CLOCK PULSES
4 CLOCK PULSES

System reads parallel outputs at clock pulse 1, 5, 9.
Shift/load may be taken low when Data Valid goes high or at fixed time t₁, after INIT CONV (t₁ ≥ 24 ms for TSC8702). Shift/load then must return high before clock pulse 2 and must remain high until all data is read out. Recommended clock frequency 2 kHz min for serial, 750 Hz min for parallel output.

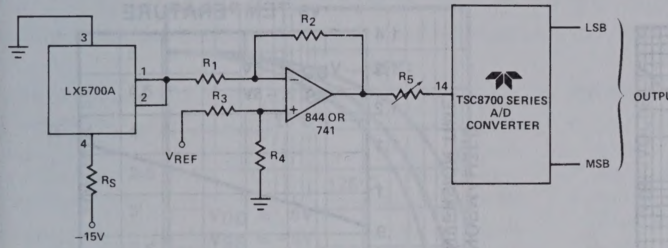

INIT CONV
SHIFT/ LOAD
CLOCK
S/L CK
D 74C195
SO
1 (MSB)
23
21
TSC8702 A/D
J S/L CK
D 74C195
SO
12 (LSB)
J S/L CK
D 74C195 Q
SO
Q1
Q2
Q3
Q4
4-BIT PARALLEL OUT
DATA VALID
SERIAL OUT

Binary Output ADCs

- **High Speed Conversion: 1-20 mSec**
- **Latched Parallel Outputs**

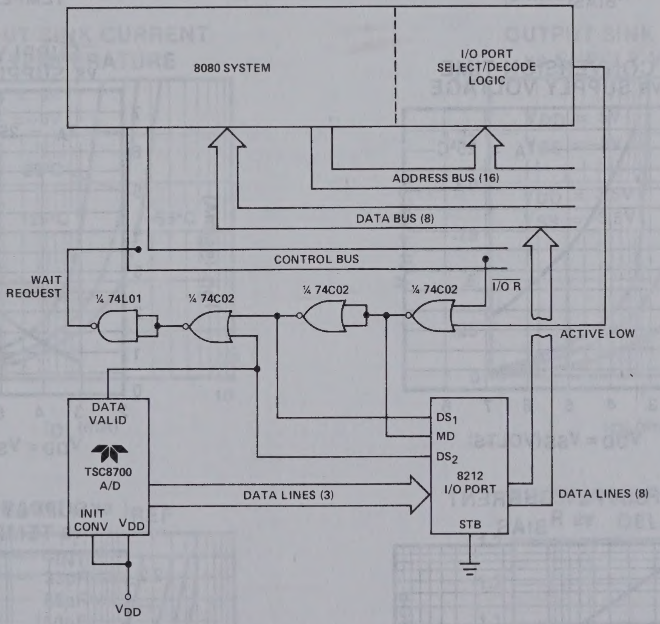
TSC8700 (8-Bit)
TSC8701 (10-Bit)
TSC8702 (12-Bit)

Digital Temperature Monitor


LX5700A
3
1
2
4
R2
R1
R3
R5
14
844 OR 741
VREF
R4
RS
−15V
TSC8700 SERIES A/D CONVERTER
LSB
MSB
OUTPUTS

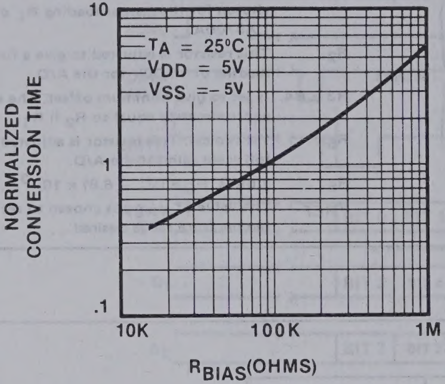
R_1.	Typically 10K min. This resistor should be chosen for the proper loading R_L of the LX5700A.
R_2.	This resistor is adjusted to give a full scale reading of 10.00V for the A/D.
R3 = R4.	Is set to give minimum offset. The value is approximately equal to $R_2 \parallel R_1$.
R_5.	1M typical. This resistor is adjusted to give full scale gain for the A/D.
R_S.	7.5KΩ. $R_S = (V^+ - 6.8) \times 10^{-3}\Omega$.
V_{REF}.	The value of V_{REF} is chosen to set the temperature range desired.

8-Bit Microprocessor Interface

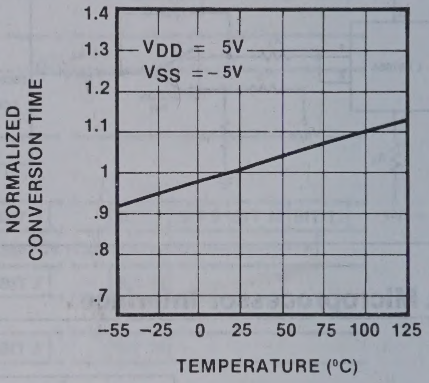

8080 SYSTEM
I/O PORT SELECT/DECODE LOGIC
ADDRESS BUS (16)
DATA BUS (8)
CONTROL BUS
WAIT REQUEST
¼ 74L01
¼ 74C02
¼ 74C02
¼ 74C02
I/O R
ACTIVE LOW
DATA VALID
TSC8700 A/D
INIT CONV
VDD
VDD
DATA LINES (3)
DS1
MD
DS2
8212 I/O PORT
STB
DATA LINES (8)

TYPICAL PERFORMANCE CURVES

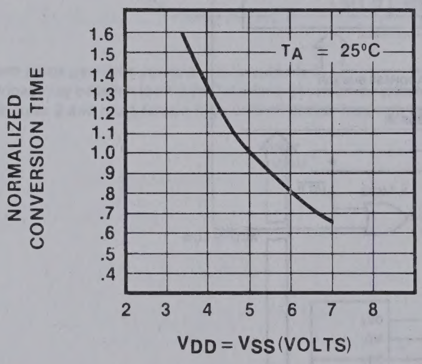
CONVERSION TIME vs R_{BIAS}



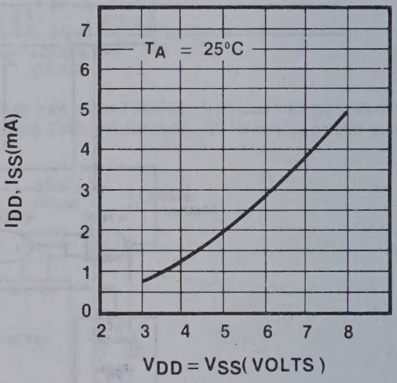
CONVERSION TIME vs TEMPERATURE



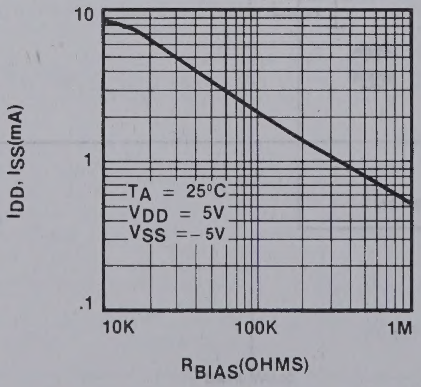
CONVERSION TIME vs SUPPLY VOLTAGE



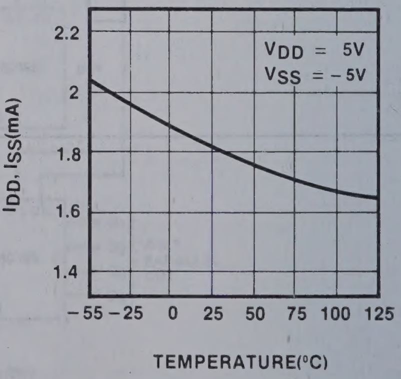
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs R_{BIAS}

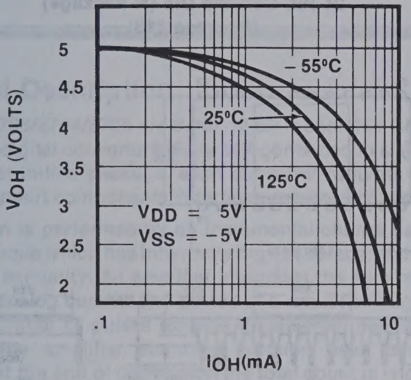


SUPPLY CURRENT vs TEMPERATURE

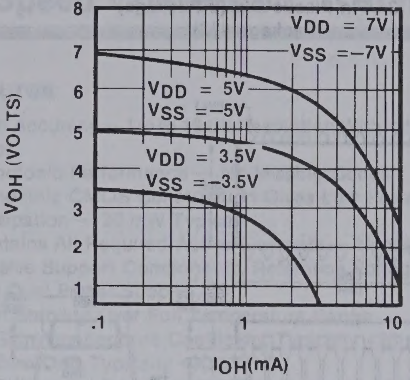


TYPICAL PERFORMANCE CURVES

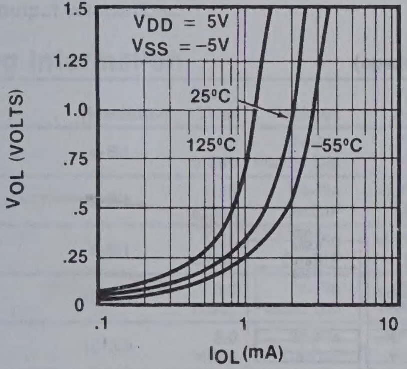
OUTPUT SOURCE CURRENT vs TEMPERATURE



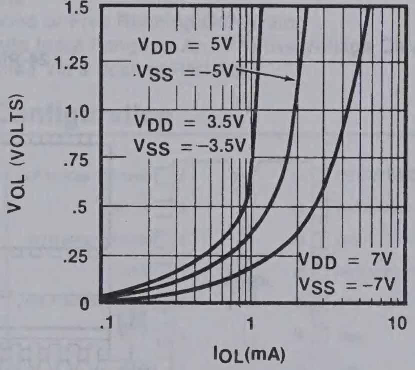
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



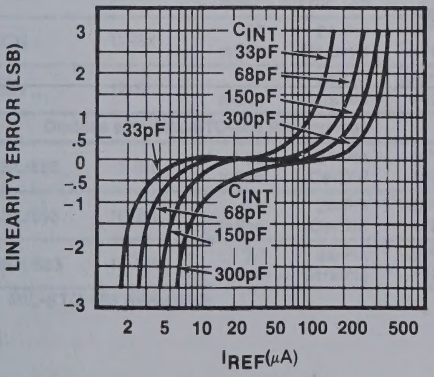
OUTPUT SINK CURRENT vs TEMPERATURE



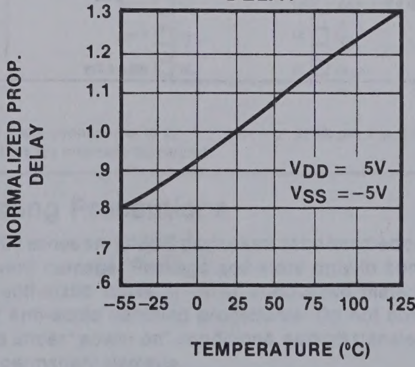
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs IREF

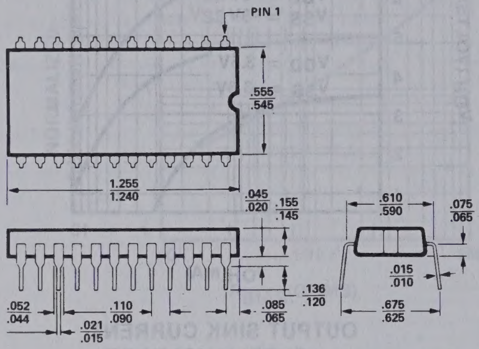


TRI-STATE PROPAGATION DELAY

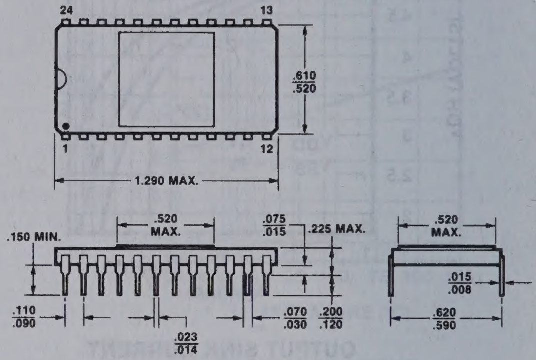


Package Information

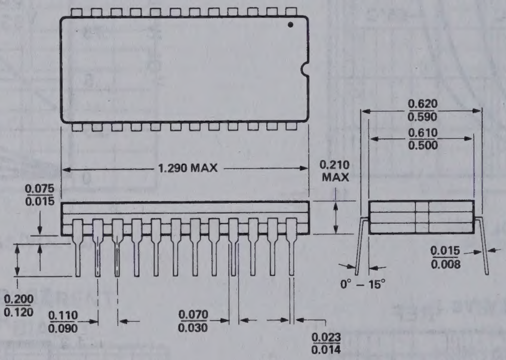
24-Pin Plastic Dip (J Package)
(Package #12)


PIN 1
.555
.545
1.255
1.240
.045
.020
.155
.145
.610
.590
.075
.065
.015
.010
.136
.120
.052
.044
.110
.090
.085
.065
.675
.625
.021
.015

24-Pin Ceramic Dip (N Package)
(Package #13)


24
13
1
12
.610
.520
1.290 MAX.
.520
MAX.
.075
.015
.225 MAX.
.150 MIN.
.520
MAX.
.015
.008
.110
.090
.070
.030
.200
.120
.620
.590
.023
.014

24-Pin CerDIP (L Package)
(Package #14)


0.620
0.590
0.610
0.500
1.290 MAX
0.210
MAX
0.075
0.015
0.015
0.008
0° – 15°
0.200
0.120
0.110
0.090
0.070
0.030
0.023
0.014

TELEDYNE SEMICONDUCTOR

TSC8703 (8-Bit)
TSC8704 (10-Bit)
TSC8705 (12-Bit)
Binary Output ADC

• Three State, Latched Outputs
• High Speed Conversion: 1-20 mSec

General Description

The TSC8703/8704/8705 are 8/10/ 12 bit monolithic CMOS analog-to-digital converters. Fully self-contained in a single 24-pin dual in-line package, each converter requires only passive support components, reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero is counted. At the end of conversion the total count is latched into the digital outputs as an 8/10/12 bit binary word. The Output Enable control switches the outputs to a high impedance or off state when held high. The off state allows bus organized output connections.

Ordering Information

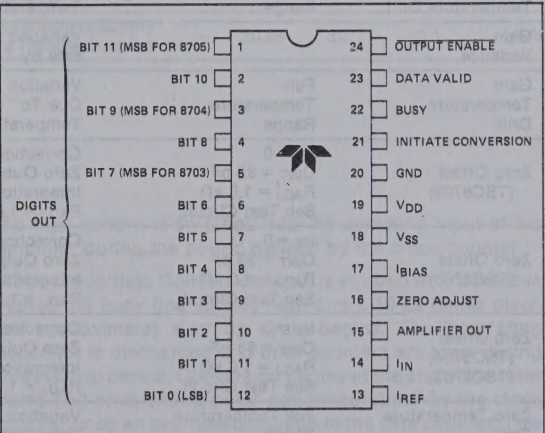
Part No.	Resolution	Conv. Time	Package	Temp. Range
TSC8703CJ	8-Bit	1.25 mSec	24-Pin Plastic Dip	0°C to +70°C
TSC8703CL	8-Bit	1.25 mSec	24-Pin CerDIP	-40°C to +85°C
TSC8703BL	8-Bit	1.25 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8704CJ	10-Bit	5.0 mSec	24-Pin Plastic Dip	0°C to +70°C
TSC8704CL	10-Bit	5.0 mSec	24-Pin CerDIP	-40°C to +85°C
TSC8704BL	10-Bit	5.0 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8705CJ	12-Bit	20 mSec	24-Pin Plastic Dip	0°C to +70°C
TSC8705CN	12-Bit	20 mSec	24-Pin Ceramic	-40°C to +85°C
TSC8705BN	12-Bit	20 mSec	24-Pin Ceramic	-55°C to +125°C
Devices with MIL-STD-883 Processing*				
TSC8703BL/883	8-Bit	1.25 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8704BL/883	10-Bit	5.0 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8705BN/883	12-Bit	20 mSec	24-Pin Ceramic	-55°C to +125°C

* Level B, MIL-STD-883 Revision B

Features

- High Accuracy — Up to 12 Bit Resolution With <±1/2 LSB Error
- Monotonic Performance — No Missing Codes
- Monolithic CMOS Construction Gives Low Power Dissipation — 20 mW Typical
- Contains All Required Active Elements — Needs only Passive Support Components, Reference Voltage and Dual Power Supply
- High Stability Over Full Temperature Range
  - — Gain Temperature Coefficient Typically <25 ppm/°C
  - — Zero Drift Typically <30 μV/°C
  - — Differential Non-Linearity Drift Typically <25 ppm/°C
- Latched Parallel Binary Outputs
- LPTTL, 74LS, CMOS Compatible Outputs and Control Inputs
- Strobed or Free Running Conversion
- Infinite Input Range — Any Positive Voltage Can Be Applied Via a Scaling Resistor

Pin Configuration



Note:
Do not make connections to pin 1, 2, 3 or 4 on 8703; pin 1 or 2 on 8704. These pins are internally connected.

Handling Precautions

The 8700 series are CMOS devices must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

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Absolute Maximum Ratings

Storage Temperature .... -65° C to + 150° C
Operating Temperature
(BL, BN) .... -55° C to +125° C
(CL) Package .... -40° C to + 85° C
(CJ) Package .... 0° to + 70° C
V_{DD} -V_{SS} .... 18 V
I_{IN} .... ±10 mA
I_{REF} .... ±10 mA
Digital Input Voltage .... -0.3 to V_{DD} +0.3 V
Operating V_{DD} and V_{SS} Range .... 3.5 V to 7 V
Package Dissipation .... 500 mW
Lead Temperature .... 300° C
(Soldering, 10 seconds)

Electrical Characteristics: Unless otherwise specified, V_{DD} = +5 V, V_{SS} = -5 V, V_{GND} = 0, V_{REF} = -6.4 V, R_{BIAS} = 100 kΩ, test circuit shown. T_A = 25° C unless Full Temperature Range is specified (-55° C to +125° C for BN and BL package, -40° C to +85° C for CL package, 0° to 70° C for CJ package).

PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	CJ/CN MAX	BN/BL MAX	UNITS
Accuracy							
Resolution Accuracy		Binary Word Length Of Digital Output					
		TSC8703	8	—	—	—	Bits
		TSC8704	10	—	—	—	Bits
		TSC8705	12	—	—	—	Bits
Relative Accuracy		Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	±1/4	±1/2	±1/2	LSB
		TSC8705CJ (Only)	—	1.0	±1.5		LSB
Differential Non-Linearity		Deviation From 1 LSB Between Transition Points	—	±1/4	±1/2	±1/2	LSB
Differential Non-Linearity Temperature Drift	Full Temperature Range	Variation in Differential Non-Linearity Due To Temperature Change	—	±2.5	±5	±5	ppm/°C
Gain Variance		Variation From Exact A (Compensate By Trimming R_{IN} or R_{REF})		±2	±5	±5	% of Nominal
Gain Temperature Drift	Full Temperature Range	Variation In A Due To Temperature Change	—	±25	±75	±80	ppm/°C
Zero Offset (TSC8703)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.6 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.6 kΩ	—	—	±80	±80	mV
Zero Offset (TSC8703)	I_{IN} = 0 C_{INT} = 33 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 33 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	±50	mV
Zero Offset (TSC8704) (TSC8705)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	±50	mV
Zero Temperature Drift	Full Temperature Range	Variation in Zero Offest Due to Temperature Change	—	±3	±5	±8	ppm/°C
Analog Inputs							
I_{IN} Full-Scale		Full-Scale Analog Input Current To Achieve Specified Accuracy	—	10	—	—	μA
I_{REF} (Note 1)		Reference Current Input To Achieve Specified Accuracy	—	-20	—	—	μA
Digital Inputs							
$V_{IN}^{(1)}$	Full Temperature Range	Logical "1" Input Threshold For Initiate Conversion Input	3.5	—	—	—	V
$V_{IN}^{(0)}$	Full Temperature Range	Logical "0" Input Threshold For Initiate Conversion Input	—	—	1.5	1.5	V
Propagation Delay							
Output Enable	C_L = 100 pF, R_L = 1 KΩ	T_{PLH}, T_{PHL}	—	500	—	1,000	ns

Electrical Characteristics (Cont.)

PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	CJ/CN MAX	BN/BL MAX	UNITS
Digital Outputs							
$I_{O(OFF)}$	OE = 3.5 V, 0.4 V < V_C <2.4	Off-state Output Current	—	0.1	±10	±10	μA
$V_{OUT}^{(1)}$	Full Temp. Range I_{OUT} = -10 μA I_{OUT} = -500 μA	Logical "1" Output Voltage For Digits Out, Busy, and Data Valid Outputs	4.5 2.4	— —	— —	— —	V V
$V_{OUT}^{(0)}$	Full Temp. Range V_{DD} = 4.75 V I_{OUT} = 500 μA	Logical "0" Output Voltage For Digits Out, Busy, and Data Valid Outputs	—	—	0.4	0.4	V
Dynamic							
Conversion Time	Full Temp. Range	Time Required to Perform One Complete A/D Conversion					
		TSC8703	—	1.25	1.8	1.8	ms
		TSC8704	—	5	6	6	ms
		TSC8705	—	20	24	24	ms
Conversion Rate in Free-Run Mode	$V_{INT\ CONV}$ = + 5 V	TSC8703 TSC8704 TSC8705	555 167 42	800 200 50	— — —	— — —	Conv'ns per Second
Minimum Pulse Width for Initiate Conversion	Full Temp. Range		500	—	—	—	ns
Supply Current							
I_{DD} Quiescent (L/N Package) (J Package)	Full Temp. Range $V_{INT\ CONV}$ = 0V	Current Required From Positive Supply During Operation	— —	1.4 1.4	2.5 5.0	3.5	mA mA
I_{SS} Quiescent (L/N Package) (J Package)	Full Temp. Range $V_{INIT\ CONV}$ = 0V	Current Required From Negative Supply During Operation	— —	-1.6 -1.6	-2.5 -5.0	-3.5	mA mA
Supply Sensitivity	V_{DD} ± 1 V, V_{SS} ±1 V	Change in Full-Scale Gain vs Supply Voltage Change	—	±0.5	±1.0	±1.0	%/V
	$\|V_{DD}\| = \|V_{SS}\|$ = 5 V ± 1 V	Change in Full-Scale Gain vs Supply Voltage Change for Tracking Supplies	—	±0.05	±0.1	±0.1	%/V

NOTE:
I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

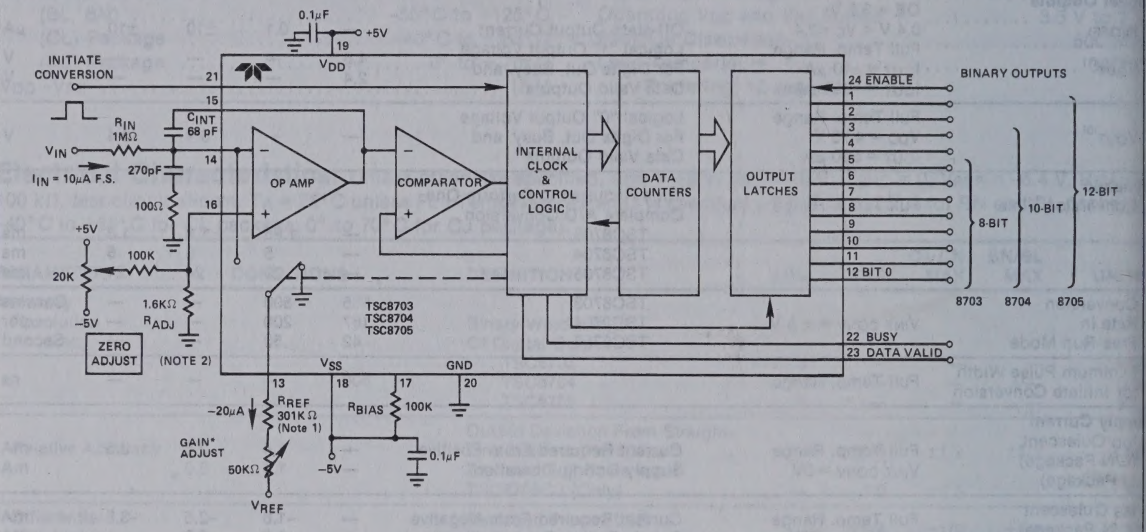
Circuit Description

During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the output of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in Binary) is latched into the outputs at the end of the conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine. The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10 μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5 μs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate Conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

Test Circuit


0.1µF
+5V
19
VDD
INITIATE CONVERSION
21
15
CINT 68 pF
RIN 1MΩ
VIN
IIN = 10µA F.S.
270pF
14
100Ω
16
OP AMP
COMPARATOR
INTERNAL CLOCK & CONTROL LOGIC
DATA COUNTERS
OUTPUT LATCHES
24 ENABLE
BINARY OUTPUTS
1
2
3
4
5
6
7
8
9
10
11
12 BIT 0
12-BIT
10-BIT
8-BIT
8703
8704
8705
22 BUSY
23 DATA VALID
+5V
20K
100K
1.6KΩ
RADJ
-5V
ZERO ADJUST
(NOTE 2)
TSC8703
TSC8704
TSC8705
VSS
GND
13
18
17
20
-20µA
RREF 301K Ω (Note 1)
RBIAS
100K
GAIN* ADJUST
50KΩ
-5V
0.1µF
VREF

Note:

1. Any V_{REF} greater than -1 V can be used.

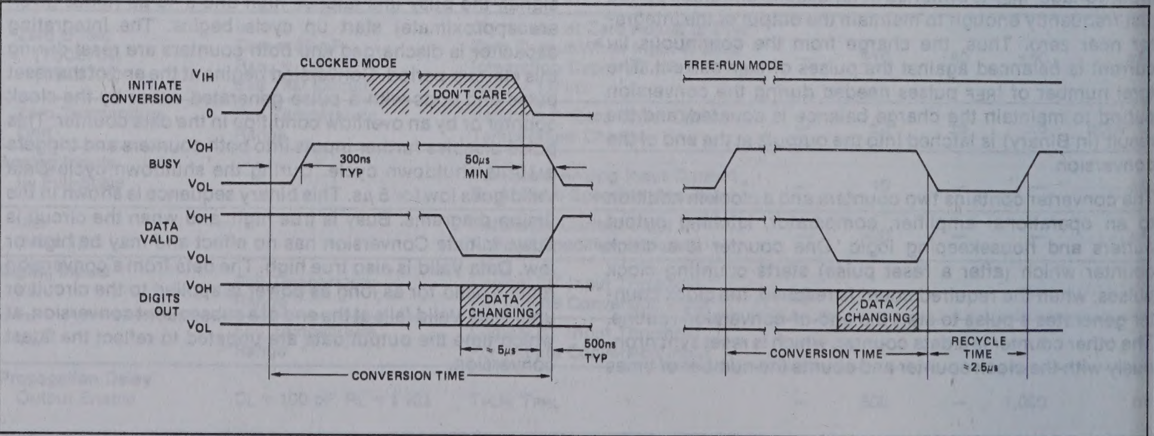
$$R_{REF} = \frac{V_{REF}}{-20\ \mu A}$$

For example with V_{REF} = -5 V, R_{REF} = 250 k.

2.

Part No.	R_{ADJ}	C_{INT}	Zero Offset Spec
TSC8703	1.6 kΩ	68 pF	±80 mV
TSC8703	1.0 kΩ	33 pF	±50 mV
TSC8704/8705	1.0 kΩ	68 pF	±50 mV

Timing Diagrams (Rise, fall times = 200 ns typ., C_L = 50 pF)


CLOCKED MODE
FREE-RUN MODE
INITIATE CONVERSION
VIH
0
DON'T CARE
BUSY
VOH
VOL
300ns TYP
50µs MIN
DATA VALID
VOH
VOL
DIGITS OUT
VOH
VOL
DATA CHANGING
≈ 5µs
500ns TYP
CONVERSION TIME
DATA CHANGING
CONVERSION TIME
RECYCLE TIME ≈2.5µs

Pin Functions

Initiate Conversion Input

Accepts CMOS and most 5 V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500 µA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5 µs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low power TTL (can sink and source 50 µA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5 µs before the completion of a conversion cycle. During this 5 µs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out

(Bit 0, Bit 1, etc.)

The binary digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

Applications Information

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital Counts} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

A = 528 for 8703
A = 2064 for 8704
A = 8208 for 8705

where Digital Counts is the value of the binary output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

Analog Input	Digital Output MSB	LSB
$V_{IN} \leq$ Full-Scale	1 . . . 111 . . .	1
= Full-Scale -1 LSB	1 . . . 111 . . .	1
= 1 LSB	0 . . . 000 . . .	1
≤ 0	0 . . . 000 . . .	0

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection

Obtaining a high accuracy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1 µF or larger right at the device pins.

R_{IN}, R_{EF}

Values of these components are chosen to give a full-scale input current of approximately 10 µA and a reference current of approximately -20 µA.

$$R_{IN} \cong \frac{V_{IN}\ \text{Full-Scale}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}$$

Examples:

$$R_{IN} \cong \frac{10\ V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4\ V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} full-scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS}

Specifications for the 87XX are based on R_{BIAS} = 100 kΩ ±10% unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20 k the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When R_{BIAS} = 1 mΩ the conversion time will be six times longer, and supply current is now reduced to .5 mA). For details of this relationship refer to AN9 typical performance curves.

Applications Information (Cont.)

R_{DAMP}

Exact value not critical but should have a nominal value of 100 Ω ±10%. Locate close to pin 14.

C_{DAMP}

Exact value not critical but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT}

Exact value not critical but should have a nominal value of 68 pF ± 10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15. For the TSC8703 $C_{INT} = 33$ pF is adequate with $R_{ADJ} = 1$ kΩ.

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of ±5 V are recommended, with 0.05% line and load regulation and 0.1 μF decoupling capacitors.

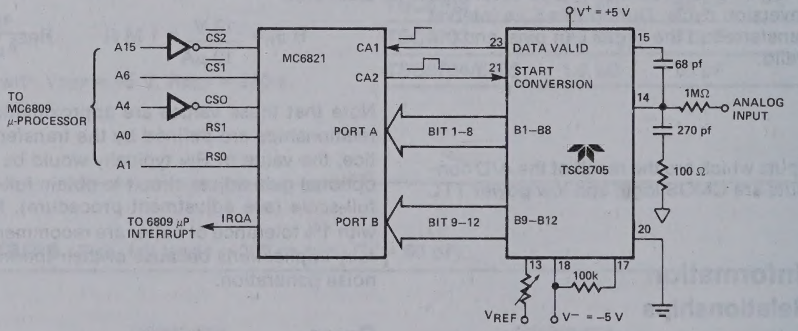
Adjustment Procedure

The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full-scale), it is recommended that transition points be used in setting the zero and full-scale values. Recommended procedure is as follows:

- Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
- Set V_{IN} to +1/2 LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
- For full-scale adjustment, set V_{IN} to the full-scale value less 1 1/2 LSB and trim the gain adjust circuit for a 111 . . . 110 to 111 . . . 111 transition.

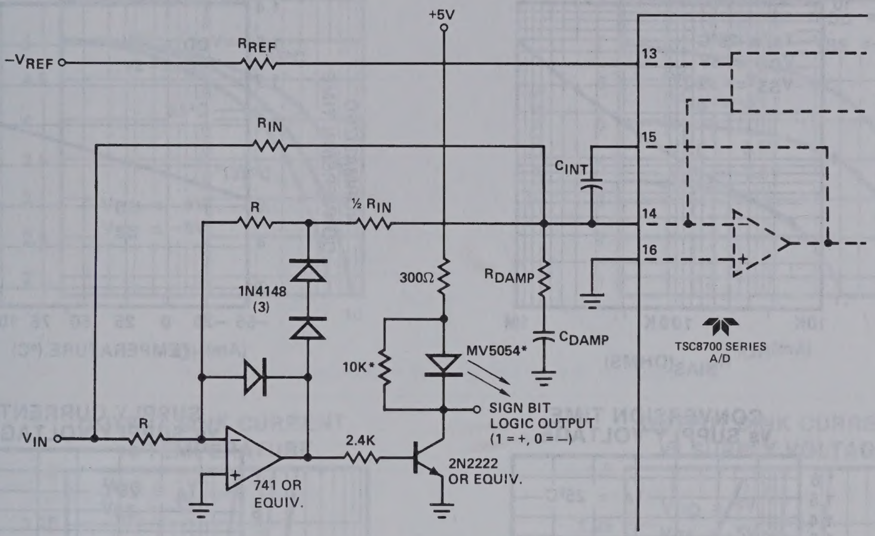
If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

TSC8705 Interface to MC6821 PIA


A15
A6
A4
A0
A1
TO
MC6809
μ-PROCESSOR
$\overline{CS2}$
$\overline{CS1}$
CSO
RS1
RS0
MC6821
CA1
CA2
PORT A
PORT B
IRQA
TO 6809 μP
INTERRUPT
BIT 1–8
BIT 9–12
V+ = +5 V
23
21
DATA VALID
START
CONVERSION
B1–B8
B9–B12
TSC8705
15
14
20
13
18
17
68 pf
1MΩ
ANALOG
INPUT
270 pf
100 Ω
100k
VREF
V− = −5 V

Application/Design Circuits

Bipolar Operation (+ and –Inputs)

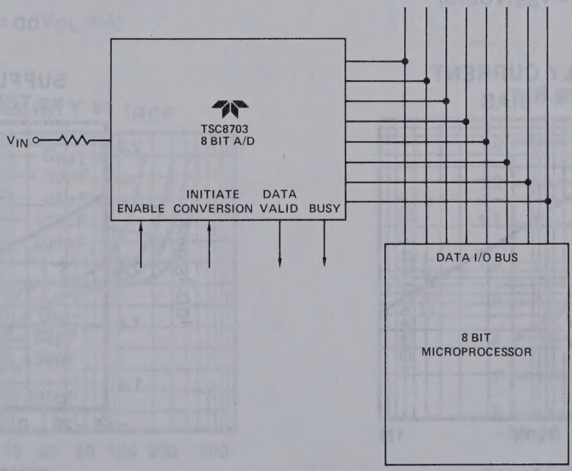

+5V
$-V_{REF}$
R_{REF}
R_{IN}
R
½ R_{IN}
C_{INT}
13
15
14
16
300Ω
R_{DAMP}
1N4148
(3)
C_{DAMP}
MV5054*
10K*
SIGN BIT
LOGIC OUTPUT
(1 = +, 0 = –)
V_{IN}
R
2.4K
2N2222
OR EQUIV.
741 OR
EQUIV.
TSC8700 SERIES
A/D

*Optional visual indication of negative input

NOTE: Values for R should be between 10KΩ and 100KΩ

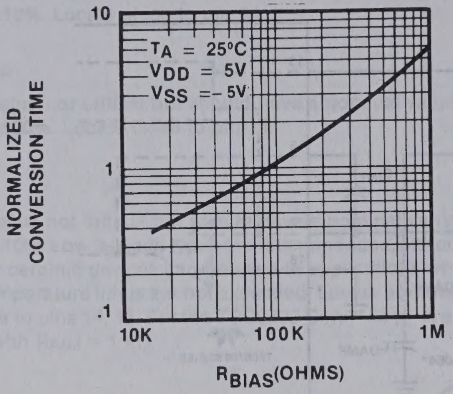
Absolute Value Circuit With Sign

8-Bit Microprocessor Interface

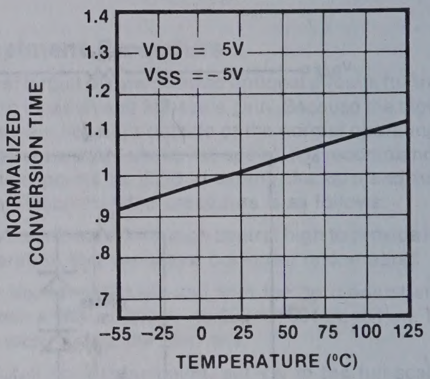

V_{IN}
TSC8703
8 BIT A/D
ENABLE
INITIATE
CONVERSION
DATA
VALID
BUSY
DATA I/O BUS
8 BIT
MICROPROCESSOR

TYPICAL PERFORMANCE CURVES

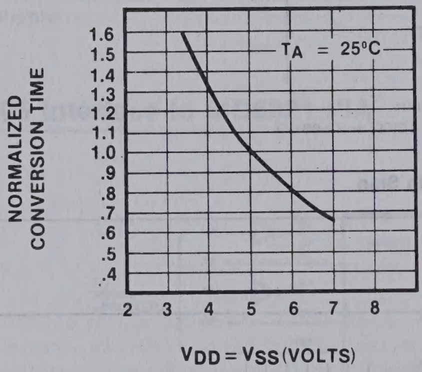
CONVERSION TIME vs R_{BIAS}



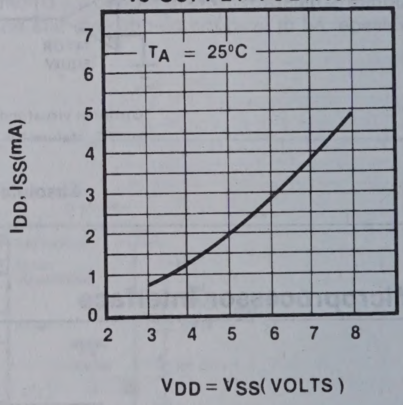
CONVERSION TIME vs TEMPERATURE



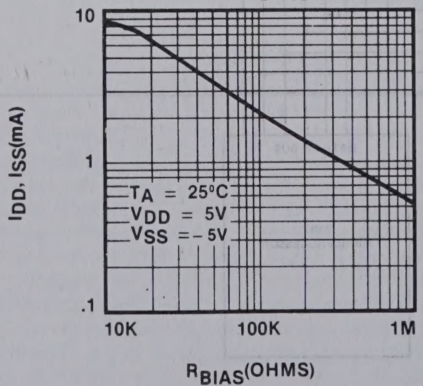
CONVERSION TIME vs SUPPLY VOLTAGE



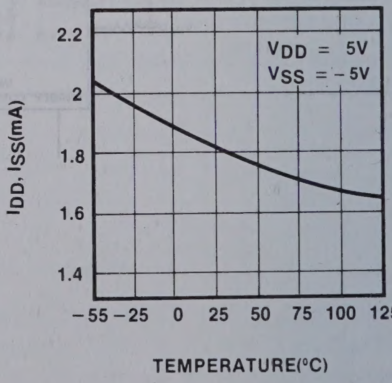
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs R_{BIAS}

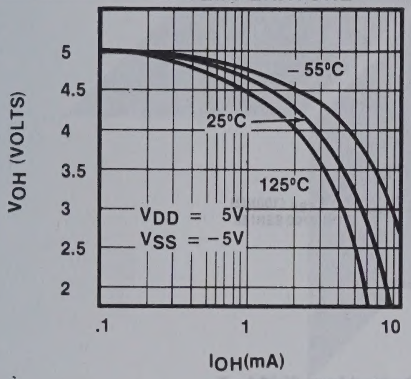


SUPPLY CURRENT vs TEMPERATURE

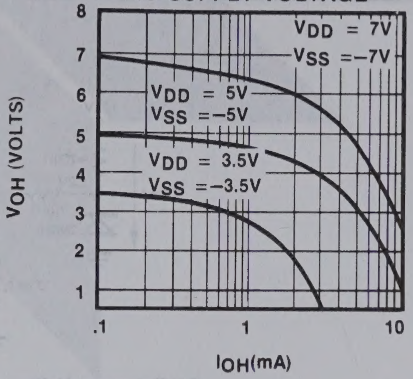


TYPICAL PERFORMANCE CURVES

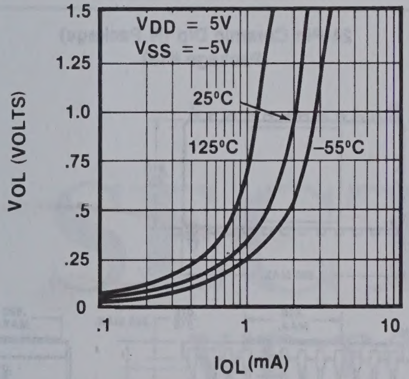
OUTPUT SOURCE CURRENT vs TEMPERATURE



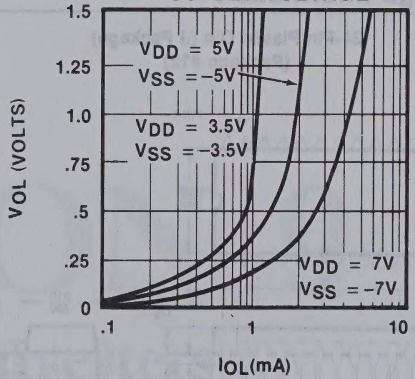
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



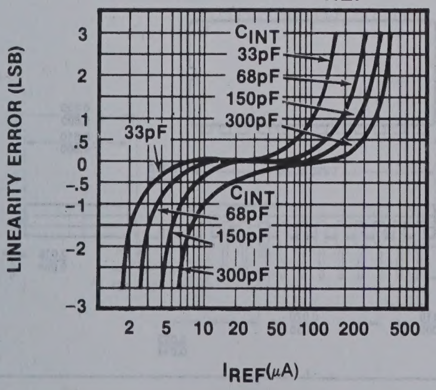
OUTPUT SINK CURRENT vs TEMPERATURE



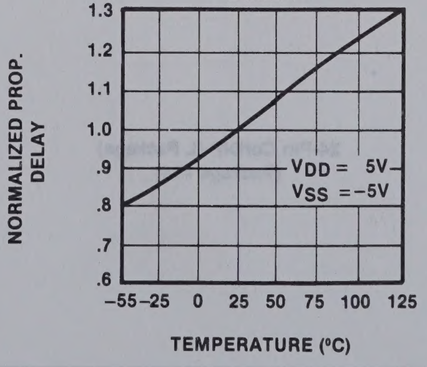
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs IREF

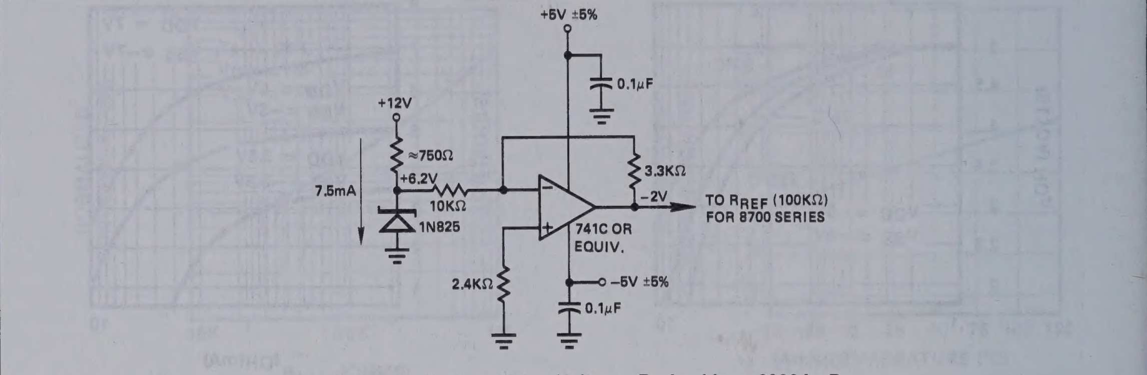


TRI-STATE PROPAGATION DELAY



Application/Design Circuits (Cont.)

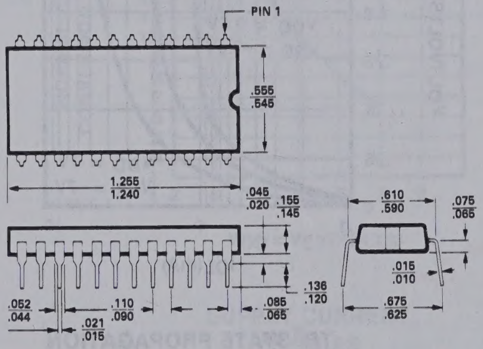
Reference Voltage Supply


+5V ±5%
0.1µF
+12V
≈750Ω
+6.2V
7.5mA
10KΩ
1N825
3.3KΩ
–2V
TO R_REF (100KΩ)
FOR 8700 SERIES
741C OR
EQUIV.
2.4KΩ
–5V ±5%
0.1µF

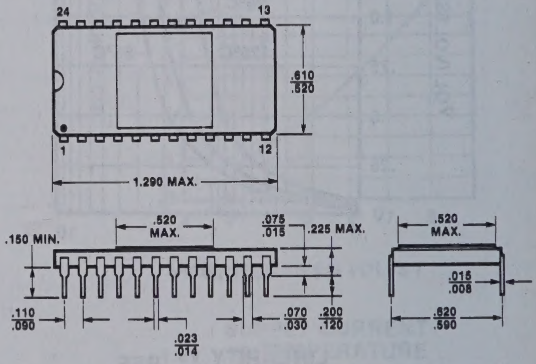
2 V Reference Voltage Using Voltages Derived from 8080A µP.

Package Information

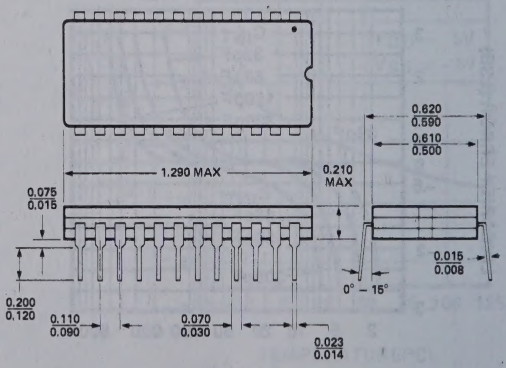
24-Pin Plastic Dip (J Package)
(Package #12)


PIN 1
.555
.545
1.255
1.240
.045
.020
.155
.145
.610
.590
.075
.065
.015
.010
.136
.120
.052
.044
.110
.090
.085
.065
.021
.015
.675
.625

24-Pin Ceramic Dip (N Package)
(Package #13)


24
13
.610
.520
1
12
1.290 MAX.
.520
MAX.
.075
.015
.225 MAX.
.520
MAX.
.150 MIN.
.015
.008
.110
.090
.070
.030
.200
.120
.620
.590
.023
.014

24-Pin CerDIP (L Package)
(Package #14)


0.620
0.590
0.610
0.500
1.290 MAX
0.210
MAX
0.075
0.015
0.015
0.008
0° – 15°
0.200
0.120
0.110
0.090
0.070
0.030
0.023
0.014

SECTION 9

V/F, F/V Converters

Section 9

Voltage to Frequency/Frequency to Voltage Converters 9-3
TSC9400 Voltage to Frequency (0.05% Linearity) 9-5
TSC9401 Voltage to Frequency (0.01% Linearity) 9-5
TSC9402 Voltage to Frequency (0.25% Linearity) 9-5

TELEDYNE SEMICONDUCTOR

TSC9400 (0.05%)
TSC9401 (0.01%)
TSC9402 (0.25%)
Voltage to Frequency/ Frequency to Voltage Converters

General Description

The TSC9400/9401/9402 are low cost Voltage-to-Frequency converters combining Bipolar and CMOS technology on the same substrate. The converters accept a variable analog nput signal and generate an output pulse train whose frequency is linearly proportional to the input voltage.

The devices can also be used as highly accurate Frequency-to-Voltage converters, accepting virtually any input frequency waveform and providing a linearly proportional voltage output.

A complete V/F or F/V system requires the addition of two capacitors, three resistors and reference voltage.

Applications

Voltage-to-Frequency

- Temperature Sensing and Control
- µP Data Acquisition
- Instrumentation
- 13-Bit A/D Converters
- Digital Panel Meters
- Analog Data Transmission and Recording
- Phase Locked Loops
- Medical Isolation
- Transducer Encoding
- Alternate to 555 Astable Timer

Frequency-to-Voltage

- Frequency Meters/Tachometer
- Speedometers
- Analog Data Transmission and Recording
- Medical Isolation
- Motor Control
- RPM Indicator
- FM Demodulation
- Frequency Multiplier/Divider
- Flow Measurement and Control

Ordering Information

Part No.	Linearity (V/F)	Package	Temperature Range
TSC9400CJ	0.05%	14-Pin Plastic Dip	0° C to +70° C
TSC9400CL	0.05%	14-Pin CerDIP	-40° C to +85° C
TSC9401CJ	0.01%	14-Pin Plastic Dip	0° C to +70° C
TSC9401CL	0.01%	14-Pin CerDIP	-40° C to +85° C
TSC9402CJ	0.25%	14-Pin Plastic Dip	0° C to +70° C
TSC9402CL	0.25%	14-Pin CerDIP	-40° C to +85° C

Features

Voltage-to-Frequency

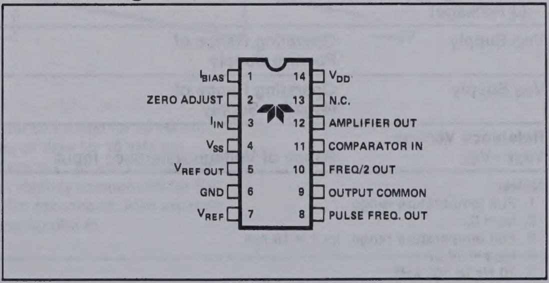
- 1 Hz to 100 kHz Operation
- Choice Guaranteed Linearity:
  - — TSC9401 0.01%
  - — TSC9400 0.05%
  - — TSC9402 0.25%
- ±25 ppm/° C Typical Gain Temperature Stability
- Open Collector Output
- Output Can Interface with Any Form of Logic
- Pulse and Square Wave Outputs
- Programmable Scale Factor
- Low Power Dissipation (27 mW Typ.)
- Single Supply Operation (8 V to 15 V)
- Dual Supply Operation (±4 V to ±7.5 V)
- Current or Voltage Input

Frequency-to-Voltage

- DC to 100 kHz Operation
- Choice of Guaranteed Linearity:
  - — TSC9401 0.02%
  - — TSC9400 0.05%
  - — TSC9402 0.25%
- Op Amp Output
- Programmable Scale Factor
- High Input Impedance (>10 MΩ)
- Accepts any Voltage Wave Shape

HANDLING PRECAUTIONS: The TSC9400 Series are CMOS Bipolar devices and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other ocnductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

Pin Configuration



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TSC9400 (0.05%)
TSC9401 (0.01%)
TSC9402 (0.25%)

Voltage to Frequency/ Frequency to Voltage Converters

Absolute Maximum Ratings

Storage Temperature	-65° C to +150° C
Operating Temperature	
J Package	0° C to 70° C
L Package	-40° C to +85° C
V_{DD} -V_{SS}	18 V
I_{IN}	10 mA
V_{OUT} Max -V_{OUT} Common	25 V
V_{REF} -V_{SS}	-1.5 V
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 sec)	300° C

Electrical Characteristics, V/F Mode:

Unless otherwise specified, V_{DD} = +5 V, V_{SS} = -5 V, V_{GND} = 0, V_{REF} = -5 V, R_{BIAS} = 100 kΩ, Full-Scale = 10 kHz. T_A = 25° C unless Full Temperature Range is specified -40° C to +85° C for L package, 0° C to 70° C for J package.

VOLTAGE-TO-FREQUENCY PARAMETER	DEFINITION	TSC9401 MIN	TSC9401 TYP	TSC9401 MAX	TSC9400 MIN	TSC9400 TYP	TSC9400 MAX	TSC9402 MIN	TSC9402 TYP	TSC9402 MAX	UNITS
Accuracy Linearity 10 kHz	Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	0.004	0.01	—	0.01	0.05	—	0.05	0.25	% Full-Scale
Linearity 100 kHz		—	0.04	0.08	—	0.1	0.25	—	0.25	0.50	% Full-Scale
Gain Temperature Drift (Note 1)	Variation in Gain A due to Temperature Change	—	±25	±40	—	±25	±40	—	±50	±100	ppm/° C Full-Scale
Gain Variance	Variation from Exact A Compensate by Trimming R_{IN}, V_{REF}, or C_{REF}	—	±10	—	—	±10	—	—	±10	—	% of Nominal
Zero Offset (Note 2)	Correction at Zero Adjust for Zero Output When Input is Zero	—	±10	±50	—	±10	±50	—	±20	±100	mV
Zero Temperature Drift (Note 1)	Variation in Zero Offset Due to Temperature Change	—	±25	±50	—	±25	±50	—	±50	±100	µV/° C
Analog Inputs I_{IN} Full-Scale	Full-Scale Analog Input Current to Achieve Specified Accuracy	—	10	—	—	10	—	—	10	—	µA
I_{IN} Overrange	Overrange Current	—	—	50	—	—	50	—	—	50	µA
Response Time	Settling Time to 0.01% Full-Scale	—	2	—	—	2	—	—	2	—	Cycles
Digital Outputs V_{SAT} @ I_{OL} = 10 µA (Note 3)	Logical "0" Output Voltage	—	—	0.4	—	—	0.4	—	—	0.4	V
V_{OUT} Max — V_{OUT} Common (Note 4)	Voltage Range Between Output and Common	—	—	18.0	—	—	18.0	—	—	18.0	V
Pulse Frequency Output Width		—	3.0	—	—	3.0	—	—	3.0	—	µsec
Supply Current I_{DD} Quiescent (L Package) (Note 9)	Current Required From Positive Supply During Operation	—	2.0	4.0	—	2.0	4.0	—	—	—	mA
(J Package)		—	2.0	6.0	—	2.0	6.0	—	3.0	10.0	mA
I_{SS} Quiescent (L Package) (Note 10)	Current Required From Negative Supply During Operation	—	-1.5	-4.0	—	-1.5	-4.0	—	—	—	mA
(J Package)		—	-1.5	-6.0	—	-1.5	-6.0	—	-3.0	-10.0	mA
V_{DD} Supply	Operating Range of Positive Supply	4.0	—	7.5	4.0	—	7.5	4.0	—	7.5	V
V_{SS} Supply	Operating Range of Negative Supply	-4.0	—	-7.5	-4.0	—	-7.5	-4.0	—	-7.5	V
Reference Voltage V_{REF} -V_{SS}	Range of Voltage Reference Input	-1.0	—	—	-1.0	—	—	-1.0	—	—	V

Notes:

1. Full temperature range
2. I_{IN} = 0.
3. Full temperature range. I_{OUT} = 10 mA.
4. I_{OUT} = 10 µA
5. 10 Hz to 100 kHz.
6. 5 µs min. positive pulse width and 0.5 µs min. negative pulse width.
7. $T_r = t_f$ = 20 ns.
8. $R_L \geq 2$ kΩ.
9. Full temperature range. V_{IN} = -0.1 V.
10. V_{IN} = -0.1 V.
11. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors.

V/F Circuit Description

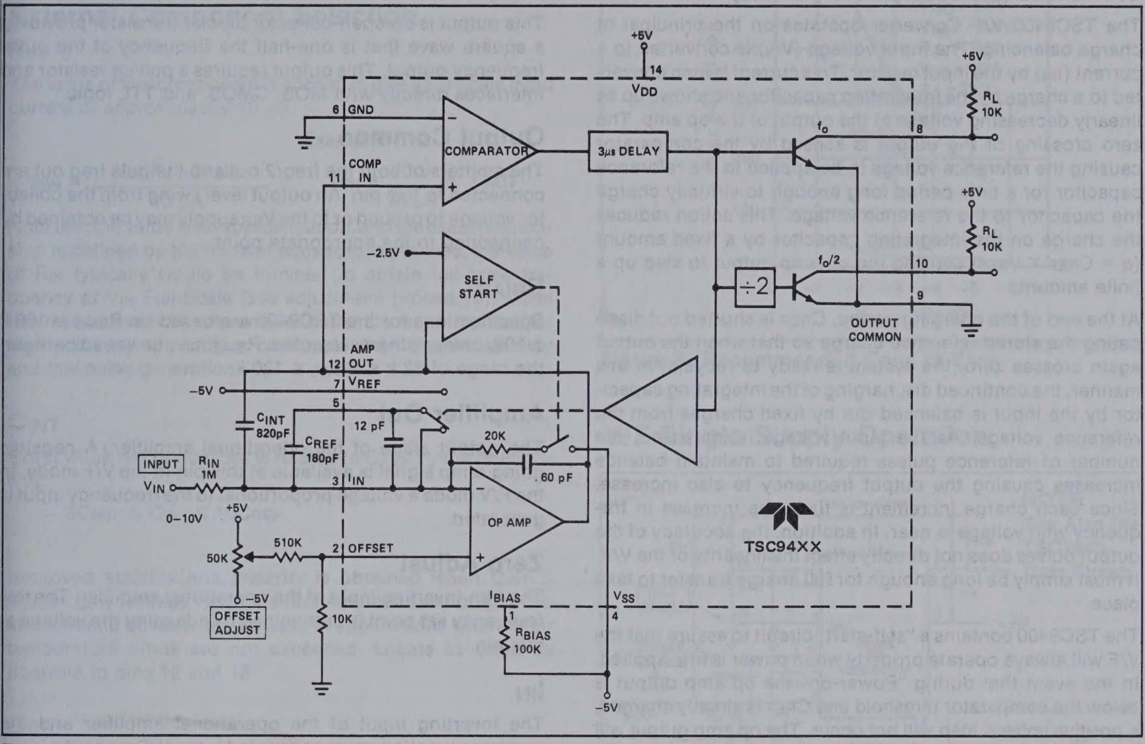
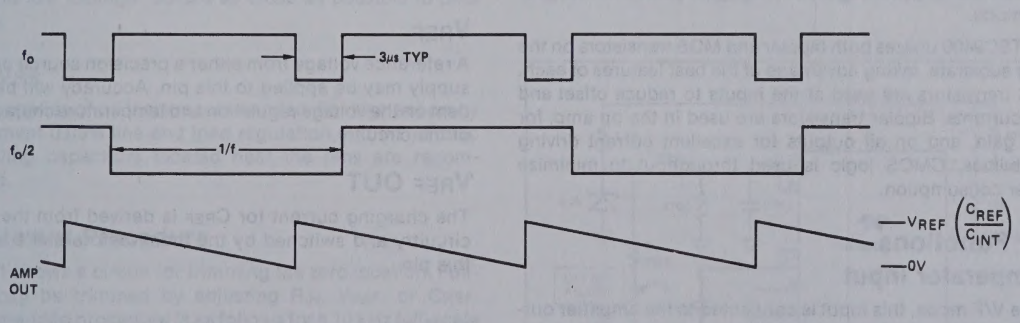

+5V
14
VDD
+5V
RL
10K
6 GND
fo
8
COMPARATOR
3µs DELAY
COMP
11 IN
+5V
RL
10K
−2.5V
fo/2
10
÷2
SELF
START
9
OUTPUT
COMMON
AMP
12 OUT
7 VREF
−5V
5
CINT
820pF
12 pF
CREF
180pF
20K
INPUT
RIN
1M
VIN
3 IIN
.60 pF
+5V
0–10V
OP AMP
TSC94XX
510K
50K
2 OFFSET
−5V
OFFSET
ADJUST
IBIAS
1
VSS
4
10K
RBIAS
100K
−5V

Figure 1: 10 Hz to 10 kHz V/F Converter


fo
3µs TYP
fo/2
1/f
AMP
OUT
VREF (CREF/CINT)
0V

Notes:

1. To adjust f_{min}, set V_{IN} = 10 mV and adjust the 50 k offset for 10 Hz out.
2. To adjust f_{max}, set V_{IN} = 10 V and adjust R_{IN} or V_{REF} for 10 kHz out.
3. To increase f_{OUT} MAX to 100 kHz change C_{REF} to 27 pF and C_{INT} to 75 pF.
4. For high performance applications use high stability components for R_{IN}, C_{REF}, V_{REF} (metal film resistors and glass film capacitors). Also separate the output ground (Pin 9) from the input ground (Pin 6).

Figure 2: Output Waveforms

V/F Circuit Description (Cont.)

The TSC9400 V/F Converter operates on the principal of charge balancing. The input voltage (V_{IN}) is converted to a current (I_{IN}) by the input resistor. This current is then converted to a charge by the integrating capacitor and shows up as linearly decreasing voltage at the output of the op amp. The zero crossing of the output is sensed by the comparator causing the reference voltage to be applied to the reference capacitor for a time period long enough to virtually charge the capacitor to the reference voltage. This action reduces the charge on the integrating capacitor by a fixed amount ($q = C_{REF} \times V_{REF}$) causing the op amp output to step up a finite amount.

At the end of the charging period, C_{REF} is shorted out dissipating the stored reference charge so that when the output again crosses zero, the system is ready to recycle. In this manner, the continued discharging of the integrating capacitor by the input is balanced out by fixed charges from the reference voltage. As the input voltage is increased, the number of reference pulses required to maintain balance increases causing the output frequency to also increase. Since each charge increment is fixed the increase in frequency with voltage is near. In addition, the accuracy of the output pulses does not directly effect the linearity of the V/F. It must simply be long enough for full charge transfer to take place.

The TSC9400 contains a "self-start" circuit to assure that the V/F will always operate properly when power is first applied. In the event that during "Power-on" the op amp output is below the comparator threshold and C_{REF} is already charged, a positive voltage step will not occur. The op amp output will continue to decrease until it crosses the -2.5 volt threshold of the "self-start" comparator. When this happens a resistor is connected to the op amp input causing the output to quickly go positive until the TSC9400 is once again in its normal operating mode.

The TSC9400 utilizes both bipolar and MOS transistors on the same substrate, taking advantage of the best features of each. MOS transistors are used at the inputs to reduce offset and bias currents. Bipolar transistors are used in the op amp, for high gain, and on all outputs for excellent current driving capabilities, CMOS logic is used throughout to minimize power consumption.

Pin Functions

Comparator Input

In the V/F mode, this input is connected to the amplifier output (Pin 12) and triggers the 3 μsec pulse delay when the input voltage passes its threshold. In the F/V mode, the input frequency is applied to the comparator input.

Pulse Freq Out

This output is an open-collector bipolar transistor providing a pulse wafeform whose frequency is proportional to the input voltage. This output requires a pull up resistor and interfaces directly with MOS, CMOS and TTL logic.

Freq/2 Out

This output is an open-collector bipolar transistor providing a square wave that is one-half the frequency of the pulse frequency output. This output requires a pull up resistor and interfaces directly with MOS, CMOS, and TTL logic.

Output Common

The emitters of both the freq/2 out and the puls freq out are connected to this pin. An output level swing from the collector voltage to ground or to the V_{SS} supply may be obtained by connecting to the appropriate point.

R_{BIAS}

Specifications for the TSC9400 are based on $R_{BIAS} = 100$ k ± 10% unless otherwise noted. R_{BIAS} may be varied between the range of $82\text{ k} \leq R_{BIAS} \leq 120\text{ k}$.

Amplifier Out

The output stage of the operational amplifier. A negative going ramp signal is available at this pin in the V/F mode. In the F/V mode a voltage proportional to the frequency input is generated.

Zero Adjust

The non-inverting input of the operational amplifier. The low frequency set point is determined by adjusting the voltage at this pin.

I_{IN}

The inverting input of the operational amplifier and the summing junction when connected in the V/F mode. An input current of 10 μA is specified for nominal full-scale but an overrange current up to 50 μA can be used without detrimental effect to the circuit operation.

V_{REF}

A reference voltage from either a precision source or the V_{SS} supply may be applied to this pin. Accuracy will be dependent on the voltage regulation and temperature characteristics of the circuitry.

V_{REF} OUT

The charging current for C_{REF} is derived from the internal circuitry and switched by the break-before-make switch to this pin.

V/F Design Information

Input/Output Relationships

The output frequency is related to the analog input voltage (V_{IN}) by the transfer equation:

$$\text{Frequency Out} = \frac{V_{IN}}{R_{IN}} \times \frac{1}{(V_{REF})\ (C_{REF})} = f_o$$

V/F Design Information (Cont.)

External Component Selection

R_{IN}

The value of this component is chosen to give a full-scale input current of approximately 10 μA.

Example:

$$R_{IN} \cong \frac{V_{IN}\ \text{Full-Scale}}{10\ \mu A} \qquad R_{IN} \cong \frac{10\ V}{10\ \mu A} = 1\ M\Omega$$

Note that the value is an approximation, and the exact relationship is defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed to obtain full-scale frequency at V_{IN} Full-Scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

C_{INT}

Exact value not critical but is related to C_{REF} by the relationship:

$$3C_{REF} \le C_{INT} \le 10C_{REF}$$

Improved stability and linearity is obtained when $C_{INT} \le 4C_{REF}$. Low leakage types are recommended although mica and ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 12 and 13.

C_{REF}

Exact value not critical and may be used to trim the full-scale frequency (See input/output relation). Glass film or air trimmer capacitors are recommended because of their stability and low leakage. Locate as close as possible to pins 5 and 3.

V_{DD}, V_{SS}

Power supplies of ±5 V are recommended. For high accuracy requirement 0.05% line and load regulation and 0.1 μF disc decoupling capacitors located near the pins are recommended.

Adjustment Procedure

Figure 1 shows a circuit for trimming the zero location. Full-scale may be trimmed by adjusting R_{IN}, V_{REF}, or C_{REF}. Recommended procedure is as follows for a 10 kHz full-scale frequency.

1. Set V_{IN} to 10 mV and trim the zero adjust circuit to obtain a 10 Hz output frequency.
2. Set V_{IN} to 10.000 V and trim either R_{IN}, V_{REF}, or C_{REF} to obtain a 10 kHz output frequency.

If adjustjments are performed in this order, there should be no interaction and they should not have to be repeated.

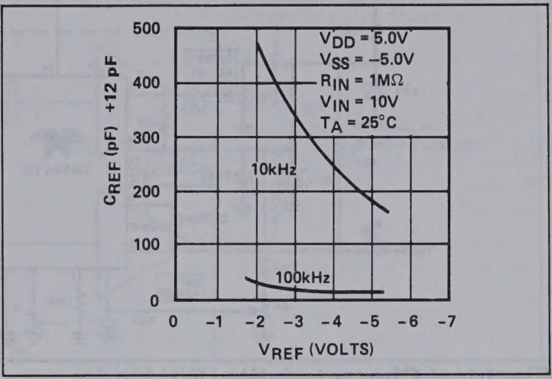
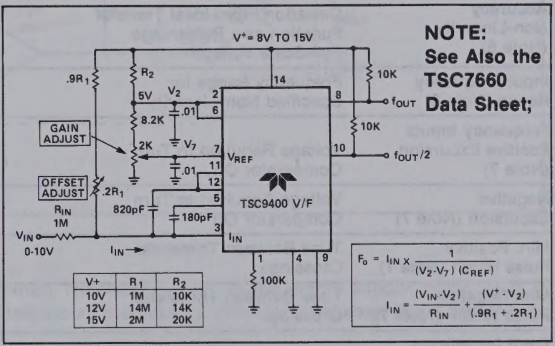


Figure 3: Recommended C_{REF} vs V_{REF}

V/F Single Supply Operation


V+= 8V TO 15V
.9R1
R2
5V
V2
.01
8.2K
GAIN ADJUST
2K
V7
.01
OFFSET ADJUST
.2R1
RIN 1M
820pF
180pF
VIN 0-10V
IIN
14
2
6
7
11
12
5
3
VREF
IIN
TSC9400 V/F
10K
8
fOUT
10K
10
fOUT/2
1
4
9
100K
V+ | R1 | R2
10V | 1M | 10K
12V | 14M | 14K
15V | 2M | 20K
F₀ = IIN x 1 / ((V2-V7) (CREF))
IIN = (VIN-V2)/RIN + (V+-V2)/(.9R1 + .2R1)

NOTE: See Also the TSC7660 Data Sheet;

Figure 4: Fixed Voltage — Single Supply Operation

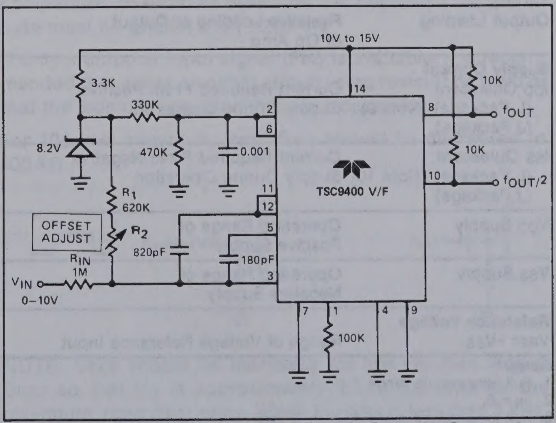
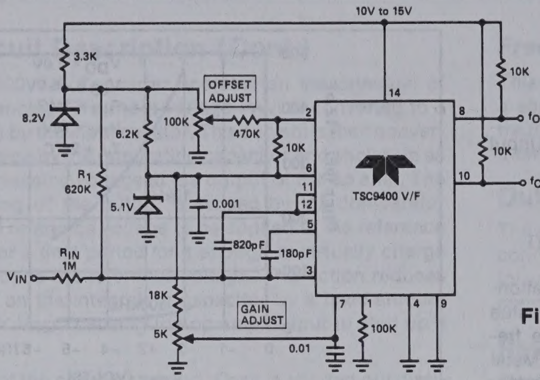

10V to 15V
3.3K
330K
8.2V
470K
0.001
R1 620K
OFFSET ADJUST
R2
820pF
180pF
RIN 1M
VIN 0–10V
14
2
6
11
12
5
3
TSC9400 V/F
10K
8
fOUT
10K
10
fOUT/2
7
1
4
9
100K

Figure 5: Variable Voltage — Single Supply Operation

Voltage to Frequency/ Frequency to Voltage Converters



See TSC7660 Data Sheet for ±5 V Operating Circuit from Single +5 V Supply.

Figure 6: Single Variable Supply Voltage with Offset and Gain Adjust

Electrical Characteristics, F/V Mode:

Unless otherwise specified, $V_{DD} = +5$ V, $V_{SS} = -5$ V, $V_{GND} = 0$, $V_{REF} = -5$ V, $R_{BIAS} = 100$ kΩ, Full-Scale = 10 kHz. $T_A = 25°$ C unless Full Temperature Range is specified -40° C to +85° C for L package, 0° C to 70° C for J package.

FREQUENCY-TO-VOLTAGE PARAMETER	DEFINITION	TSC9401			TSC9400			TSC9402			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Accuracy Non-Linearity (Note 5)	Deviation From Ideal Transfer Function as a Percentage Full-Scale Voltage	—	0.01	0.02	—	0.02	0.05	—	0.05	0.25	% Full-Scale
Input Frequency Range (Note 6)	Frequency Range for Specified Non-Linearity	10	—	100 k	10	—	100 k	10	—	100 k	Hz
Frequency Inputs Positive Excursion (Note 7)	Voltage Required to Turn Comparator On	0.4	—	V_{DD}	0.4	—	V_{DD}	0.4	—	V_{DD}	V
Negative Excursion (Note 7)	Voltage Required to Turn Comparator Off	-0.4	—	-2	-0.4	—	-2	-0.4	—	-2	V
Min. Positive Pulse Width (Note 7)	Time Between Threshold Crossings	—	5.0	—	—	5.0	—	—	5.0	—	µs
Min. Negative Pulse Width (Note 7)	Time Between Threshold Crossings	—	0.5	—	—	0.5	—	—	0.5	—	µs
Input Impedance		10	—	—	10	—	—	10	—	—	MΩ
Analog Outputs Output voltage (Note 8)	Voltage Range of Op Amp Output for Specified Non-Linearity	—V_{DD}-1		—	—V_{DD}-1		—	—V_{DD}-1		—	V
Output Loading	Resistive Loading at Output of Op Amp	2 k	—	—	2 k	—	—	2 k	—	—	Ω
Supply Current I_{DD} Quiescent (L Package) (Note 9) (J Package)	Current Required From Positive Supply During Operation	— —	2.0 2.0	4.0 6.0	— —	2.0 2.0	4.0 6.0	— —	— 3.0	— 10.0	mA mA
I_{SS} Quiescent (L Package) (Note 10) (J Package)	Current Required From Negative Supply During Operation	— —	-1.5 -1.5	-4.0 -6.0	— —	-1.5 -1.5	-4.0 -6.0	— —	— -3.0	— -10.0	mA mA
V_{DD} Supply	Operating Range of Positive Supply	4.0	—	7.5	4.0	—	7.5	4.0	—	7.5	V
V_{SS} Supply	Operating Range of Negative Supply	-4.0	—	-7.5	-4.0	—	-7.5	-4.0	—	-7.5	V
Reference Voltage $V_{REF} - V_{SS}$	Range of Voltage Reference Input	-1.0	—	—	-1.0	—	—	-1.0	—	—	V

Notes:

1. Full temperature range
2. $I_{IN} = 0$.
3. Full temperature range. $I_{OUT} = 10$ mA.
4. $I_{OUT} = 10$ µA
5. 10 Hz to 100 kHz.
6. 5 µs min. positive pulse width and 0.5 µs min. negative pulse width.
7. $T_r = t_f = 20$ ns.
8. $R_L \geq 2$ kΩ.
9. Full temperature range. $V_{IN} = -0.1$ V.
10. $V_{IN} = -0.1$ V.
11. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors.

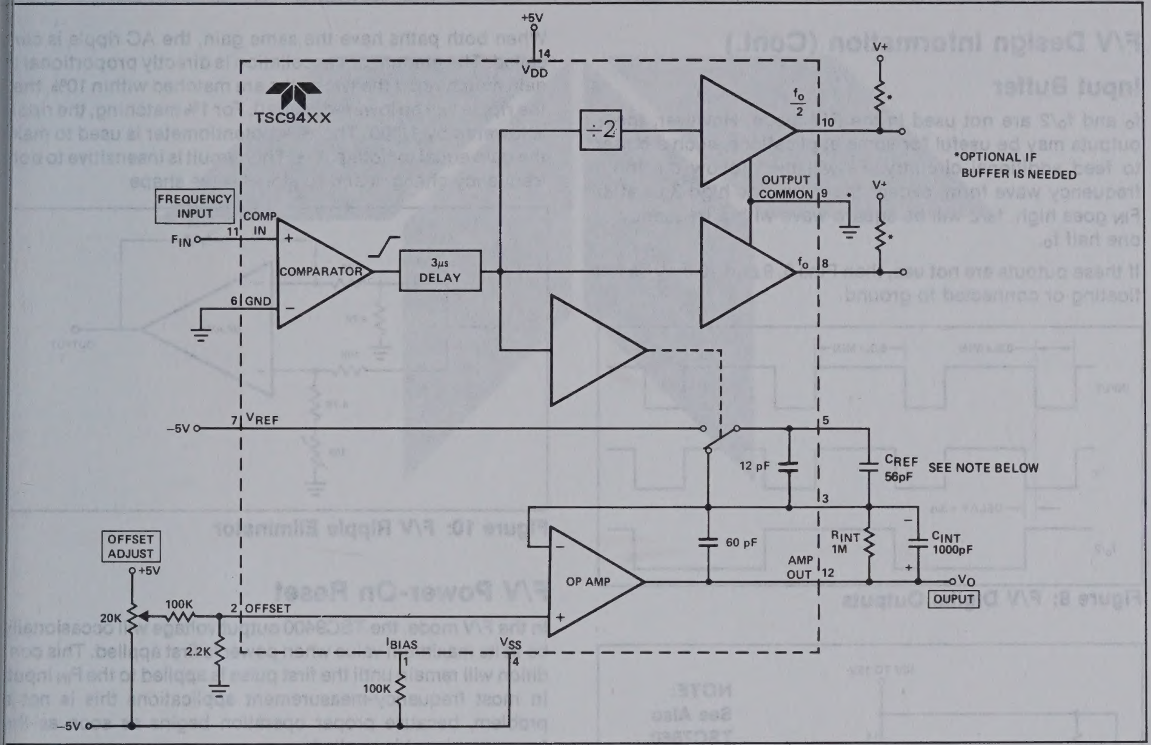

+5V
14
VDD
TSC94XX
÷2
$\frac{f_o}{2}$
10
V+
*OPTIONAL IF
BUFFER IS NEEDED
OUTPUT
COMMON
9
V+
FREQUENCY
INPUT
FIN
11
COMP
IN
COMPARATOR
3μs
DELAY
f_o
8
6
GND
−5V
7
VREF
5
12 pF
CREF
56pF
SEE NOTE BELOW
3
60 pF
RINT
1M
CINT
1000pF
AMP
OUT
12
VO
OUPUT
OP AMP
OFFSET
ADJUST
+5V
20K
100K
2
OFFSET
2.2K
IBIAS
1
100K
VSS
4
−5V

Figure 7: DC — 10 kHz F/V Converter

F/V Circuit Description

The TSC9400, when used as a frequency to voltage converter, generates an output voltage which is linearly proportional to the input frequency wave form.

Each zero crossing at the comparator's input causes a precise amount of charge ($q = C_{REF} \times V_{REF}$) to be dispensed into the op amp's summing junction. This charge in turn flows through the feedback resistor generating voltage pulses at the output of the op amp. A capacitor (C_{INT}) across R_{INT} averages these pulses into a DC voltage which is linearly proportional to the input frequency.

F/V Design Information

Input/Output Relationships

The output voltage is related to the input frequency (F_{IN}) by the transfer equation:

$$V_{OUT} = \left[V_{REF} C_{REF} R_{INT} \right] F_{IN}$$

The response time to a change in F_{IN} is equal to ($R_{INT} C_{INT}$). The amount of ripple on V_{OUT} is inversely proportional to C_{INT} and the Input Frequency.

C_{INT} can be increased to lower the ripple. 1 μF to 100 μF are perfectly acceptable values for low frequencies.

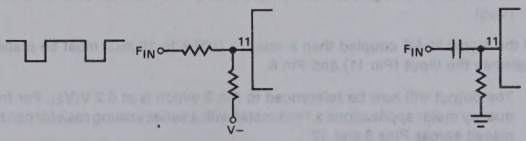
When TSC9400 is used in the single supply mode, V_{REF} is defined as the voltage difference between Pin 7 and Pin 2.

Input Voltage Levels

The input signal must cross through zero in order to trip the comparator. In order to overcome the hysteresis the amplitude must be greater than ±200 mV.

If only a unipolar input signal (F_{IN}) is available, it is recommended that either an offset circuit using resistor be used or that the signal be coupled in a via a capacitor.

For 100 kHz maximum input R_{INT} should be decreased to 100 kΩ.


FIN
11
V−
FIN
11

NOTE: C_{REF} should be increased for low F_{IN} max. Adjust C_{REF} so that V_O is approximately 2.5 to 3.0 volts for the maximum input frequency. When F_{IN} max is less than 1 kHz, the duty cycle should be greater than 20% to insure that C_{REF} is fully charged and discharged.

F/V Design Information (Cont.)

Input Buffer

f_o and $f_o/2$ are not used in the F/V mode. However, these outputs may be useful for some applications, such a buffer to feed additional circuitry. F_o will then follow the input frequency wave form; except that f_o will go high 3 µs after F_{IN} goes high. $f_o/2$ will be square wave with a frequency of one half f_o.

If these outputs are not use, then Pins 8, 9 and 10 may be left floating or connected to ground.

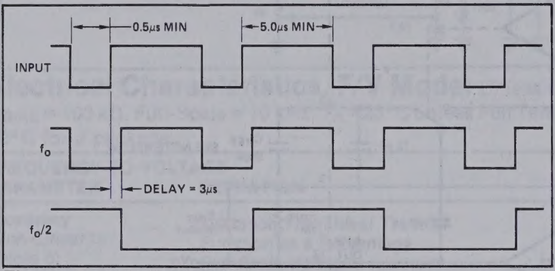
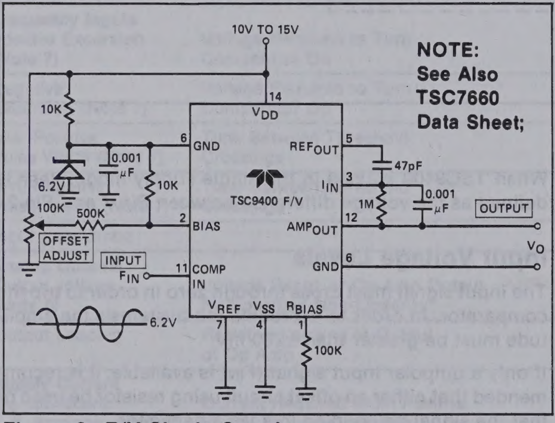

0.5µs MIN
5.0µs MIN
INPUT
f_o
DELAY = 3µs
$f_o/2$

Figure 8: F/V Digital Outputs


10V TO 15V
14
V_{DD}
10K
6
GND
REF_{OUT}
5
47pF
0.001 µF
6.2V
10K
3
I_{IN}
1M
0.001 µF
OUTPUT
TSC9400 F/V
100K
500K
2
BIAS
AMP_{OUT}
12
V_O
OFFSET ADJUST
INPUT
F_{IN}
11
COMP IN
GND
6
6.2V
V_{REF}
V_{SS}
R_{BIAS}
7
4
1
100K

NOTE: See Also TSC7660 Data Sheet;

Figure 9: F/V Single Supply

Notes:

1. The input is now referenced to 6.2 V (Pin 6). The input signal must therefore be restricted to be greater than 4 volts (Pin 6 –2 V) and less than 10 to 15 V (V_{DD}).

If the signal is AC coupled then a resistor (100 k to 10 mΩ) must be placed between the input (Pin 11) and Pin 6.

2. The output will now be referenced to Pin 6 which is at 6.2 V(Vz). For frequency meter applications a 1 mA meter with a series scaling resistor can be placed across Pins 6 and 12.

The sawtooth ripple which is on the output of an F/V can be eliminated without affecting the F/V's response time by using the circuit in Figure 10. The circuit has a DC gain of +1. Any AC components such as a ripple are amplified both positively, via the lower path, and negatively, via the upper path.

When both paths have the same gain, the AC ripple is cancelled. The amount of cancellation is directly proportional to gain matching. If the two paths are matched within 10%, then the ripple will be lowered by 1/10. For 1% matching, the ripple is lowered by 1/100. The 10 k potentiometer is used to make the gain equal in both paths. This circuit is insensitive to both frequency changes and to signal wave shape.

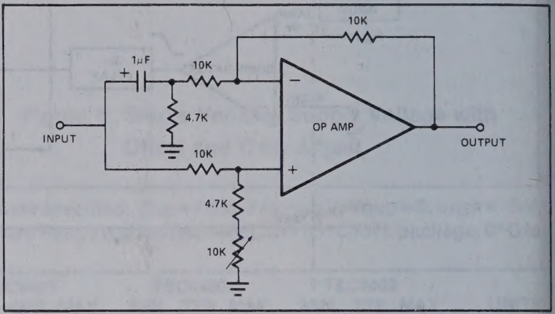

10K
1µF
+
10K
−
4.7K
OP AMP
INPUT
OUTPUT
10K
+
4.7K
10K

Figure 10: F/V Ripple Eliminator

F/V Power-On Reset

In the F/V mode, the TSC9400 output voltage will occasionally be at its maximum value when power is first applied. This condition will remain until the first pulse is applied to the F_{IN} input. In most frequency-measurement applications this is not a problem, because proper operation begins as soon as the frequency input is applied.

In some cases, however, the TSC9400 output must be zero at power-on without a frequency input. In such cases, a capacitor connected from Pin 11 to V_{DD} will usually be sufficient to pulse the TSC9400 and provide a power on reset (Figure 11a). Where predictable power-on operation is critical, a more complicated circuit, such as Figure 11b, may be required.

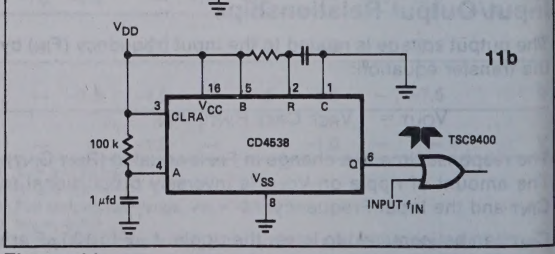

V_{DD}
11a
14
1000 pf
V_{DD}
INPUT f_{IN}
1 kΩ
11
COMP
V_{DD}
11b
16
5
2
1
3
$CLRA$
V_{CC}
B
R
C
100 k
CD4538
TSC9400
4
A
Q
6
V_{SS}
1 µfd
8
INPUT f_{IN}

Figure 11

SECTION 10

Display Drivers

Section 10

Display Drivers 10-3

TSC700A	High Current Four Digit LED Driver	10-5
TSC701AM	High Current Bus Compatible Four Digit LED Driver	10-13
TSC7211A	Four Digit LCD Driver	10-21
TSC7212A	Four Digit LED Driver	10-21
TSC7211AM	Bus Compatible Four Digit LCD Driver	10-33
TSC7212AM	Bus Compatible Four Digit LED Driver	10-33

TELEDYNE SEMICONDUCTOR

TSC700A
Four Digit LED Display Decoder and Driver
High Segment Drive Current

General Description

The TSC700A drives common anode LED displays with 28 high current, open-drain N channel output transistors. Four seven segment LED displays may be driven. Drive current is guaranteed to be 11 mA minimum. This is twice the minimum drive current available from comparable devices and will provide high LED luminance. High luminous intensity is an important factor when a dark contrasting background is unavailable or the LED is viewed at a distance. The TSC700A current capability makes it an ideal large character LED driver.

Four data bit inputs and four digit select signals permit interfacing to multiplexed BCD or binary output devices. The four bit data input is decoded into the seven segment alphanumeric code known as "Code B". A 0 to 9, —, E, H, L, P or "blank" reading may be displayed.

An added feature includes a brightness control input that adjusts segment drive current. The control pin may also be used as a digital display enable. The TSC700A is an improved pin compatible and functional equivalent to the ICM7212A and TSC7212A.

Ordering Information

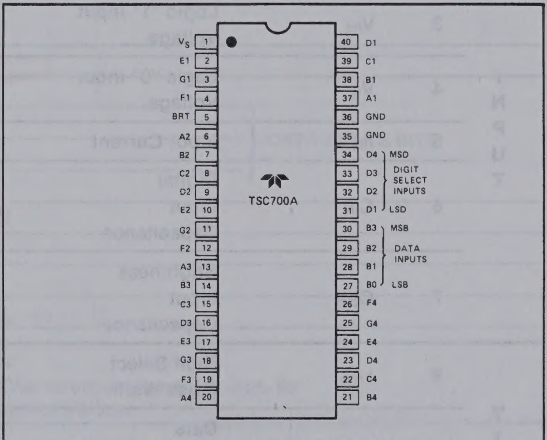
Part No.	Package	Temp. Range	LED Segment Current	Output Code
TES700AMJL*	40-Pin CerDIP	-55°C to +125°C	14 mA	Code B
TSC700AIJL*	40-Pin CerDIP	-25°C to +85°C	14 mA	Code B
TSC700A/Y	CHIP	25°C	14 mA	Code B

* Add /BI to part number suffix for 160 hour, +125°C burn-in.

Features

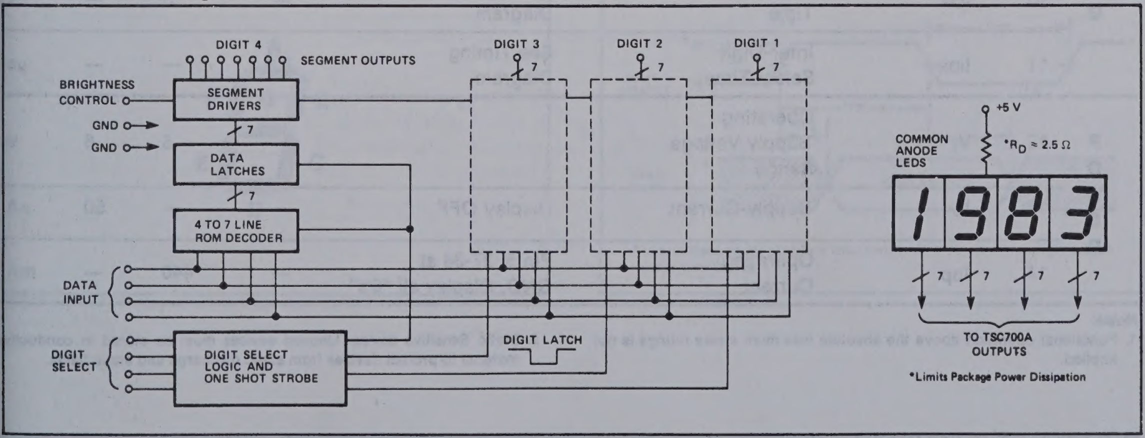
- High Drive Current for High Luminance LED Display
- Guaranteed High LED Segment Current 11 mA Minimum
- 28 Common Anode LED Drivers (4 Digits)
- Code B Output Format . . . 0 to 9, —, E, H, L, P, "blank"
- BCD/Binary Input to Seven Segment LED Code
- Four Separate Digit Selects for Multiplexed Input
- Digital or Analog Brightness Control
- Digital Display Enable
- Low Thermal Resistance Package
- Military Temperature Range Devices Available
- Pin Compatible With TSC7212A, ICM7212A

Pin Configuration


TSC700A
VS 1
E1 2
G1 3
F1 4
BRT 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
40 D1
39 C1
38 B1
37 A1
36 GND
35 GND
34 D4 MSD
33 D3
32 D2
31 D1 LSD
DIGIT SELECT INPUTS
30 B3 MSB
29 B2
28 B1
27 B0 LSB
DATA INPUTS
26 F4
25 G4
24 E4
23 D4
22 C4
21 B4

If Brightness Control is not needed, connect BRT (pin 5) to Vs.

Functional Diagram


DIGIT 4
SEGMENT OUTPUTS
DIGIT 3
DIGIT 2
DIGIT 1
7
BRIGHTNESS CONTROL
SEGMENT DRIVERS
GND
GND
7
DATA LATCHES
7
4 TO 7 LINE ROM DECODER
DATA INPUT
DIGIT SELECT
DIGIT SELECT LOGIC AND ONE SHOT STROBE
DIGIT LATCH
+5 V
COMMON ANODE LEDS
*R_D ≈ 2.5 Ω
1983
7
7
7
7
TO TSC700A OUTPUTS
*Limits Package Power Dissipation

© 1983

TSC700A

Four Digit LED Display Decoder and Driver

High Segment Drive Current

Absolute Maximum Ratings (Notes 1, 2)

Power Dissipation	*1.0 W
Supply Voltage	6.5 V
Input Voltage (Any Terminal)	V_S + 0.3 V to Ground −0.3 V
Operating Temperature	
M Version	−55° C to +125° C
I Version	−25° C to +85° C
Maximum Chip Temperature	+150° C
Storage Temperature	−55° C to +150° C
Lead Temperature (10 Sec)	300° C

* To 85° C, See Derating Curve on Page 4 for operation above 85° C.

Electrical Characteristics: Specifications measured with V_S = 5.0 V at T_A = 25° C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC700A MIN	TSC700A TYP	TSC700A MAX	UNIT
LED DRIVER	1	I_{SEG}	Segment ON Current	Test Circuit	11	14	18	mA
	2	I_{SLK}	Segment Leakage		—	±0.01	±1.0	µA
INPUT	3	V_{IH}	Logic "1" Input Voltage		3.0	—	—	V
	4	V_{IL}	Logic "0" Input Voltage		—	—	1.0	V
	5	I_{IN}	Input Current	Pins 27-34	—	±0.01	±1.0	µA
	6	C_{IN}	Digital Input Capacitance	Pins 27-34	—	5	—	pF
	7	C_{BR}	Brightness Input Capacitance		—	200	—	pF
TIMING	8	t_{PW}	Digit Select Pulse Width	See Timing Diagram	1.0	—	—	µs
	9	t_{DS}	Data Setup Time	See Timing Diagram	—	—	100	ns
	10	t_{DH}	Data Hold Time	See Timing Diagram	—	0	—	ns
	11	t_{IDS}	Inter-Digit Select Time	See Timing Diagram	2.0	—	—	µs
POWER	12	V_S	Operating Supply Voltage Range		4	5	6	V
	13	I_S	Supply Current	Display OFF	—	—	50	µA
	14	I_{OP}	Operating Current	Pin 5, 27-34 at GND, Display all "8's"	—	440	—	mA

Notes:

1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.

Four Digit LED Display Decoder and Driver
High Segment Drive Current
TSC700A

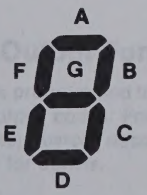
Output Pin Description and Function

OUTPUT	TERMINAL	FUNCTION	OUTPUT	TERMINAL	FUNCTION
A1	37	A Segment Dr. Digit 1 (LSD)	A3	13	A Segment Dr. Digit 3
B1	38	B	B3	14	B
C1	39	C	C3	15	C
D1	40	D	D3	16	D
E1	2	E	E3	17	E
F1	4	F	F3	19	F
G1	3	G	G3	18	G
A2	6	A Segment Dr. Digit 2	A4	20	A Segment Dr. Digit 4 (MSD)
B2	7	B	B4	21	B
C2	8	C	C4	22	C
D2	9	D	D4	23	D
E2	10	E	E4	24	E
F2	12	F	F4	26	F
G2	11	G	G4	25	G

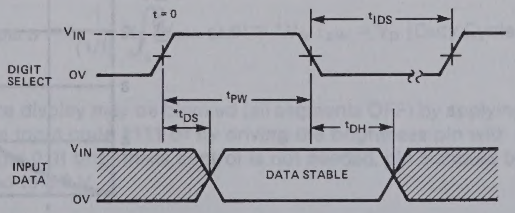
Input Pin Description and Function

INPUT	TERMINAL	FUNCTION	
B0	27	Ones (Least Significant)	DATA INPUTS BITS
B1	28	Twos	
B2	29	Fours	
B3	30	Eights (Most Significant)	
D1	31	D1 (Least Significant) Digit Select	
D2	32	D2 Digit Select	
D3	33	D3 Digit Select	
D4	34	D4 (Most Significant) Digit Select	
BRT	5	Brightness Control: Logic 1 = ON Logic 0 = OFF See Typical Characteristic Curve for I_{SEG} Vs Brightness Control Voltage	

Segment Assignment

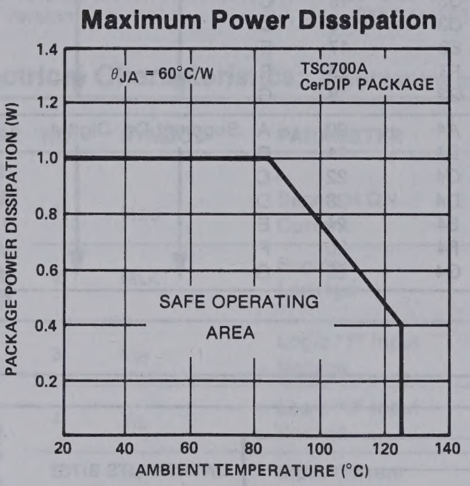


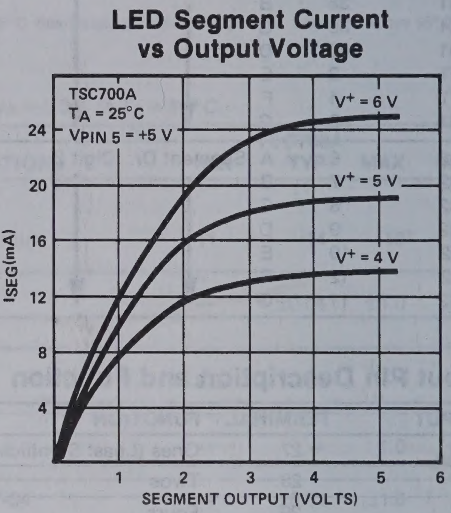
Timing Diagram

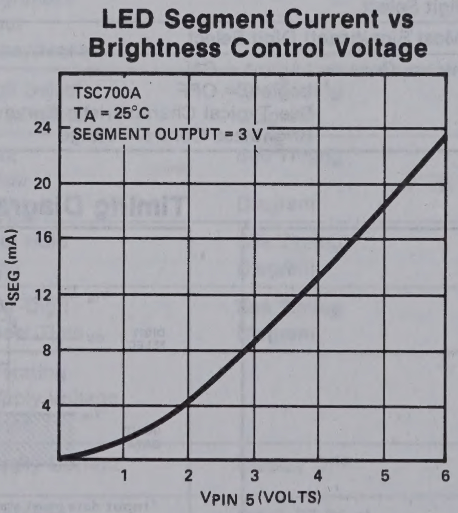


*Input data must stable a maximum of 100 ns after digit select becomes active.

Electrical Operating Characteristics







Operation Description

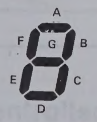
Output Format

The TSC700A accepts four bit binary information at pins 27 (LSB) through 30 (MSB). The binary input is decoded to the seven segment output in a format known as "Code B". The display format is 0 to 9, —, E, H, L, P and "blank".

Output Code

BINARY INPUT				TSC700A Output "Code B"
B3	B2	B1	B0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	-
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

Segment Assignment



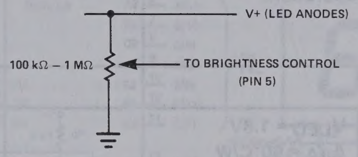
Special Order Output Format

The TSC700A is mask programmed to give 16 combinations of seven segment output codes. For large volume orders (50 K minimum pieces) custom decoder options are available. Contact factory for details.

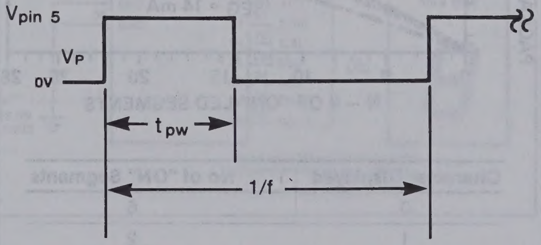
Brightness Control Operation

The voltage at the brightness control input is transferred to the output transistor gate for "ON" segments. The brightness voltage directly modulates the segment driver "ON" resistance. A brightness input (pin 5) can be used in two ways to control output transistor drain current. A variable brightness control may be implemented with a single potentiometer. A high value potentiometer (100 KΩ to 1 MΩ) will minimize power consumption.

Brightness Control



A logic signal of varying duty cycle will also control display brightness.

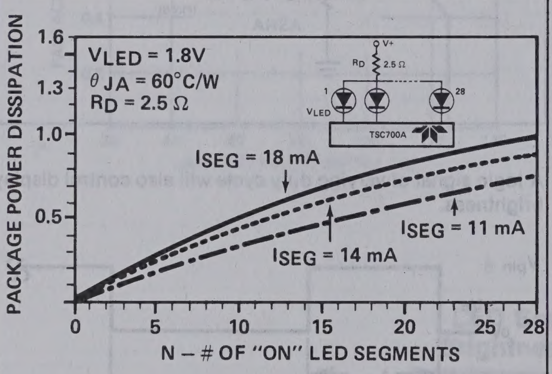


$$V_{pin\ 5} = \left(\frac{1}{(1/f)}\right) \int_{o}^{(1/f)} (V_{pin\ 5})\, dt = f\, V_P\, t_{pw} = V_p \text{ [Duty Cycle]}$$

The display may be blanked (all segments OFF) by applying the input code 1111 or by driving the brightness pin with a logic 0. If brightness control is not needed, pin 5 should be tied to 5.0 V.

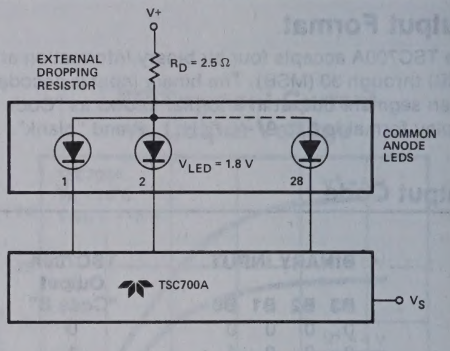
Package Power Dissipation Minimization

The TSC700A high LED current drive capability requires package power dissipation be limited and that a low thermal resistance package be used. The cerDIP package thermal resistance ($\theta jc = 30°$ C/W, $\theta ja = 60°$ C/W) permits operation over the full −25°C to +85°C industrial operating temperature range. Power dissipation is easily controlled by reducing the applied voltage at the segment driver outputs. A 2.5 Ω voltage dropping resistor placed in series with the common anode LED display voltage will maintain dissipation under 1 watt with a worst case continuous 8888 display. Figure 1 gives the package power dissipation vs the number of "ON" LED segments for the operating circuit in Figure 2. Driver outputs should be maintained above 1.85 V for constant current operation.



Character Displayed	No of "ON" Segments
0	6
1	2
2	5
3	5
4	4
5	5
6	6
7	3
8	7
9	6
—	1
E	5
H	5
L	3
P	5

Figure 1: Package Power Dissipation



$$P_D = V_S I_S + I_{SEG}(N)\,[V^+ - V_{LED} - N(I_{SEG})\,R_D]$$

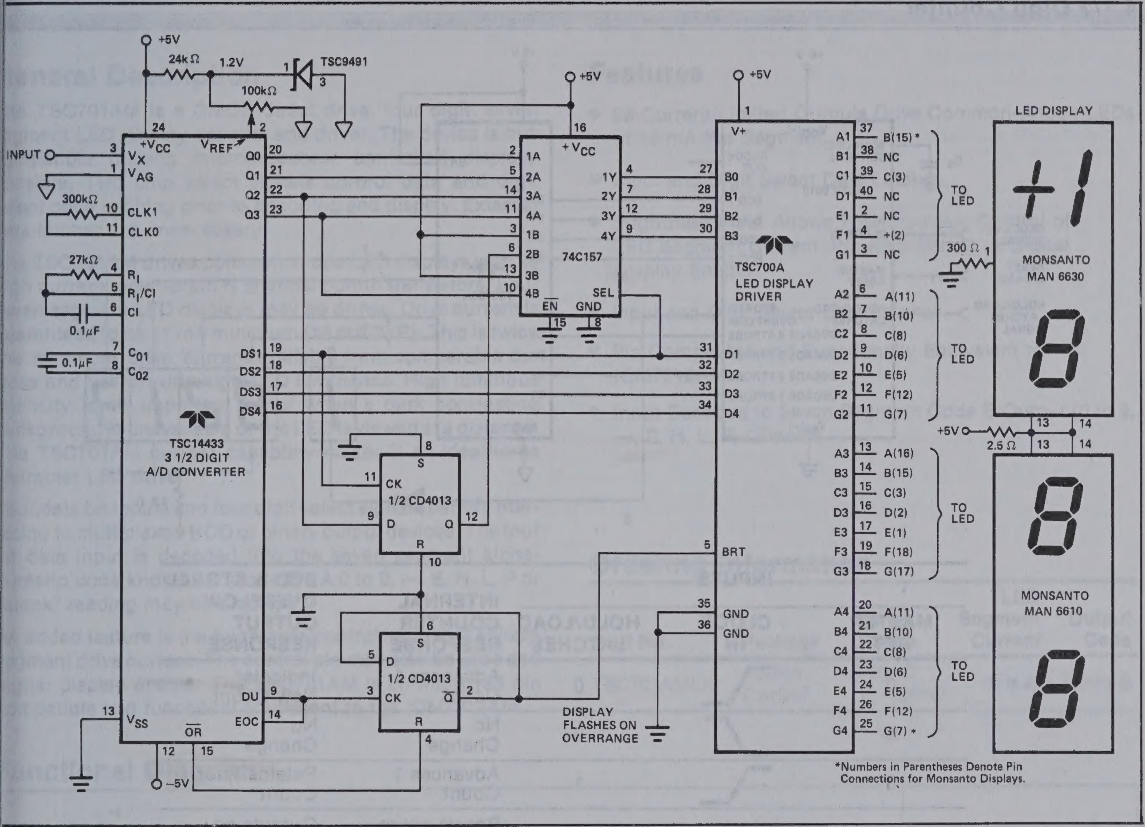
$$\approx I_{SEG}(N)\,[V^+ - V_{LED} - N(I_{SEG})\,R_D]$$

Where:
I_{SEG} = LED Segment Current
N = Number of ON Segments
V_{LED} = Voltage Across on LED
P_D = Max. Package Power Dissipation
V_S = TSC700A Power Supply Voltage (5 V)
I_S = TSC700A Quiescent Current (≈ 50 μA)

Figure 2: Operating Circuit

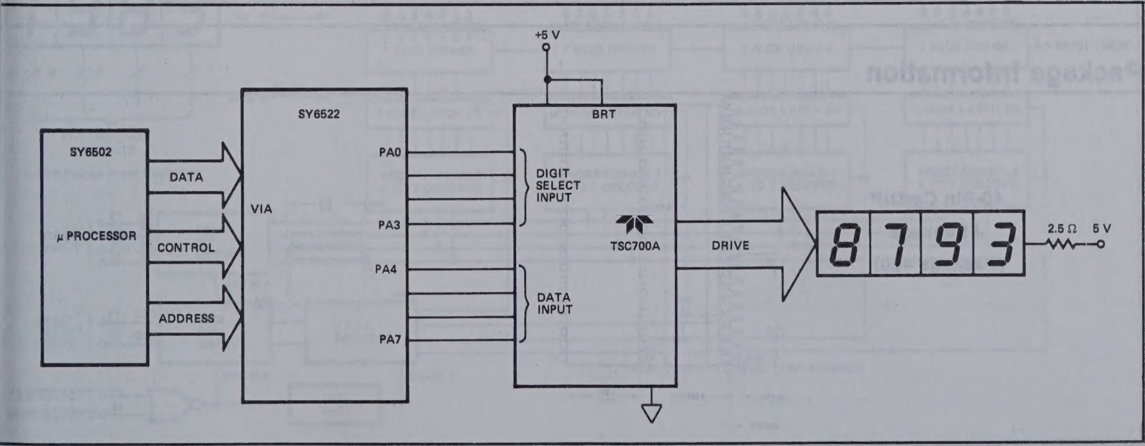
Applications Information:

3 1/2 Digit ADC with LED Display


+5V
24kΩ
1.2V
TSC9491
100kΩ
INPUT
300kΩ
27kΩ
0.1μF
0.1μF
+VCC
VX
VAG
VREF
CLK1
CLK0
RI
RI/CI
CI
CO1
CO2
Q0
Q1
Q2
Q3
DS1
DS2
DS3
DS4
VSS
DU
EOC
OR
TSC14433
3 1/2 DIGIT
A/D CONVERTER
–5V
74C157
+VCC
1A
2A
3A
4A
1B
2B
3B
4B
1Y
2Y
3Y
4Y
SEL
EN
GND
1/2 CD4013
CK
S
D
Q
R
1/2 CD4013
Q̄
DISPLAY
FLASHES ON
OVERRANGE
V+
B0
B1
B2
B3
D1
D2
D3
D4
BRT
GND
GND
TSC700A
LED DISPLAY
DRIVER
A1
B1
C1
D1
E1
F1
G1
A2
B2
C2
D2
E2
F2
G2
A3
B3
C3
D3
E3
F3
G3
A4
B4
C4
D4
E4
F4
G4
B(15)*
NC
C(3)
NC
NC
+(2)
NC
A(11)
B(10)
C(8)
D(6)
E(5)
F(12)
G(7)
A(16)
B(15)
C(3)
D(2)
E(1)
F(18)
G(17)
A(11)
B(10)
C(8)
D(6)
E(5)
F(12)
G(7) *
TO
LED
300 Ω
+5V
2.5 Ω
LED DISPLAY
MONSANTO
MAN 6630
MONSANTO
MAN 6610

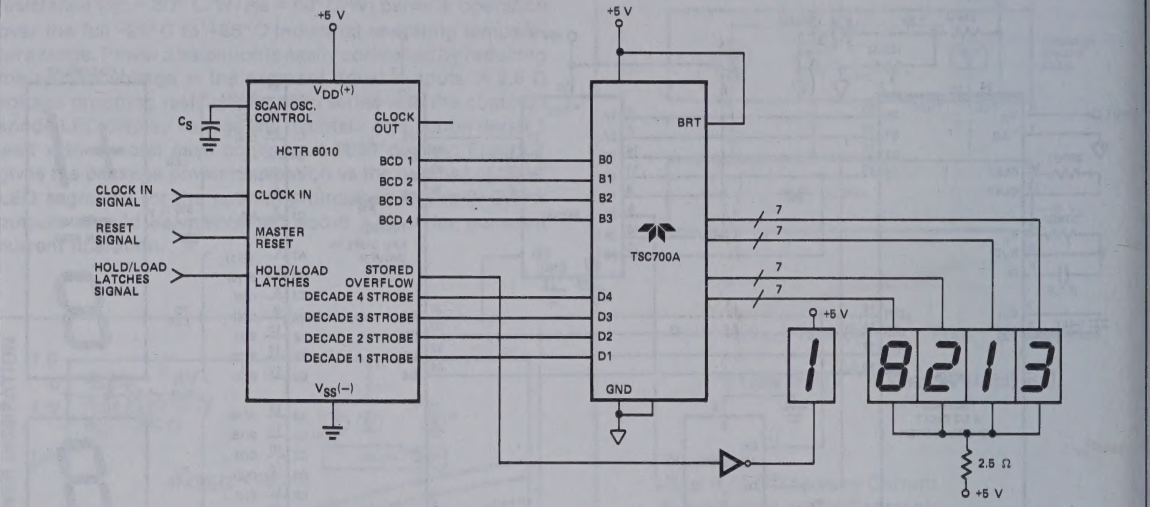
*Numbers in Parentheses Denote Pin Connections for Monsanto Displays.

μ - Processor Controlled Display


SY6502
μ PROCESSOR
DATA
CONTROL
ADDRESS
SY6522
VIA
PA0
PA3
PA4
PA7
+5 V
BRT
DIGIT
SELECT
INPUT
DATA
INPUT
TSC700A
DRIVE
8793
2.5 Ω
5 V

Applications Information (continued)

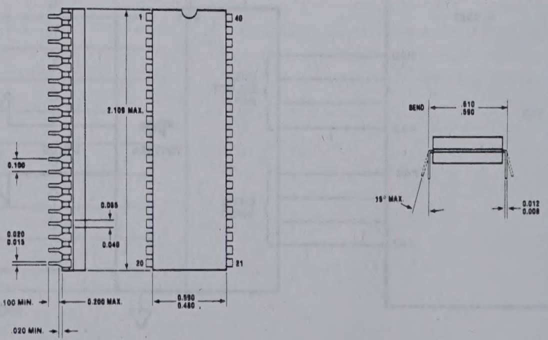
4 1/2 Digit Counter


+5 V
VDD(+)
SCAN OSC. CONTROL
CS
CLOCK OUT
HCTR 6010
BCD 1
BCD 2
BCD 3
BCD 4
CLOCK IN SIGNAL
CLOCK IN
RESET SIGNAL
MASTER RESET
HOLD/LOAD LATCHES SIGNAL
HOLD/LOAD LATCHES
STORED OVERFLOW
DECADE 4 STROBE
DECADE 3 STROBE
DECADE 2 STROBE
DECADE 1 STROBE
VSS(−)
+5 V
BRT
B0
B1
B2
B3
TSC700A
D4
D3
D2
D1
GND
7
7
7
7
+5 V
1
8213
2.5 Ω
+5 V

INPUTS			INTERNAL COUNTER RESPONSE	BCD & STORED OVERFLOW OUTPUT RESPONSE
MASTER RET	CLOCK IN	HOLD/LOAD LATCHES		
0	↘	0	Advances 1 Count	Indicates New Count
0	↗	0	No Change	No Change
0	↘	1	Advances 1 Count	Retains Prior Count
1	x	0	Resets entire Counter	Outputs go to Zero
1	x	1	Resets entire Counter	Retains Prior Count

Package Information

40-Pin CerDIP
J Package
(Package #20)


1
40
2.109 MAX.
0.100
0.065
0.040
0.020
0.015
20
21
.100 MIN.
0.200 MAX.
0.590
0.480
.020 MIN.
BEND
.610
.590
15° MAX.
0.012
0.008

TELEDYNE
EMICONDUCTOR

TSC701AM
Bus Compatible Four Digit LED Display Driver
• High Segment Drive Current
• Input Data Latches

eneral Description

he TSC701AM is a CMOS direct drive, four digit, seven egment LED display decoder and driver. The device is bus ompatible making microprocessor controlled displays ossible. Two chip select signals control data and digit elect code latching prior to decoding and display. External ata latches are unnecessary.

he TSC701AM drives common anode LED displays with 28 igh current, open-drain N channel output transistors. Four even segment LED displays may be driven. Drive current is uaranteed to be 11 mA minimum (18 mA TYP). This is twice e minimum drive current available from comparable deices and will provide high LED luminance. High luminous tensity is an important factor when a dark contrasting ackground is unavailable or the LED is viewed at a distance. he TSC701AM current capability makes it an ideal large haracter LED driver.

our data bit inputs and four digit select signals permit interacing to multiplexed BCD or binary output devices. The four it data input is decoded into the seven segment alphaumeric code known as "Code B". A 0 to 9, —, E, H, L, P or blank" reading may be displayed.

n added feature is the brightness control input that adjusts egment drive current. The control pin may also be used as a igital display enable. The TSC701AM is an improved pin ompatible and functional equivalent to the ICM7212AM.

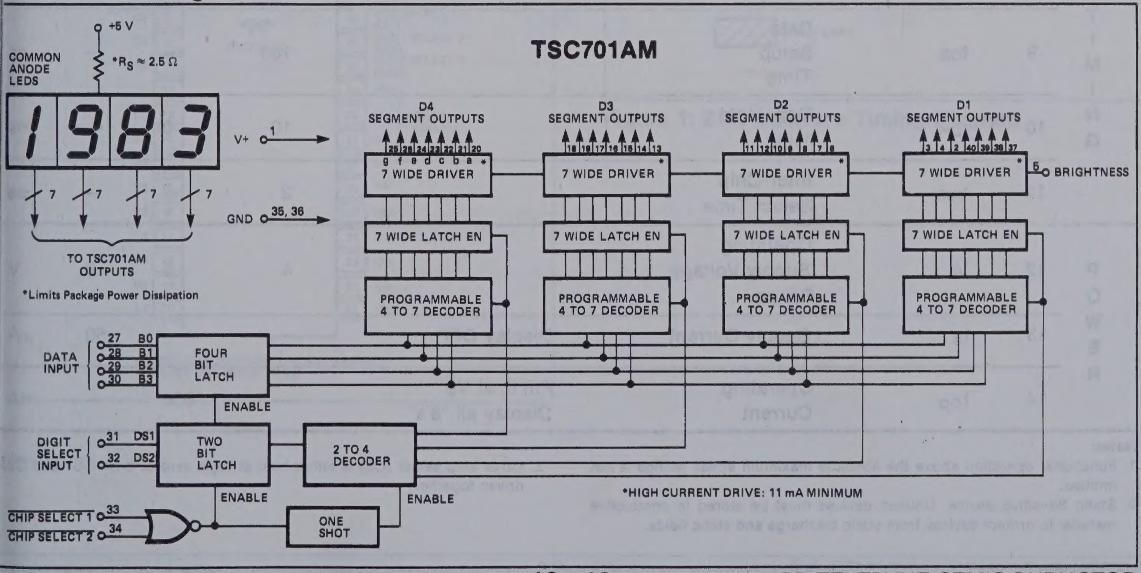
Features

- 28 Current Limited Outputs Drive Common-Anode LEDs at 18 mA Per Segment.
- Input and Digit Select Data Latches.
- Brightness Input Allows Potentiometer Control of LED Segment Current. Pin Also Serves as Digital Display Enable.
- Input and Digit Select Data Latches.
- Pin Compatible and Functionally Equivalent to ICM7212AM.
- Input Decoded to Seven Segment Code B Output (0 to 9, —, E, H, L, P, "Blank")

Ordering Information

Part No.	Package	Temp. Range	LED Segment Current	Output Code
TSC701AMIJL	40-Pin CerDIP	-25° C to +85° C	18 mA	Code B

unctional Diagram


TSC701AM
+5 V
COMMON ANODE LEDS
*RS ≈ 2.5 Ω
1983
V+
1
GND
35, 36
7
7
7
7
TO TSC701AM OUTPUTS
*Limits Package Power Dissipation
D4 SEGMENT OUTPUTS
25 26 24 23 22 21 20
g f e d c b a
D3 SEGMENT OUTPUTS
18 19 17 16 15 14 13
D2 SEGMENT OUTPUTS
11 12 10 8 9 7 6
D1 SEGMENT OUTPUTS
3 4 2 40 39 38 37
7 WIDE DRIVER
5
BRIGHTNESS
7 WIDE LATCH EN
PROGRAMMABLE 4 TO 7 DECODER
DATA INPUT
27 B0
28 B1
29 B2
30 B3
FOUR BIT LATCH
ENABLE
DIGIT SELECT INPUT
31 DS1
32 DS2
TWO BIT LATCH
2 TO 4 DECODER
ENABLE
ENABLE
CHIP SELECT 1 33
CHIP SELECT 2 34
ONE SHOT
*HIGH CURRENT DRIVE: 11 mA MINIMUM

© 1983

Bus Compatible Four Digit LED Display Driver

• High Segment Drive Current
• Input Data Latches

TSC701AM

Absolute Maximum Ratings

Power Dissipation .... 1.0 W
Supply Voltage .... 6.5 V
Input Voltage (Any Terminal) V_S + 0.3 V to Ground −0.3 V
Operating Temperature
I Version .... −25° C to +85° C

Maximum Chip Temperature .... +150° C
Storage Temperature .... −55° C to +150° C
Lead Temperature (10 Sec) .... 300° C

Electrical Characteristics: Specifications measured with V_S = 5.0 V at T_A = 25° C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC701AM MIN	TYP	MAX	UNIT
LED DRIVER	1	I_{SEG}	Segment ON Current	Test Circuit	11	18	20	mA
	2	I_{SLK}	Segment Leakage		—	±0.01	±1.0	µA
INPUT	3	V_{IH}	Logic "1" Input Voltage		3.0	—	—	V
	4	V_{IL}	Logic "0" Input Voltage		—	—	1.0	V
	5	I_{IN}	Input Current	Pins 27-34, 5	—	±0.01	±1.0	µA
	6	C_{IN}	Digital Input Capacitance	Pins 27-34	—	5	—	pF
	7	C_{BR}	Brightness Input Capacitance		—	200	—	pF
TIMING	8	t_{CSA}	Chip Select Active Pulse Width	Note 3	200	—	—	ns
	9	t_{DS}	Data Setup Time		100	—	—	ns
	10	t_{DH}	Data Hold Time		10	0	—	ns
	11	t_{ICS}	Inter-Chip Select Time		2	—	—	µs
POWER	12	V_S	Operating Supply Voltage Range		4	5	6	V
	13	I_S	Supply Current	Display OFF	—	—	50	µA
	14	I_{op}	Operating Current	Pin 5, at V_S^+ Display all "8's"	—	504	—	mA

Notes:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Other chip select ($\overline{CS}$) is either held at logic zero or both $\overline{CS1}$ and $\overline{CS2}$ driven together.

Bus Compatible Four Digit LED Display Driver

- **High Segment Drive Current**
- **Input Data Latches**

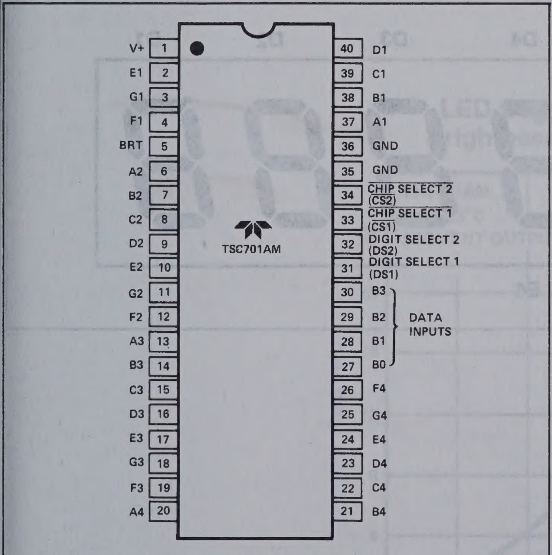
TSC701AM

Input Definitions

In this table, V + and GROUND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V + Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V+ = Logical One GND = Logical Zero	Twos	
B2	29	V+ = Logical One GND = Logical Zero	Fours	
B3	30	V+ = Logical One GND = Logical Zero	Eights (Most Significant)	
DS1	31	V+ = Logical One	Digit Select Inputs DS2, DS1 = 00 Selects D4 DS2, DS1 = 01 Selects D3 DS2, DS1 = 10 Selects D2 DS2, DS1 = 11 Selects D1	
DS2	32	GND = Logical Zero		
$\overline{CS1}$	33	V+ = Inactive	When both $\overline{CS1}$ and $\overline{CS2}$ are low the data and digit select input latches are open or enabled. On the rising of $\overline{CS1}$ or $\overline{CS2}$ data is latched, decoded and stored in the output drive latches.	
$\overline{CS2}$	34	GND = Active		

Pin Configuration


V+ 1
E1 2
G1 3
F1 4
BRT 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
40 D1
39 C1
38 B1
37 A1
36 GND
35 GND
34 CHIP SELECT 2 (CS2)
33 CHIP SELECT 1 (CS1)
32 DIGIT SELECT 2 (DS2)
31 DIGIT SELECT 1 (DS1)
30 B3
29 B2
28 B1
27 B0
DATA INPUTS
26 F4
25 G4
24 E4
23 D4
22 C4
21 B4
TSC701AM

IF BRIGHTNESS CONTROL IS NOT NEEDED, CONNECT BRT (PIN 5) TO V_S.

Timing Diagram

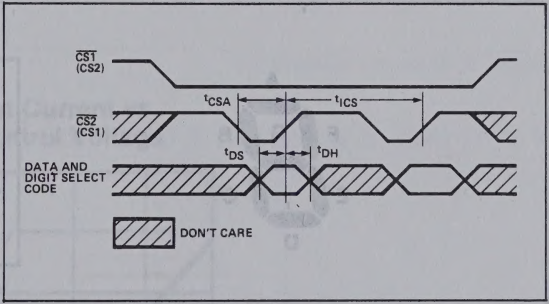

$\overline{CS1}$ ($\overline{CS2}$)
t_{CSA}
t_{ICS}
$\overline{CS2}$ ($\overline{CS1}$)
t_{DS}
t_{DH}
DATA AND DIGIT SELECT CODE
DON'T CARE

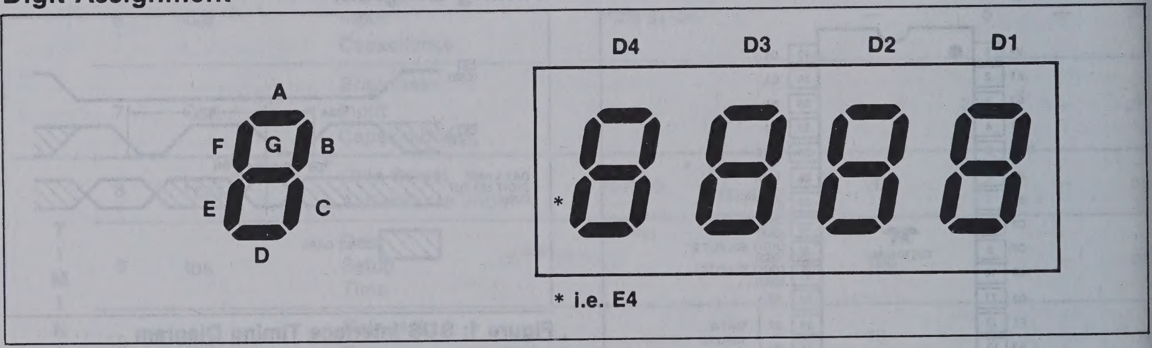
Figure 1: BUS Interface Timing Diagram

Output Definitions

Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

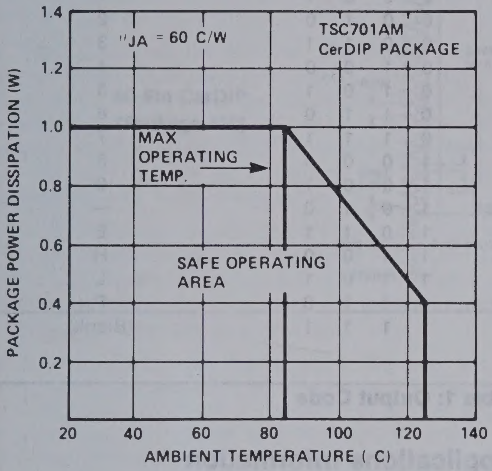
OUTPUT	TERMINAL	FUNCTION	OUTPUT	TERMINAL	FUNCTION
A1	37	A Segment Dr. Digit 1 (LSD)	A3	13	A Segment Dr. Digit 3
B1	38	B	B3	14	B
C1	39	C	C3	15	C
D1	40	D	D3	16	D
E1	2	E	E3	17	E
F1	4	F	F3	19	F
G1	3	G	G3	18	G
A2	6	A Segment Dr. Digit 2	A4	20	A Segment Dr. Digit 4 (MSD)
B2	7	B	B4	21	B
C2	8	C	C4	22	C
D2	9	D	D4	23	D
E2	10	E	E4	24	E
F2	12	F	F4	26	F
G2	11	G	G4	25	G

Digit Assignment

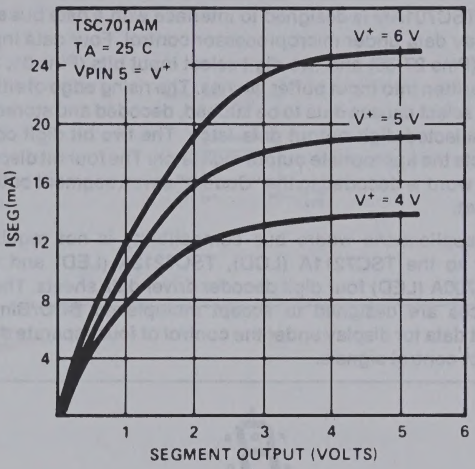


Electrical Operating Characteristics

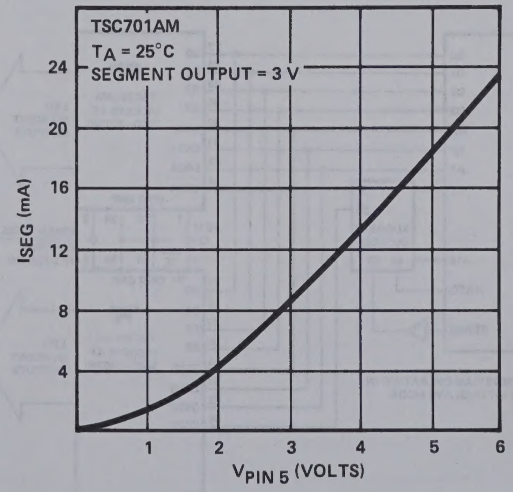
Maximum Power Dissipation



LED Segment Current vs Output Voltage



LED Segment Current vs Brightness Control Voltage



Input Configuration and Output Codes

The TSC701AM accepts a four bit, true binary (positive level = logic 1) input at pins 27 (LSB) through 30 (MSB). The output display format is 0 to 9, —, E, H, L, P and blank (see Table 1). The TSC701AM correctly decodes binary and BCD true codes to a seven segment output.

The TSC701AM is designed to interface with a data bus and display data under microprocessor control. Four data input bits (Pins 27-30) and two digit select input bits (Pins 31, 32) are written into input buffer latches. The rising edge of either chip select causes data to be latched, decoded and stored in the selected digit output data latch. The two bit digit code selects the appropriate output digit latch. The four bit display data word is decoded to the "Code B" seven segment output format.

For applications where bus compatibility is not required refer to the TSC7211A (LCD), TSC7212A (LED) and the TSC700A (LED) four digit decoder driver data sheets. These devices are designed to accept multiplexed BCD/Binary input data for display under the control of four separate digit select control signals.

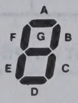


Figure 5: Segment Assignment

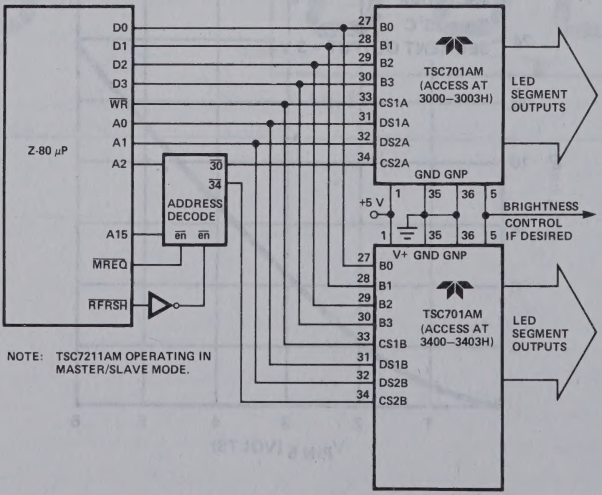
BINARY INPUT				CODE B TSC701AM
B3	B2	B1	B0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	—
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

Table 1: Output Code

Applications Information

The TSC701AM has two ground pins. These pins should be connected together.

TSC701AM Interfaced to Z-80 Microprocessor


Z-80 μP
D0
D1
D2
D3
$\overline{\text{WR}}$
A0
A1
A2
A15
$\overline{\text{MREQ}}$
$\overline{\text{RFRSH}}$
ADDRESS DECODE
$\overline{30}$
$\overline{34}$
$\overline{\text{en}}$ $\overline{\text{en}}$
27 B0
28 B1
29 B2
30 B3
33 CS1A
31 DS1A
32 DS2A
34 CS2A
GND GNP
TSC701AM (ACCESS AT 3000–3003H)
LED SEGMENT OUTPUTS
+5 V
1
35
36
5
BRIGHTNESS CONTROL IF DESIRED
V+ GND GNP
27 B0
28 B1
29 B2
30 B3
33 CS1B
31 DS1B
32 DS2B
34 CS2B
TSC701AM (ACCESS AT 3400–3403H)
LED SEGMENT OUTPUTS

NOTE: TSC7211AM OPERATING IN MASTER/SLAVE MODE.

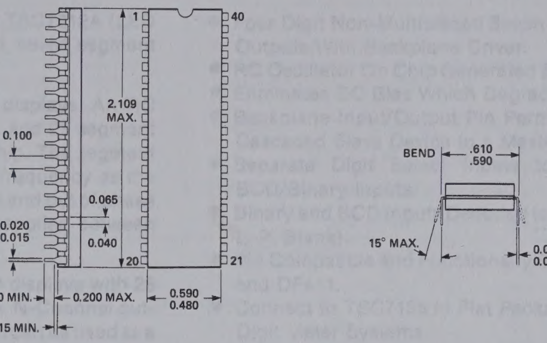
Bus Compatible Four Digit LED Display Driver

- **High Segment Drive Current**
- **Input Data Latches**

TSC701AM

Package Information

40-Pin CerDIP
(Package #20)



1
40
2.109
MAX.
0.100
BEND
.610
.590
0.065
0.020
0.015
0.040
15° MAX.
0.012
0.008
20
21
0.090 MIN.
0.200 MAX.
0.590
0.480
0.015 MIN.

Notes

TELEDYNE
SEMICONDUCTOR

TSC7211A (LCD)
TSC7212A (LED)

Four Digit CMOS Display Decoder and Driver

General Description

The TSC7211A (LCD Decoder/Driver) and TSC7212A (LED Decoder/Driver) are direct drive, four digit, seven segment display decoder and drivers.

The TSC7211A drives conventional LCD displays. An RC oscillator, divider chain, backplane driver, and 28 segment outputs are provided on a single CMOS chip. The segment drivers supply square waves of the same frequency as the backplane but in phase for an OFF segment and out of phase for an ON segment. The net d.c. voltage applied between driver segment and backplane is zero.

The TSC7212A drives common anode LED displays with 28 current controlled, low leakage, open drain, N-Channel output transistors. The brightness control input can be used as a digital display enable. A varying voltage at the control input will allow continuous display brightness control.

The TSC7211A (LCD) and TSC7212A (LED) require only four data bit inputs and four digit select signals to interface with multiplexed BCD or binary output devices such as the ICM7217, ICM7226, ICL7103 and TSC7135. The four bit binary input code is decoded into the seven segment alphanumeric code known as "Code B."

The "Code B" output format results in a 0 to 9, —, E, H, L, P or blank display. True BCD or binary inputs will be correctly decoded to the seven segment display format.

The CMOS TSC7211A and TSC7212A are available in a 40-pin epoxy dual-in-line package and a compact 60-pin flat package. All inputs are protected against static discharge.

TSC7211A Features (LCD Driver)

- Four Digit Non-Multiplexed Seven Segment LCD Display Outputs With Backplane Driver.
- RC Oscillator On Chip Generated Backplane Drive Signal.
- Eliminates DC Bias Which Degrade LCD Display Life.
- Backplane Input/Output Pin Permits Synchronization of Cascaded Slave Device to a Master Backplane Signal.
- Separate Digit Select Inputs to Accept Multiplexed BCD/Binary Inputs.
- Binary and BCD Inputs Decoded to Code B (0 to 9, —, E, H, L, P, Blank).
- Pin Compatible and Functionally Equivalent to ICM7211A and DF411.
- Connect to TSC7135 in Flat Package For Compact 4 1/2 Digit Meter Systems

TSC7212A Features (LED Driver)

- 28 Current Limited Outputs Drive Common Anode LEDs at Greater Than 5 mA Per Segment.
- Brightness Input Allows Potentiometer Control of LED Segment Current. Pin Also Serves as Digital Display Enable.
- Same Input Configuration and Output Decoding as the TSC7211A.
- Pin Compatible and Functionally Equivalent to ICM7212A.

Ordering Information

Part No.	Driver Type	Package	Output Code	Input Config.
TSC7211AIPL	LCD	40-Pin Epoxy Dip	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212AIPL	LED	40-Pin Epoxy Dip	Code B	Multiplexed 4-Bit Binary or BCD
TSC7211A/Y	LCD	DICE	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212A/Y	LED	DICE	Code B	Multiplexed 4-Bit Binary or BCD
TSC7211AIJL	LCD	40-Pin CerDIP	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212AIJL	LED	40-Pin CerDIP	Code B	Multiplexed 4-Bit Binary or BCD
TSC7211AIBQ	LCD	60-Pin Flat Package Formed Leads	Code B	Multiplexed 4-Bit Binary or BCD
TSC7211AISQ	LCD	60-Pin Flat Package Unformed Leads	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212AIBQ	LED	60-Pin Flat Package Formed Leads	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212AISQ	LED	60-Pin Flat Package Unformed Leads	Code B	Multiplexed 4-Bit Binary or BCD

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Absolute Maximum Ratings

Power Dissipation (Note 1)	0.8 W at 70° C
Supply Voltage	6.5 V
Input Voltage (Any Terminal) (Note 2)	V⁺ +0.3 V, GROUND −0.3 V
Operating Temperature Range	−20° C to +85° C
Storage Temperature Range	−55° C to +125° C
Lead Temperature (Soldering 10 sec.)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This limit refers to that of the package and will not be realized during normal operation.

Note 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V⁺ or less than GROUND may cause destructive device latchup. For this reason it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the TSC7211A/TSC7212A be turned on first.

Table I: Operating Characteristics

Test Conditions: All parameters measured with V+ = 5 V

TSC7211A CHARACTERISTICS (LCD DECODER/DRIVER)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{OP}	Test Circuit, Display Blank	—	10	50	µA
Oscillator Input Current	I_{OSCI}	Pin 36	—	± 2	± 10	µA
Segment Rise/Fall Time	t_{rfs}	C_L = 200 pF	—	0.5	—	µA
Backplane Rise/Fall Time	t_{rfb}	C_L = 5000 pF	—	1.5	—	µs
Oscillator Frequency	f_{OSC}	Pin 36 Floating	—	16	—	kHz
Backplane Frequency	f_{bp}	Pin 36 Floating	—	125	—	Hz

TSC7212A CHARACTERISTICS (COMMON ANODE LED DECODER/DRIVER)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{OP}	Pin 5 (Brightness), Pins 27-34 — GROUND	—	10	50	µA
Operating Current	I_{OP}	Pin 5 at V+, Display all 8's	—	200	—	mA
Segment Leakage Current	I_{SLK}	Segment Off	—	± 0.01	± 1	µA
Segment On Current	I_{SEG}	Segment On, V_O = +3 V	5	8	—	mA

INPUT CHARACTERISTICS (LCD AND LED DECODER/DRIVER)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" Input Voltage	V_{IH}		3	—	—	V
Logical "0" Input Voltage	V_{IL}		—	—	1	V
Input Leakage Current	I_{ILK}	Pins 27-34	—	± 0.01	± 1	µA
Input Capacitance	C_{IN}	Pins 27-34	—	5	—	pF
BP/Brightness Input Leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND	—	± 0.01	± 1	µA
BP/Brightness Input Capacitance	C_{BPI}	All Devices	—	200	—	pF

AC CHARACTERISTICS (LCD AND LED DECODER/DRIVER)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Digit Select Active Pulse Width	t_{sa}	Refer to Timing Diagrams	1	—	—	µs
Data Valid Time	t_{ds}	Refer to Timing Diagrams	—	—	100	ns
Data Hold Time	t_{dh}	Refer to Timing Diagrams	200	—	—	ns
Inter-Digit Select Time	t_{ids}	Refer to Timing Diagrams	2	—	—	µs

Timing Diagrams

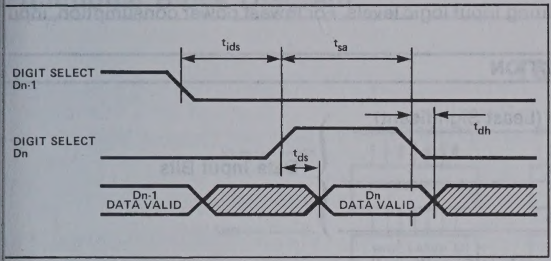

t_{ids}
t_{sa}
DIGIT SELECT Dn-1
DIGIT SELECT Dn
t_{dh}
t_{ds}
Dn-1 DATA VALID
Dn DATA VALID

Figure 1: Input Timing Diagram (LED or LCD)

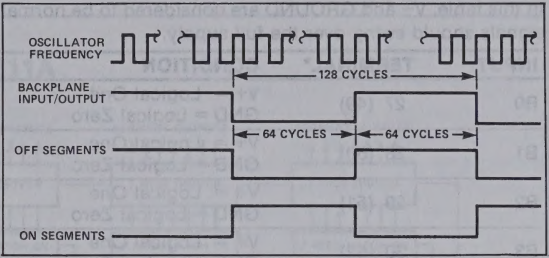

OSCILLATOR FREQUENCY
128 CYCLES
BACKPLANE INPUT/OUTPUT
64 CYCLES
64 CYCLES
OFF SEGMENTS
ON SEGMENTS

Figure 2: LCD Display Waveforms

Test Circuit

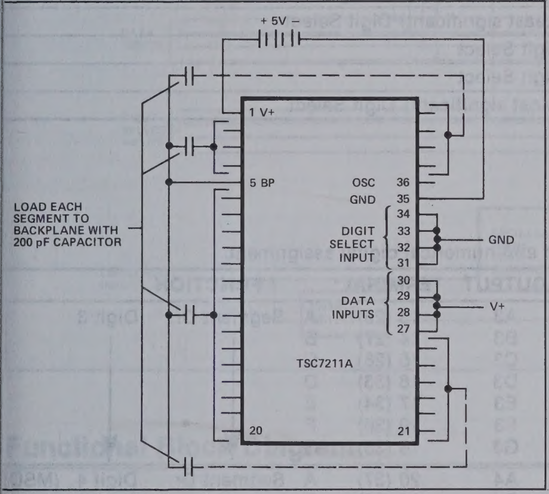
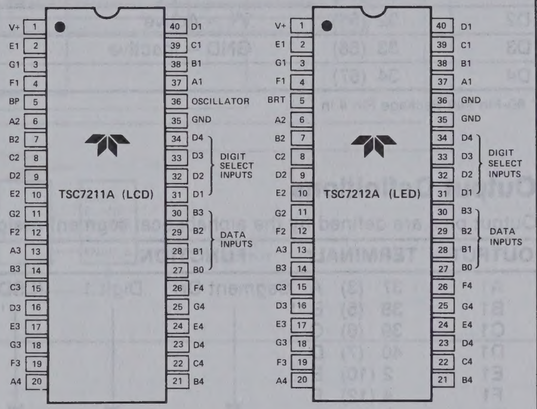

+ 5V –
1 V+
5 BP
OSC 36
GND 35
34
33
32
31
DIGIT SELECT INPUT
GND
30
29
28
27
DATA INPUTS
V+
TSC7211A
20
21
LOAD EACH SEGMENT TO BACKPLANE WITH 200 pF CAPACITOR

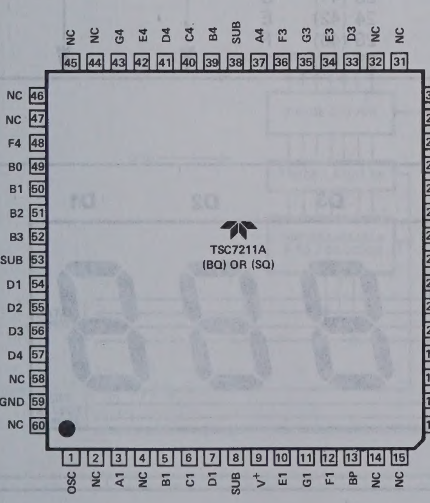
Figure 3: Test Circuit

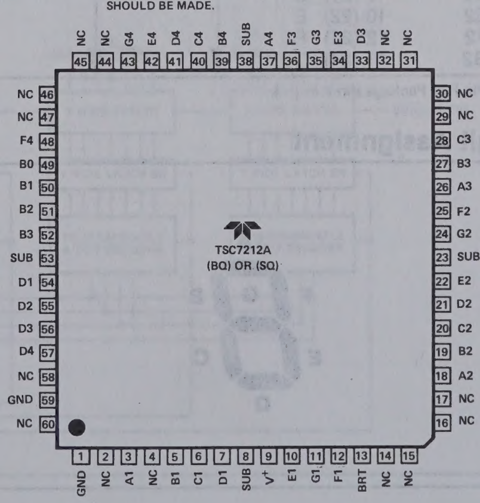
Pin Configuration


V+ 1
E1 2
G1 3
F1 4
BP 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
40 D1
39 C1
38 B1
37 A1
36 OSCILLATOR
35 GND
34 D4
33 D3
32 D2
31 D1
DIGIT SELECT INPUTS
30 B3
29 B2
28 B1
27 B0
DATA INPUTS
26 F4
25 G4
24 E4
23 D4
22 C4
21 B4
TSC7211A (LCD)
V+ 1
E1 2
G1 3
F1 4
BRT 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
40 D1
39 C1
38 B1
37 A1
36 GND
35 GND
34 D4
33 D3
32 D2
31 D1
DIGIT SELECT INPUTS
30 B3
29 B2
28 B1
27 B0
DATA INPUTS
26 F4
25 G4
24 E4
23 D4
22 C4
21 B4
TSC7212A (LED)

Flat Package

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.


NC 45
NC 44
G4 43
E4 42
D4 41
C4 40
B4 39
SUB 38
A4 37
F3 36
G3 35
E3 34
D3 33
NC 32
NC 31
NC 46
NC 47
F4 48
B0 49
B1 50
B2 51
B3 52
SUB 53
D1 54
D2 55
D3 56
D4 57
NC 58
GND 59
NC 60
30 NC
29 NC
28 C3
27 B3
26 A3
25 F2
24 G2
23 SUB
22 E2
21 D2
20 C2
19 B2
18 A2
17 NC
16 NC
TSC7211A (BQ) OR (SQ)
1 OSC
2 NC
3 A1
4 NC
5 B1
6 C1
7 D1
8 SUB
9 V+
10 E1
11 G1
12 F1
13 BP
14 NC
15 NC


NC 45
NC 44
G4 43
E4 42
D4 41
C4 40
B4 39
SUB 38
A4 37
F3 36
G3 35
E3 34
D3 33
NC 32
NC 31
NC 46
NC 47
F4 48
B0 49
B1 50
B2 51
B3 52
SUB 53
D1 54
D2 55
D3 56
D4 57
NC 58
GND 59
NC 60
30 NC
29 NC
28 C3
27 B3
26 A3
25 F2
24 G2
23 SUB
22 E2
21 D2
20 C2
19 B2
18 A2
17 NC
16 NC
TSC7212A (BQ) OR (SQ)
1 GND
2 NC
3 A1
4 NC
5 B1
6 C1
7 D1
8 SUB
9 V+
10 E1
11 G1
12 F1
13 BRT
14 NC
15 NC

Input Definitions

In this table, V+ and GROUND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL*	CONDITION	FUNCTION	
B0	27 (49)	V+ = Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28 (50)	V+ = Logical One GND = Logical Zero	Twos	
B2	29 (51)	V+ = Logical One GND = Logical Zero	Fours	
B3	30 (52)	V+ = Logical One GND = Logical Zero	Eights (Most Significant)	
OSC (LCD Devices only)	36 (1)	Floating or with external capacitor	Oscillator Input	
		GROUND	Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (Pin 5)	
D1	31 (54)		D1 (Least significant) Digit Select	
D2	32 (55)	V+ = Active	D2 Digit Select	
D3	33 (56)	GND = Inactive	D3 Digit Select	
D4	34 (57)		D4 (Most significant) Digit Select	

* 60-Pin Flat Package Pin # in ( ).

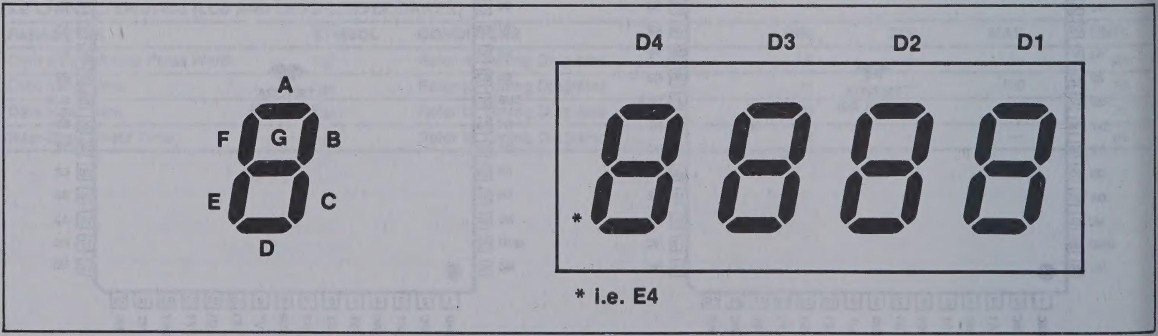
Output Definitions

Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

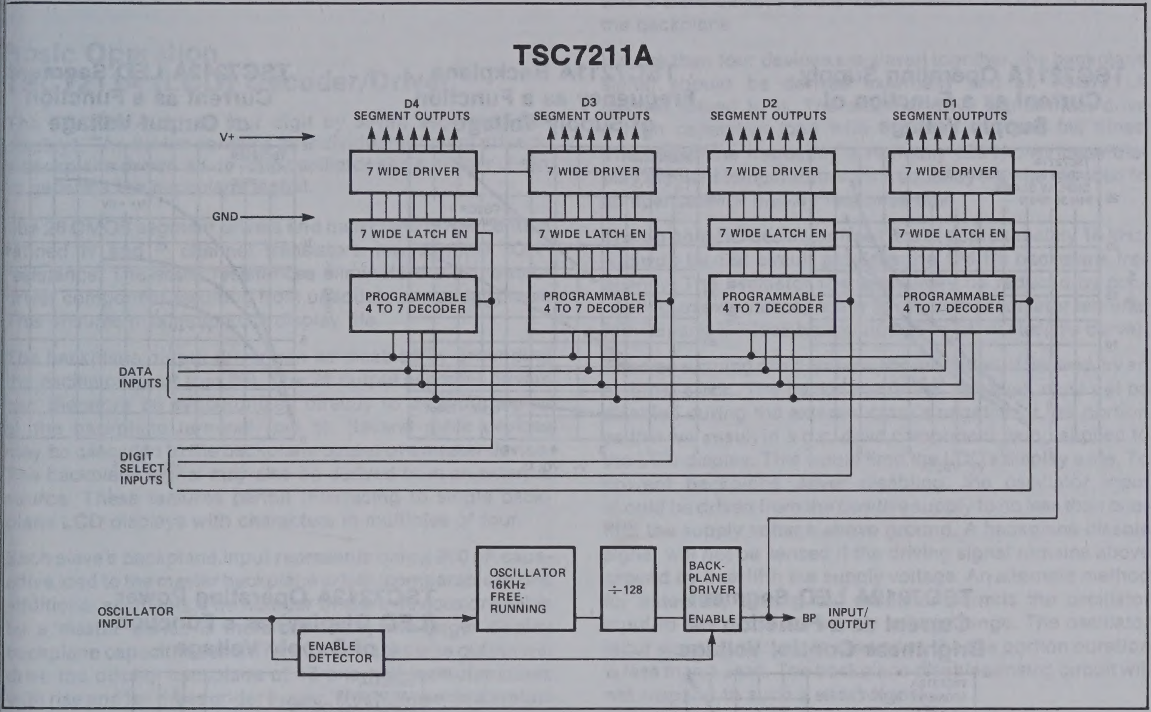
OUTPUT	TERMINAL*		FUNCTION	OUTPUT	TERMINAL*		FUNCTION
A1	37 (3)	A	Segment Dr. Digit 1 (LSD)	A3	13 (26)	A	Segment Dr. Digit 3
B1	38 (5)	B		B3	14 (27)	B	
C1	39 (6)	C		C3	15 (28)	C	
D1	40 (7)	D		D3	16 (33)	D	
E1	2 (10)	E		E3	17 (34)	E	
F1	4 (12)	F		F3	19 (36)	F	
G1	3 (11)	G		G3	18 (35)	G	
A2	6 (18)	A	Segment Dr. Digit 2	A4	20 (37)	A	Segment Dr. Digit 4 (MSD)
B2	7 (19)	B		B4	21 (39)	B	
C2	8 (20)	C		C4	22 (40)	C	
D2	9 (21)	D		D4	23 (41)	D	
E2	10 (22)	E		E4	24 (42)	E	
F2	12 (25)	F		F4	26 (48)	F	
G2	11 (24)	G		G4	25 (43)	G	

* 60-Pin Flat Package Pin # in ( ).

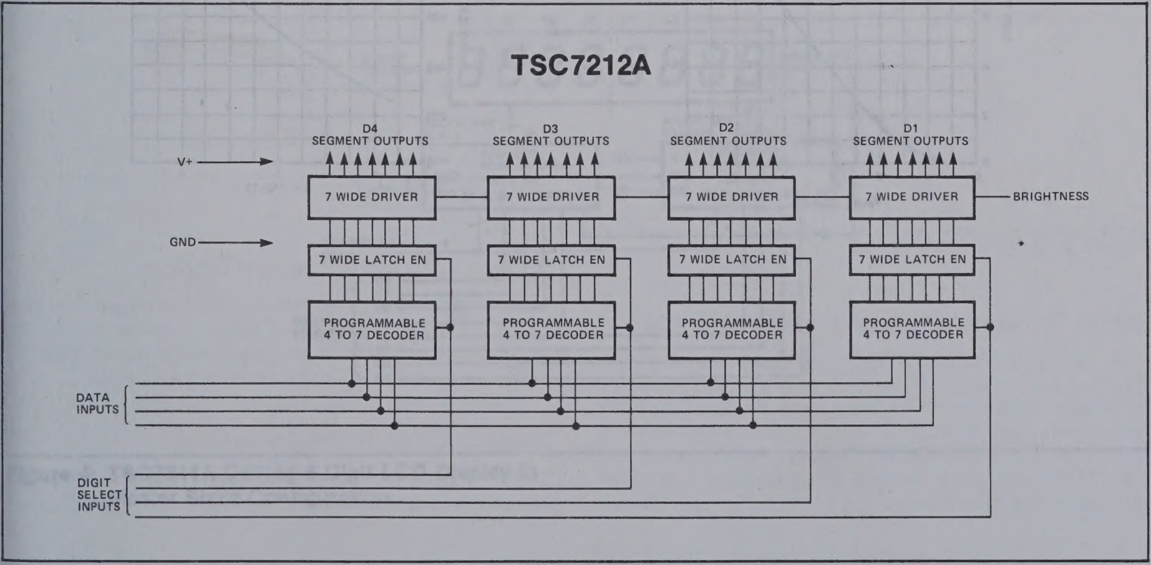
Digit Assignment



Functional Block Diagram

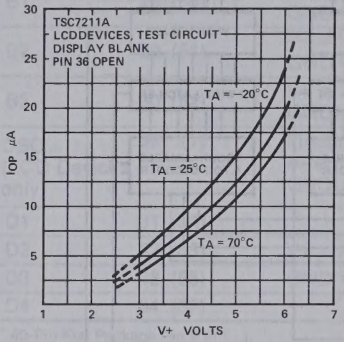

TSC7211A
D4 SEGMENT OUTPUTS
D3 SEGMENT OUTPUTS
D2 SEGMENT OUTPUTS
D1 SEGMENT OUTPUTS
V+
GND
7 WIDE DRIVER
7 WIDE LATCH EN
PROGRAMMABLE 4 TO 7 DECODER
DATA INPUTS
DIGIT SELECT INPUTS
OSCILLATOR INPUT
OSCILLATOR 16KHz FREE-RUNNING
÷128
BACK-PLANE DRIVER
ENABLE
ENABLE DETECTOR
BP
INPUT/ OUTPUT

Functional Block Diagram

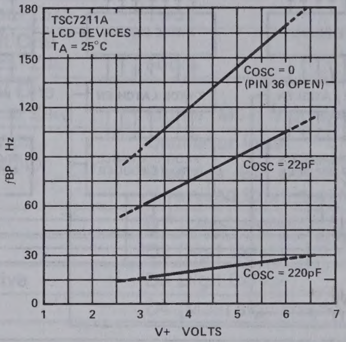

TSC7212A
D4 SEGMENT OUTPUTS
D3 SEGMENT OUTPUTS
D2 SEGMENT OUTPUTS
D1 SEGMENT OUTPUTS
V+
GND
7 WIDE DRIVER
BRIGHTNESS
7 WIDE LATCH EN
PROGRAMMABLE 4 TO 7 DECODER
DATA INPUTS
DIGIT SELECT INPUTS

Typical Operating Characteristics

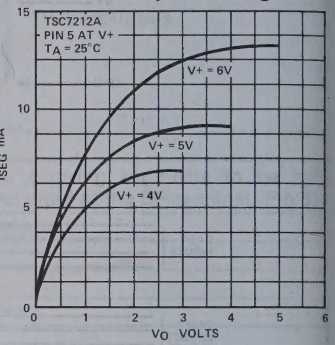
TSC7211A Operating Supply Current as a Function of Supply Voltage



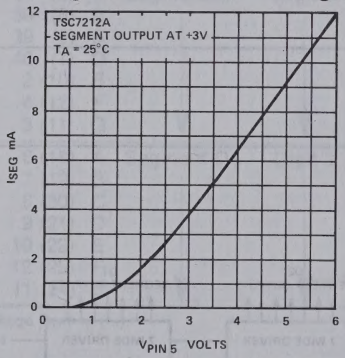
TSC7211A Backplane Frequency as a Function of Supply Voltage



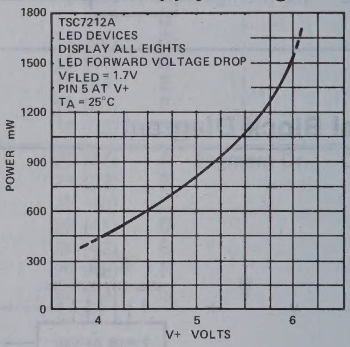
TSC7212A LED Segment Current as a Function of Output Voltage



TSC7212A LED Segment Current as a Function of Brightness Control Voltage



TSC7212A Operating Power (LED Display) as a Function of Supply Voltage



Basic Operation

Basic Operation TSC7211A (LCD) Decoder/Driver

The TSC7211A drives four digit by seven segment LCD displays. The device contains 28 individual segment drivers, a backplane driver, an on chip oscillator and a divider chain to generate the backplane signal.

The 28 CMOS segment drivers and backplane driver contain ratioed N and P channel transistors for identical "ON" resistance. The equal resistances eliminate the d.c. output driver component resulting from unequal rise and fall times. This ensures maximum LCD display life.

The backplane output driver can be disabled by grounding the oscillator input (pin 36). The 28 output segment drivers can therefore be synchronized directly to an input signal at the backplane terminal (pin 5). Several slave devices may be cascaded to the backplane output of a master device. The backplane signal may also be derived from an external source. These features permit interfacing to single backplane LCD displays with characters in multiples of four.

Each slave's backplane input represents only a 200 pF capacitive load to the master backplane driver (comparable to one additional segment). The number of slave devices driveable by a master device is therefore set by the larger display backplane capacitive load. The master backplane output will drive the display backplane of 16 one-half inch characters with rise and fall times under 5 µsec. This represents a system with 3 slave devices and a fourth master TSC7211A driving the backplane.

If more than four devices are slaved together, the backplane signal should be derived externally and all TSC7211A devices slaved to it. The external drive signal must drive a high capacitive load with 1-2 µsec rise and fall times. The backplane frequency is normally 125 Hz. At lower display ambient temperatures the frequency may be reduced to compensate for display response time.

The on chip RC oscillator free runs at approximately 16 kHz. A divide by 128 circuit provides the 125 Hz backplane frequency. The oscillator frequency may be reduced by connecting an external capacitor between the oscillator terminal (pin 36) and V+ (see typical operating characteristic curve).

The free running oscillator may be overriden, if desired, by an external clock. The backplane driver, however, must not be disabled during the external clock's negative or low portion as this will result in a d.c. drive component being applied to the LCD display. This would limit the LCD's display's life. To prevent backplane driver disabling, the oscillator input should be driven from the positive supply to no less than one-fifth the supply voltage above ground. A backplane disable signal will not be sensed if the driving signal remains above ground by one-fifth the supply voltage. An alternate method for externally driving the oscillator permits the oscillator input to swing the full supply voltage range. The oscillator input signal duty cycle is skewed so the low portion duration is less than 1 µsec. The backplane disable sensing circuit will not respond to such a short signal.

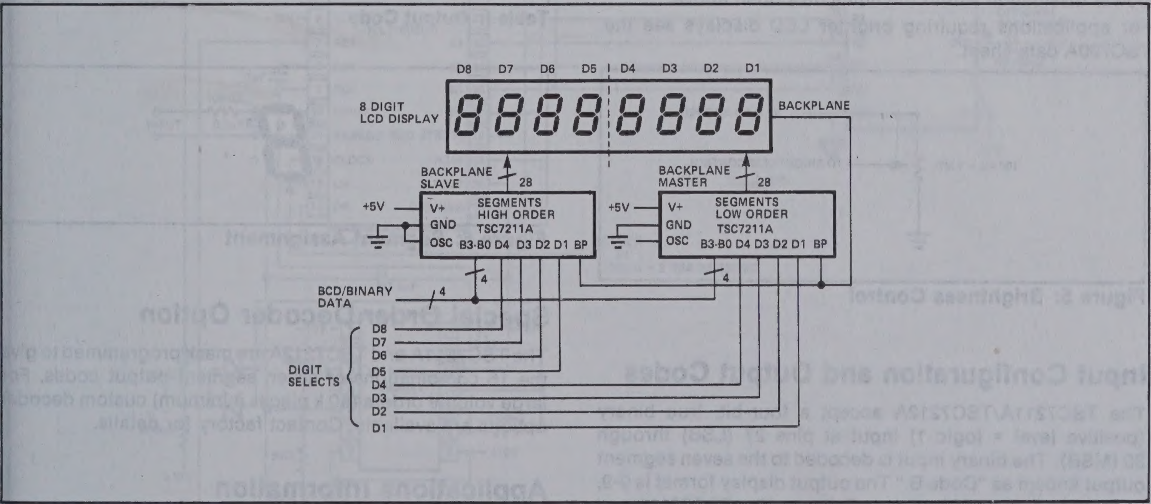


Figure 4: TSC7211A Driving 8 Digit LCD Display In Master Slave Configuration.

TSC7212A LED Decoder/Driver

The TSC7212A directly drives four digit, seven segment, common anode LED displays. The 28 segment drivers are low leakage, current controlled, open drain N-channel MOS transistors.

A brightness input (pin 5) can be used in two ways to control output transistor drain current. The voltage at the brightness control input is transferred to the output transistor gate for "ON" segments. The brightness voltage directly modulates the segment drivers "ON" resistance. A variable brightness control may be implemented with a single potentiometer (Figure 4). A high value potentiometer (100 kΩ to 1 mΩ) will minimize power consumption.

The brightness input may also be operated digitally as a display enable. At a logic 1 the display is fully "ON" and at a logic 0 fully "OFF." The display brightness may be controlled by a logic signal of varying duty cycle also. When operating with LEDs at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperature rise. The maximum power dissipation is 1 watt at 25°C. Derated linearly above 35°C to 500 mW at 70°C (-15 mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V^+ - V_{FLED})\ (I_{SEG})\ \ (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "ON" segments. If the device is operated at elevated temperatures, the segment current can be limited through the brightness input to keep power dissipation within the limits described above.

For applications requiring brighter LED displays see the TSC700A data sheet.

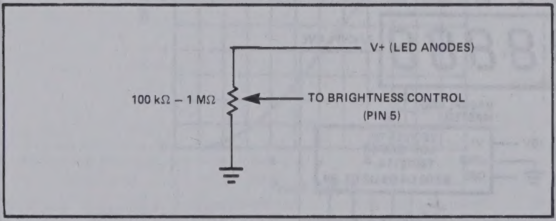


Figure 5: Brightness Control

Input Configuration and Output Codes

The TSC7211A/TSC7212A accept a four-bit, true binary (positive level = logic 1) input at pins 27 (LSB) through 30 (MSB). The binary input is decoded to the seven segment output known as "Code B." The output display format is 0-9, dash, E, H, L.,P and blank (see Table 1). The TSC7211A and TSC7212A will correctly decode binary and BCD true codes to a seven-segment output.

The TSC7211A/TSC7212A accept multiplexed binary or BCD input data at pins 27 (LSB) through pin 30 (MSB). Pins 31 (LSD) through 34 (MSD) are the digit select lines. When the digit select line is taken to a logic 1 level the input data is decoded and stored in the enabled output latch of the selected digit. More than one digit select line may be activated simultaneously. The same character will be written into all selected digits. See Figure 5 for decoder segment assignments.

BINARY INPUT				CODE B
B3	B2	B1	B0	TSC7211A TSC7212A
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	-
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

Table I: Output Code

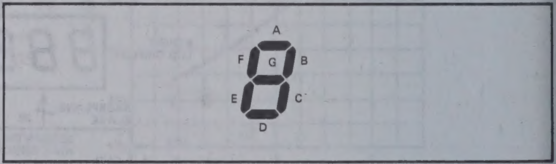


Figure 6: Segment Assignment

Special Order Decoder Option

The TSC7211A and TSC7212A are mask programmed to give the 16 combinations of seven segment output codes. For large volume orders (50 k pieces minimum) custom decoder options are available. Contact factory for details.

Applications Information

The TSC7212A has two ground pins. These pins should be connected together.

Applications Information (Continued)

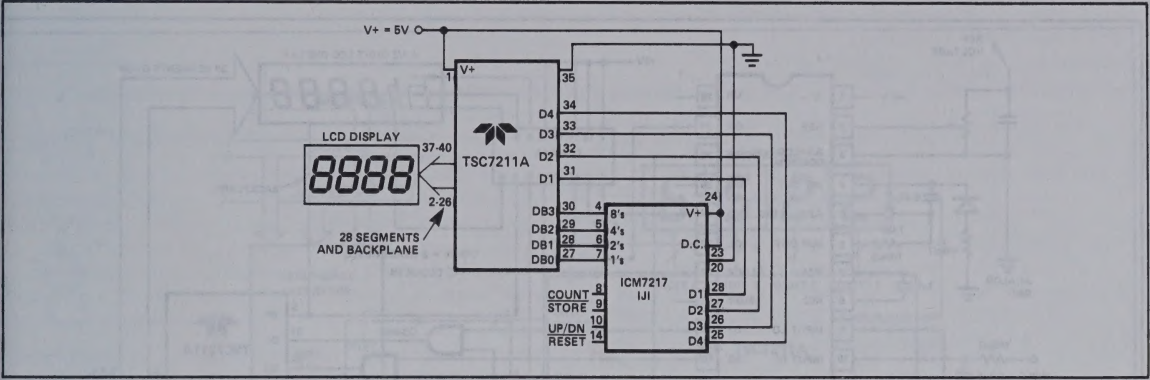

V+ = 5V
LCD DISPLAY
8888
37-40
2-26
28 SEGMENTS AND BACKPLANE
TSC7211A
V+
1
35
34
33
32
31
D4
D3
D2
D1
DB3
DB2
DB1
DB0
30
29
28
27
4
5
6
7
8's
4's
2's
1's
ICM7217 IJI
V+
24
D.C.
23
20
COUNT 8
STORE 9
UP/DN 10
RESET 14
D1 28
D2 27
D3 26
D4 25

Figure 7: LCD Display Interface to 4 Digit Counter

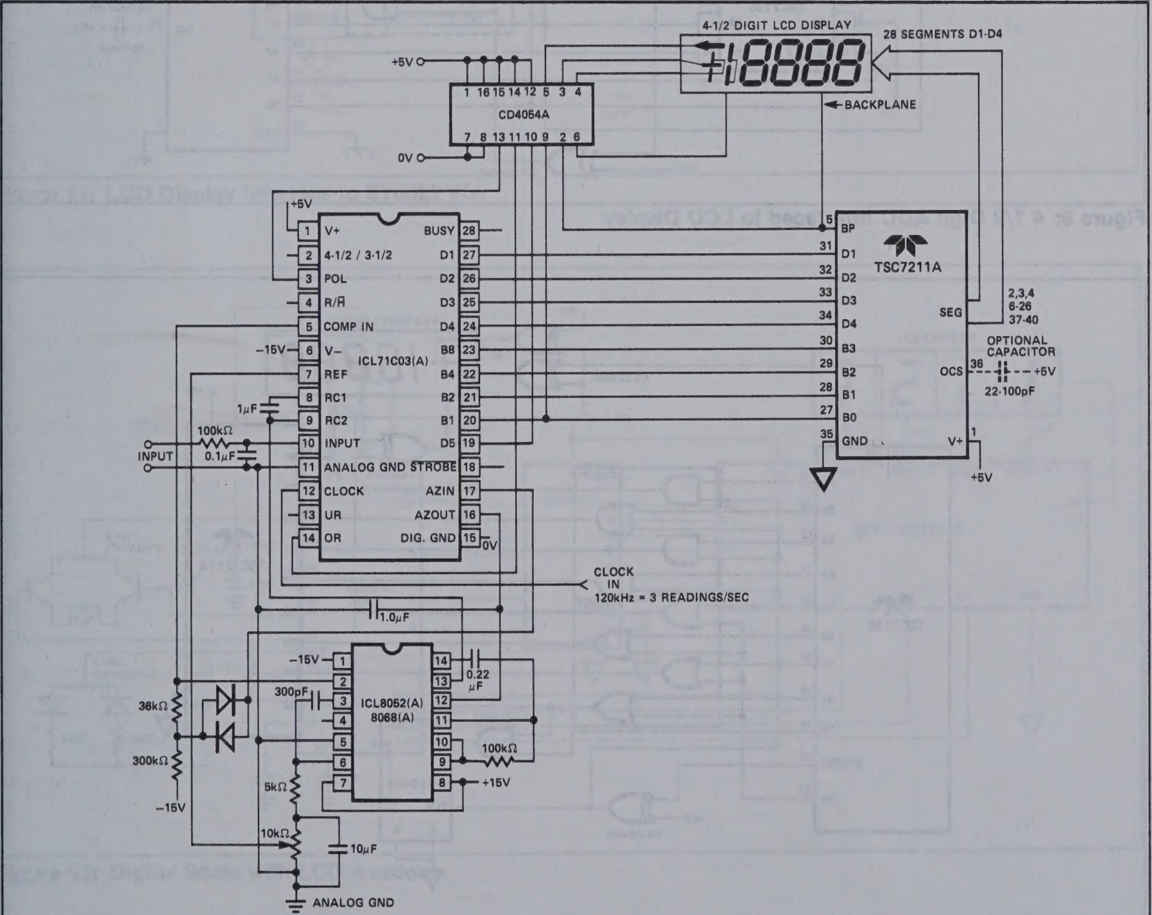

4-1/2 DIGIT LCD DISPLAY
28 SEGMENTS D1-D4
BACKPLANE
+5V
0V
CD4054A
1 16 15 14 12 5 3 4
7 8 13 11 10 9 2 6
+5V
ICL71C03(A)
1 V+
2 4-1/2 / 3-1/2
3 POL
4 R/H
5 COMP IN
6 V−
7 REF
8 RC1
9 RC2
10 INPUT
11 ANALOG GND
12 CLOCK
13 UR
14 OR
BUSY 28
D1 27
D2 26
D3 25
D4 24
B8 23
B4 22
B2 21
B1 20
D5 19
STROBE 18
AZIN 17
AZOUT 16
DIG. GND 15
0V
−15V
1µF
100kΩ
0.1µF
INPUT
CLOCK IN
120kHz = 3 READINGS/SEC
1.0µF
TSC7211A
5 BP
31 D1
32 D2
33 D3
34 D4
30 B3
29 B2
28 B1
27 B0
35 GND
SEG
2,3,4 6-26 37-40
OPTIONAL CAPACITOR
OCS 36
+5V
22-100pF
V+ 1
+5V
ICL8052(A) 8068(A)
−15V
300pF
0.22 µF
100kΩ
+15V
36kΩ
300kΩ
−15V
5kΩ
10kΩ
10µF
ANALOG GND

Figure 8: 4 1/2 Digit DPM Interfaced to LCD Display

Typical Applications

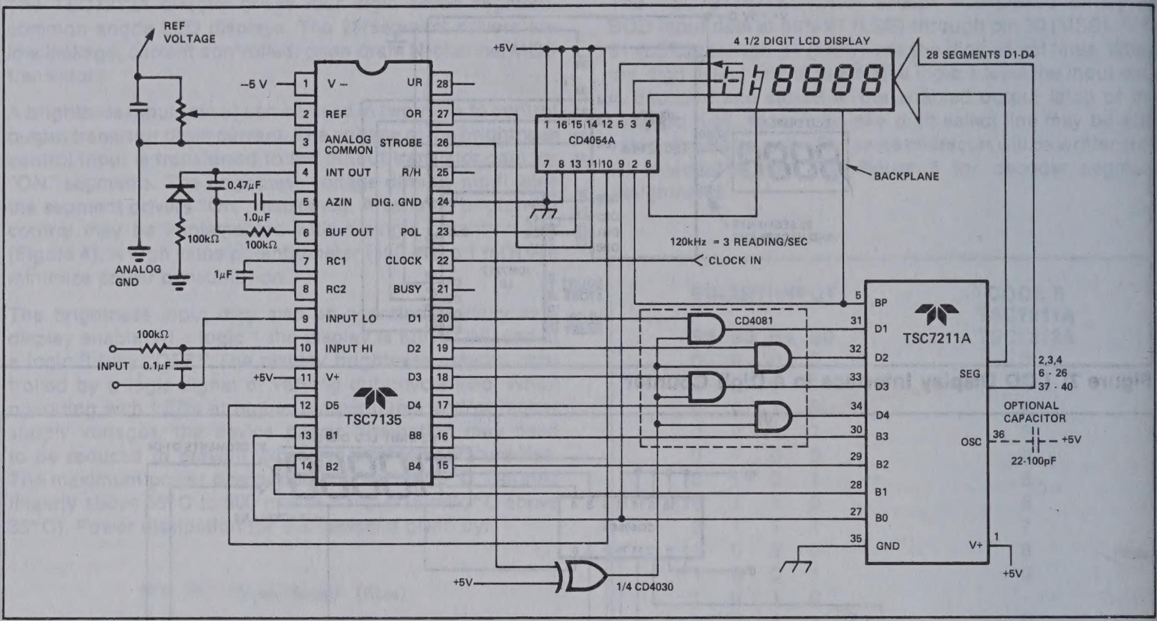

REF VOLTAGE
–5 V
1 V–
UR 28
2 REF
OR 27
3 ANALOG COMMON
STROBE 26
4 INT OUT
R/H 25
5 AZIN
DIG. GND 24
6 BUF OUT
POL 23
7 RC1
CLOCK 22
8 RC2
BUSY 21
9 INPUT LO
D1 20
10 INPUT HI
D2 19
11 V+
D3 18
12 D5
D4 17
13 B1
B8 16
14 B2
B4 15
TSC7135
0.47µF
1.0µF
100kΩ
100kΩ
1µF
ANALOG GND
100kΩ
INPUT
0.1µF
+5V
+5V
4 1/2 DIGIT LCD DISPLAY
28 SEGMENTS D1-D4
1 16 15 14 12 5 3 4
CD4054A
7 8 13 11 10 9 2 6
BACKPLANE
120kHz = 3 READING/SEC
CLOCK IN
CD4081
5 BP
31 D1
32 D2
33 D3
34 D4
30 B3
29 B2
28 B1
27 B0
35 GND
V+ 1
+5V
TSC7211A
SEG
2,3,4
6 - 26
37 - 40
OPTIONAL CAPACITOR
OSC 36
+5V
22-100pF
+5V
1/4 CD4030

Figure 9: 4 1/2 Digit ADC Interfaced to LCD Display

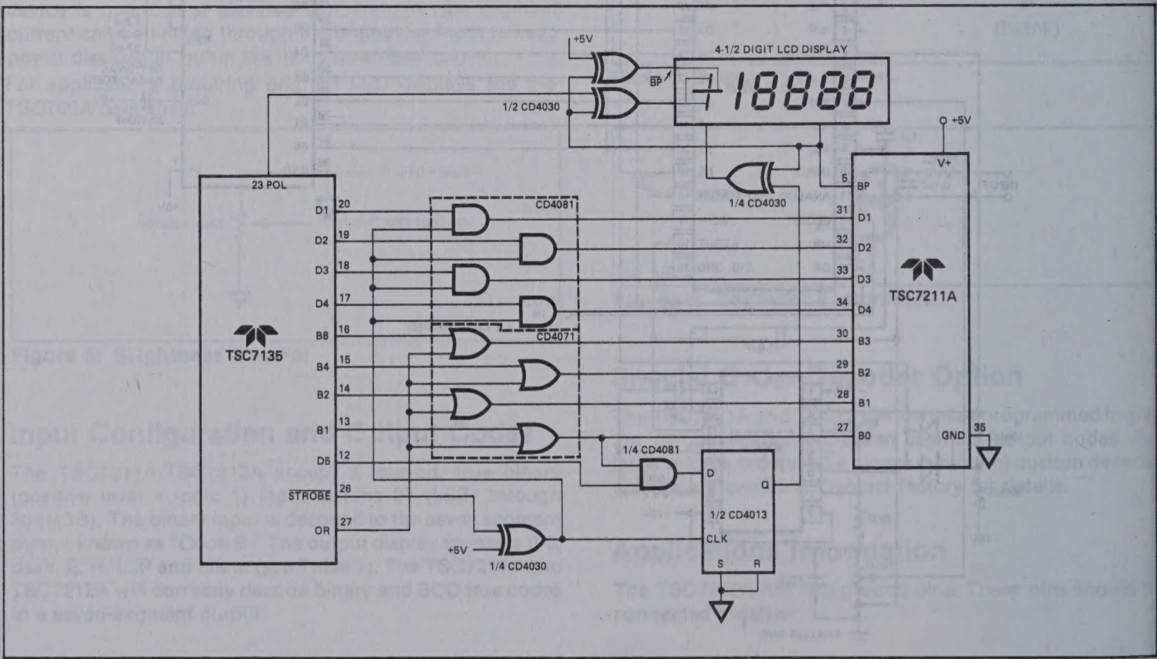

+5V
4-1/2 DIGIT LCD DISPLAY
BP
1/2 CD4030
+5V
V+
5 BP
1/4 CD4030
31 D1
32 D2
33 D3
34 D4
30 B3
29 B2
28 B1
27 B0
35 GND
TSC7211A
23 POL
D1 20
D2 19
D3 18
D4 17
B8 16
B4 15
B2 14
B1 13
D5 12
STROBE 26
OR 27
TSC7135
CD4081
CD4071
1/4 CD4081
D
Q
1/2 CD4013
CLK
S
R
+5V
1/4 CD4030

Figure 10: 4 1/2 Digit ADC Interfaced to LCD Display with Digit Blanking on Overrange

Typical Applications (continued)

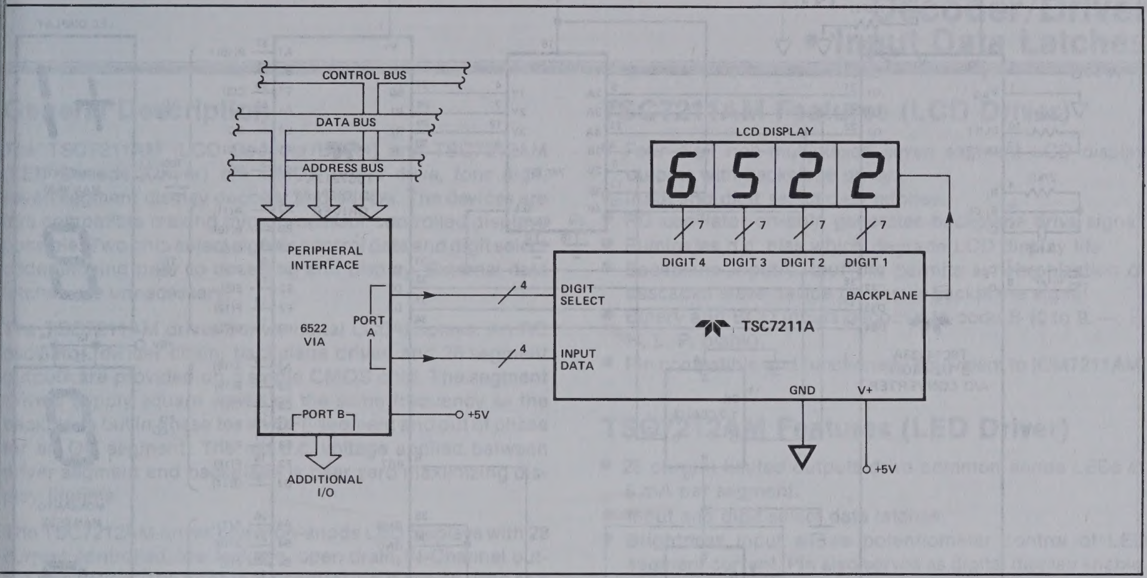

CONTROL BUS
DATA BUS
ADDRESS BUS
PERIPHERAL INTERFACE
6522 VIA
PORT A
PORT B
+5V
ADDITIONAL I/O
4
4
LCD DISPLAY
6522
7
7
7
7
DIGIT 4
DIGIT 3
DIGIT 2
DIGIT 1
DIGIT SELECT
INPUT DATA
BACKPLANE
TSC7211A
GND
V+
+5V

Figure 11: LCD Display Interface to SY6522 VIA

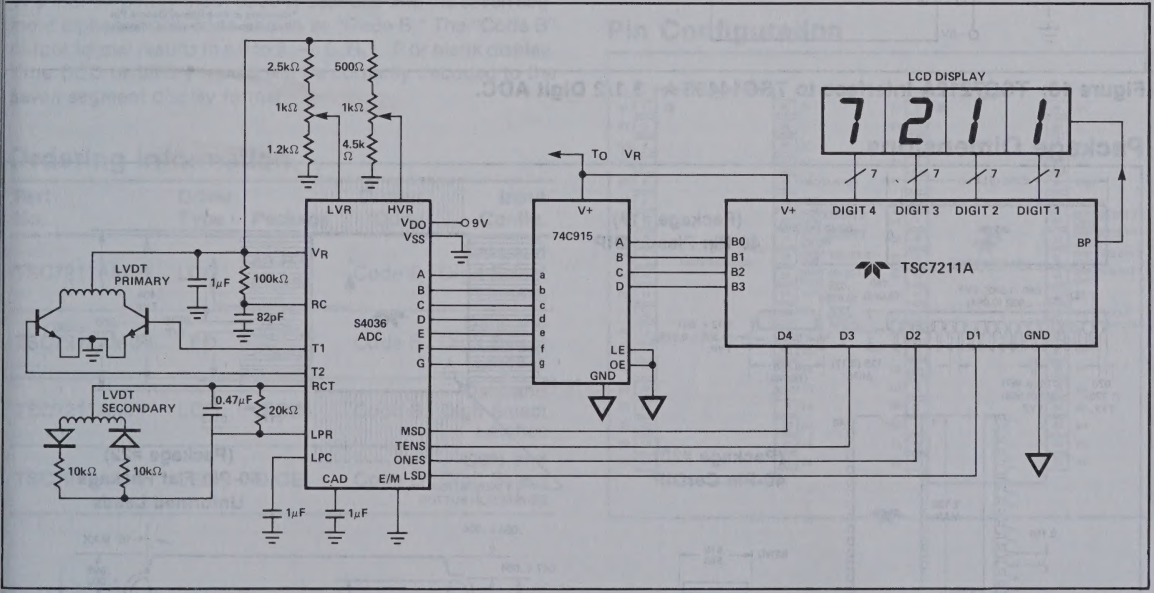

2.5kΩ
500Ω
1kΩ
1kΩ
1.2kΩ
4.5kΩ
LVDT PRIMARY
1μF
100kΩ
82pF
LVDT SECONDARY
0.47μF
20kΩ
10kΩ
10kΩ
1μF
1μF
LVR
HVR
VDD
VSS
9V
VR
RC
T1
T2
RCT
LPR
LPC
CAD
S4036 ADC
A
B
C
D
E
F
G
MSD
TENS
ONES
E/M
LSD
74C915
V+
A
B
C
D
a
b
c
d
e
f
g
LE
OE
GND
To VR
LCD DISPLAY
7211
7
7
7
7
V+
DIGIT 4
DIGIT 3
DIGIT 2
DIGIT 1
BP
B0
B1
B2
B3
TSC7211A
D4
D3
D2
D1
GND

Figure 12: Digital Scale with LCD Readout

Typical Applications (continued)

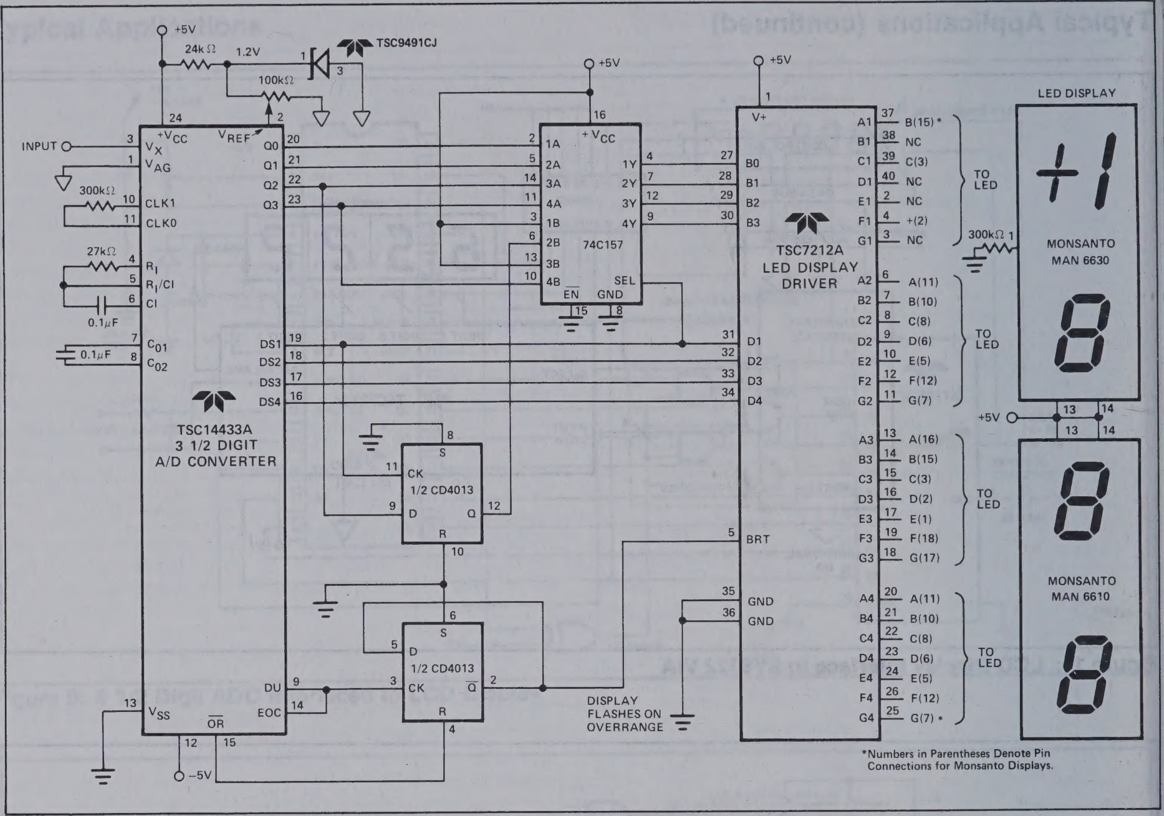
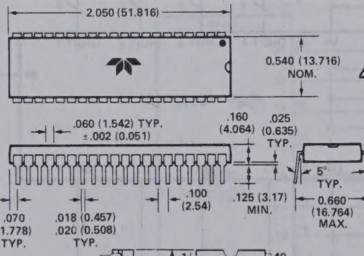
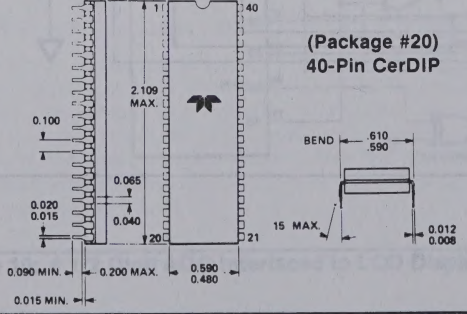

+5V
24kΩ
1.2V
TSC9491CJ
100kΩ
+5V
+5V
INPUT
300kΩ
27kΩ
0.1μF
0.1μF
V_X
V_{AG}
CLK1
CLK0
R_I
R_I/CI
CI
C_{01}
C_{02}
$+V_{CC}$
V_{REF}
Q0
Q1
Q2
Q3
DS1
DS2
DS3
DS4
TSC14433A
3 1/2 DIGIT
A/D CONVERTER
DU
EOC
V_{SS}
$\overline{OR}$
−5V
1A
2A
3A
4A
1B
2B
3B
4B
$+V_{CC}$
1Y
2Y
3Y
4Y
74C157
EN
SEL
GND
S
CK
1/2 CD4013
D
Q
R
S
D
1/2 CD4013
CK
$\overline{Q}$
R
DISPLAY
FLASHES ON
OVERRANGE
V+
B0
B1
B2
B3
D1
D2
D3
D4
BRT
GND
GND
TSC7212A
LED DISPLAY
DRIVER
A1
B1
C1
D1
E1
F1
G1
A2
B2
C2
D2
E2
F2
G2
A3
B3
C3
D3
E3
F3
G3
A4
B4
C4
D4
E4
F4
G4
B(15)*
NC
C(3)
NC
NC
+(2)
NC
A(11)
B(10)
C(8)
D(6)
E(5)
F(12)
G(7)
A(16)
B(15)
C(3)
D(2)
E(1)
F(18)
G(17)
A(11)
B(10)
C(8)
D(6)
E(5)
F(12)
G(7)*
TO LED
TO LED
TO LED
TO LED
300kΩ
LED DISPLAY
MONSANTO
MAN 6630
+5V
MONSANTO
MAN 6610
*Numbers in Parentheses Denote Pin Connections for Monsanto Displays.

Figure 13: TSC7212A Interface to TSC14433 A 3 1/2 Digit ADC.

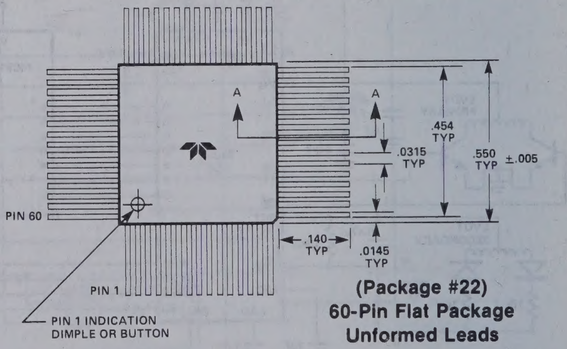
Package Dimensions


2.050 (51.816)
0.540 (13.716) NOM.
.060 (1.542) TYP. ±.002 (0.051)
.160 (4.064)
.025 (0.635) TYP.
5° TYP.
.012 ± .001 (0.305 ± 0.025) TYP.
.070 (1.778) TYP.
.018 (0.457) .020 (0.508) TYP.
.100 (2.54)
.125 (3.17) MIN.
0.660 (16.764) MAX.

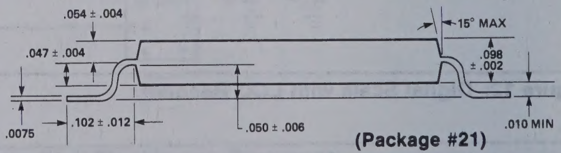
(Package #17)
40-Pin Plastic DIP


1
40
2.109 MAX.
0.100
0.065
0.020
0.015
0.040
20
21
0.090 MIN.
0.200 MAX.
0.590
0.480
0.015 MIN.
BEND
.610
.590
15 MAX.
0.012
0.008

(Package #20)
40-Pin CerDIP


A
A
.454 TYP
.0315 TYP
.550 TYP ±.005
PIN 60
PIN 1
.140 TYP
.0145 TYP
PIN 1 INDICATION
DIMPLE OR BUTTON

(Package #22)
60-Pin Flat Package
Unformed Leads


.054 ± .004
15° MAX
.047 ± .004
.098 ± .002
.0075
.102 ± .012
.050 ± .006
.010 MIN

(Package #21)
60-Pin Flat Package
Formed Leads

TELEDYNE SEMICONDUCTOR

TSC7211AM (LCD)
TSC7212AM (LED)
BUS Compatible Four Digit CMOS Decoder/Driver
• Input Data Latches

General Description

The TSC7211AM (LCD Decoder/Driver) and TSC7212AM (LED Decoder/Driver) are CMOS direct drive, four digit, seven segment display decoder and drivers. The devices are bus compatible making microprocessor controlled displays possible. Two chip select signals control data and digit select code latching prior to decoding and display. External data latches are unnecessary.

The TSC7211AM drives conventional LCD displays. An RC oscillator, divider chain, backplane driver, and 28 segment outputs are provided on a single CMOS chip. The segment drivers supply square waves of the same frequency as the backplane but in phase for an OFF segment and out of phase for an ON segment. The net d.c. voltage applied between driver segment and backplane is near zero maximizing display lifetime.

The TSC7212AM drives common-anode LED displays with 28 current controlled, low leakage, open drain, N-Channel output transistors. The brightness control input can be used as a digital display enable. A varying voltage at the control input will allow continuous display brightness control.

The four bit binary input code is decoded into the seven segment alphanumeric code known as "Code B." The "Code B" output format results in a 0 to 9, —, E, H, L, P or blank display. True BCD or binary inputs will be correctly decoded to the seven segment display format.

Ordering Information

Part No.	Driver Type	Package	Output Code	Input Config.
TSC7211AMIPL	LCD	40-Pin Plastic	Code B	Data and Digit Select Latches
TSC7212AMIPL	LED	40-Pin Plastic	Code B	Data and Digit Select Latches
TSC7211AM/Y	LCD	DICE	Code B	Data and Digit Select Latches
TSC7212AM/Y	LED	DICE	Code B	Data and Digit Select Latches

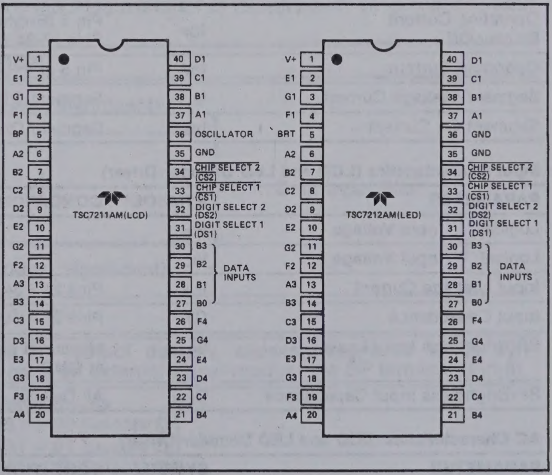
TSC7211AM Features (LCD Driver)

- Four digit non-multiplexed seven segment LCD display outputs with backplane driver.
- Input and digit select data latches.
- RC oscillator on-chip generates backplane drive signal.
- Eliminates d.c. bias which degrade LCD display life.
- Backplane input/output pin permits synchronization of cascaded slave device to master backplane signal.
- Binary and BCD inputs decoded to code B (0 to 9, —, E, H, L, P, blank).
- Pin compatible and functionally equivalent to ICM7211AM.

TSC7212AM Features (LED Driver)

- 28 current limited outputs drive common-anode LEDs at 8 mA per segment.
- Input and digit select data latches.
- Brightness input allows potentiometer control of LED segment current. Pin also serves as digital display enable.
- Same input configuration and output decoding as the TSC7211AM.
- Pin compatible and functionally equivalent to ICM7212AM.

Pin Configuration


TSC7211AM(LCD)
V+ 1
E1 2
G1 3
F1 4
BP 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
40 D1
39 C1
38 B1
37 A1
36 OSCILLATOR
35 GND
34 CHIP SELECT 2 (CS2)
33 CHIP SELECT 1 (CS1)
32 DIGIT SELECT 2 (DS2)
31 DIGIT SELECT 1 (DS1)
30 B3
29 B2
28 B1
27 B0
DATA INPUTS
26 F4
25 G4
24 E4
23 D4
22 C4
21 B4
TSC7212AM(LED)
V+ 1
E1 2
G1 3
F1 4
BRT 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
40 D1
39 C1
38 B1
37 A1
36 GND
35 GND
34 CHIP SELECT 2 (CS2)
33 CHIP SELECT 1 (CS1)
32 DIGIT SELECT 2 (DS2)
31 DIGIT SELECT 1 (DS1)
30 B3
29 B2
28 B1
27 B0
DATA INPUTS
26 F4
25 G4
24 E4
23 D4
22 C4
21 B4

© 1983

TSC7211AM (LCD)
TSC7212AM (LED)

BUS Compatible Four Digit CMOS Display Decoder/Driver
• Input Data Latches

Absolute Maximum Ratings

Power Dissipation (Note 1) .... 1.0 W at 70°C
Supply Voltage .... 6.5 V
Input Voltage (Any
Terminal) (Note 2) .... V⁺ +0.3 V, GROUND -0.3 V
Operating Temperature Range .... -20°C to +85°C
Storage Temperature Range .... -55°C to +125°C
Lead Temperature (Soldering 10 sec.) .... 300°C

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This limit refers to that of the package and will not be realized during normal operation.

Note 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V⁺ or less than GROUND may cause destructive device latchup. For this reason it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the TSC7211AM/TSC7212AM be turned on first.

Table I: Operating Characteristics

Test Conditions: All parameters measured with V+ = 5 V.

TSC7211AM Characteristics (LCD Decoder/Driver)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{OP}	Display Blank	—	10	50	µA
Oscillator Input Current	I_{OSCI}	Pin 36	—	±2	±10	µA
Segment Rise/Fall Time	t_{RFS}	C_L = 200 pF	—	0.5	—	µA
Backplane Rise/Fall Time	t_{RFB}	C_L = 5000 pF	—	1.5	—	µs
Oscillator Frequency	f_{OSC}	Pin 36 Floating	—	16	—	kHz
Backplane Frequency	f_{BP}	Pin 36 Floating	—	125	—	Hz

TSC7212AM Characteristics (Common-Anode LED Decoder/Driver)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{OP}	Pin 5 (Brightness), Pins 27-34 = GROUND	—	10	50	µA
Operating Current	I_{OP}	Pin 5 at V+, Display all 8's	—	200	—	mA
Segment Leakage Current	I_{SLK}	Segment Off	—	±0.01	±1	µA
Segment On Current	I_{SEG}	Segment On, V_O = +3 V	5	8	—	mA

Input Characteristics (LCD and LED Decoder/Driver)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" Input Voltage	V_{IH}		3	—	—	V
Logical "0" Input Voltage	V_{IL}		—	—	1	V
Input Leakage Current	I_{ILK}	Pins 27 - 34	—	±0.01	±1	µA
Input Capacitance	C_{IN}	Pins 27 - 34	—	5	—	pF
BP/Brightness Input Leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND	—	±0.01	±1	µA
BP/Brightness Input Capacitance	C_{BPI}	All Devices	—	200	—	pF

AC Characteristics (LCD and LED Decoder/Driver)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Chip Select Active Pulse Width	t_{CSA}	Note 1	200	—	—	ns
Data Setup Time	t_{DS}		100	—	—	ns
Data Hold Time	t_{DH}		10	0	—	ns
Inter-Chip Select Time	t_{ICS}		2	—	—	µs

Note:
1. Other Chip Select $(\overline{CS})$ is either held at logic zero or both $\overline{CS1}$ and $\overline{CS2}$ driven together.

Timing Diagrams

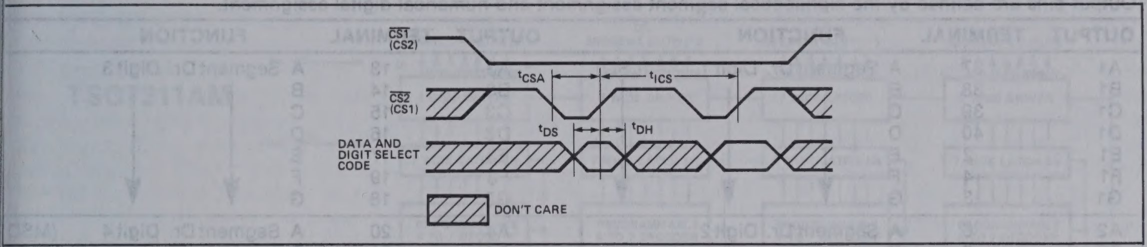

$\overline{CS1}$ ($\overline{CS2}$)
t_{CSA}
t_{ICS}
$\overline{CS2}$ ($\overline{CS1}$)
t_{DS}
t_{DH}
DATA AND DIGIT SELECT CODE
▨ DON'T CARE

Figure 1: BUS Interface Timing Diagram (LED or LCD)

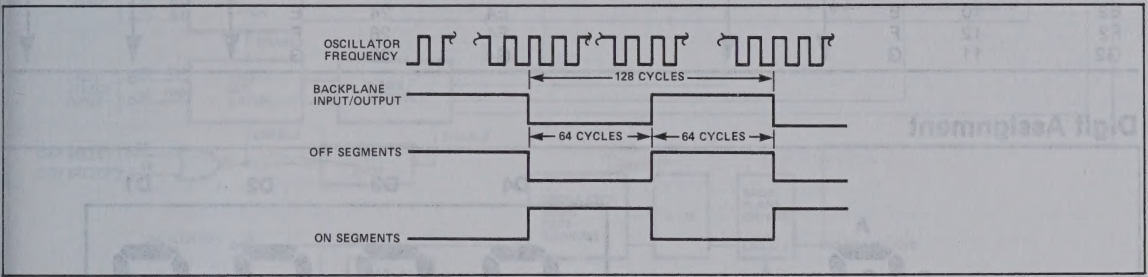

OSCILLATOR FREQUENCY
128 CYCLES
BACKPLANE INPUT/OUTPUT
64 CYCLES
64 CYCLES
OFF SEGMENTS
ON SEGMENTS

Figure 2: LCD Display Waveforms

Input Definitions

In this table, V + and GROUND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

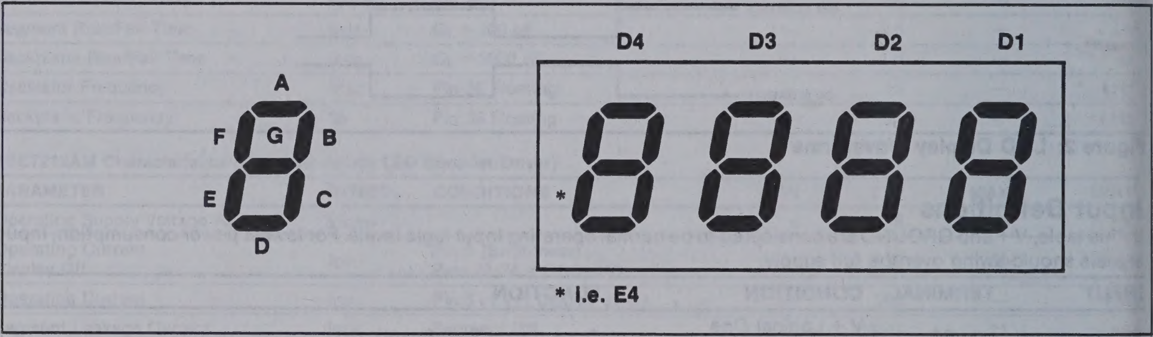
INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V + Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V+ = Logical One GND = Logical Zero	Twos	
B2	29	V+ = Logical One GND = Logical Zero	Fours	
B3	30	V+ = Logical One GND = Logical Zero	Eights (Most Significant)	
OSC (LCD Devices only)	36	Floating or with external capacitor	Oscillator Input	
		GROUND	Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (Pin 5)	
DS1	31	V+ = Logical One	Digit Select Inputs DS2, DS1 = 00 Selects D4 DS2, DS1 = 01 Selects D3 DS2, DS1 = 10 Selects D2 DS2, DS1 = 11 Selects D1	
DS2	32	GND = Logical Zero		
$\overline{CS1}$	33	V+ = Inactive	When both $\overline{CS1}$ and $\overline{CS2}$ are low the data and digit select input latches are open or enabled. On the rising of $\overline{CS1}$ or $\overline{CS2}$ data is latched, decoded and stored in the output drive latches.	
$\overline{CS2}$	34	GND = Active		

Output Definitions

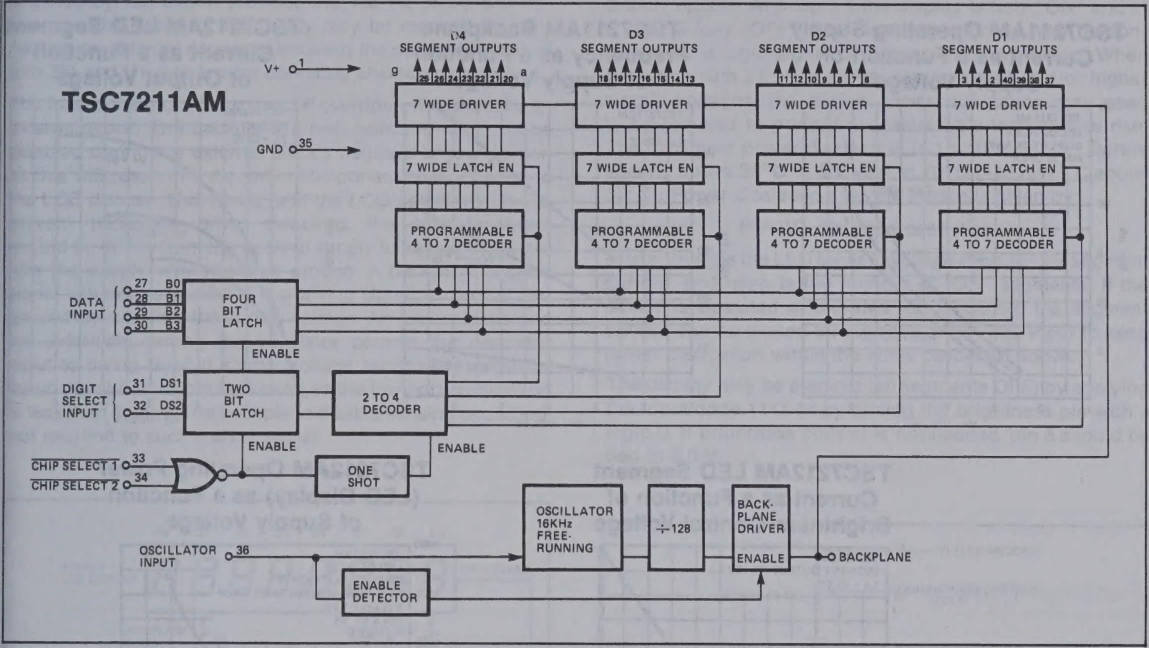
Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

OUTPUT	TERMINAL	FUNCTION	OUTPUT	TERMINAL	FUNCTION
A1	37	A Segment Dr. Digit 1 (LSD)	A3	13	A Segment Dr. Digit 3
B1	38	B	B3	14	B
C1	39	C	C3	15	C
D1	40	D	D3	16	D
E1	2	E	E3	17	E
F1	4	F	F3	19	F
G1	3	G	G3	18	G
A2	6	A Segment Dr. Digit 2	A4	20	A Segment Dr. Digit 4 (MSD)
B2	7	B	B4	21	B
C2	8	C	C4	22	C
D2	9	D	D4	23	D
E2	10	E	E4	24	E
F2	12	F	F4	26	F
G2	11	G	G4	25	G

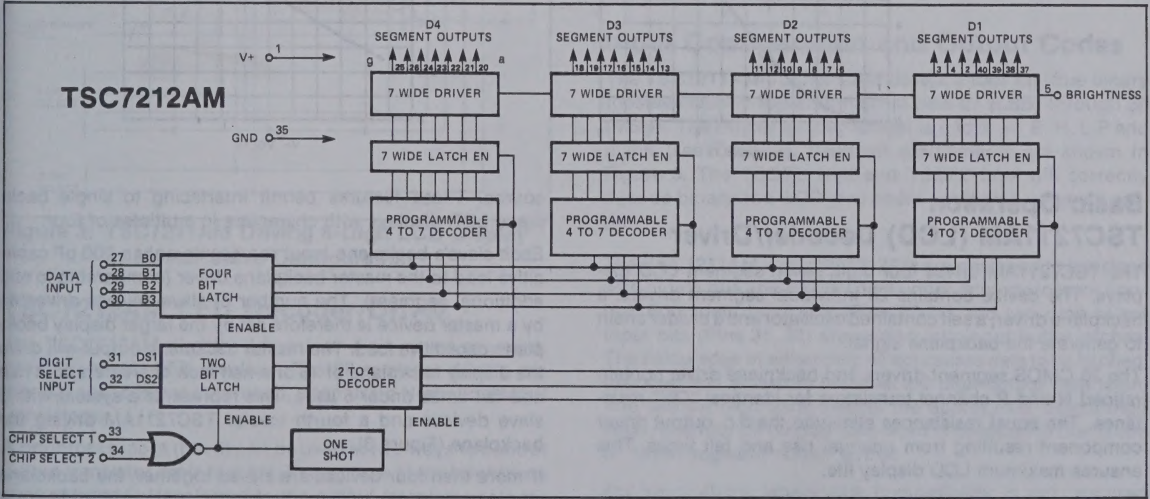
Digit Assignment



Functional Block Diagram

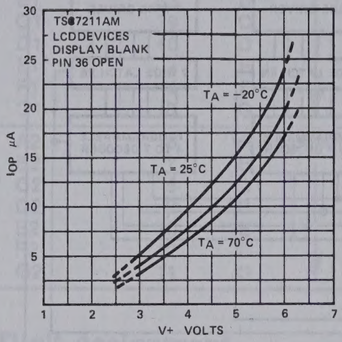

TSC7211AM
V+ 1
GND 35
D4 SEGMENT OUTPUTS
g a
25 26 24 23 22 21 20
D3 SEGMENT OUTPUTS
18 19 17 16 15 14 13
D2 SEGMENT OUTPUTS
11 12 10 9 8 7 6
D1 SEGMENT OUTPUTS
3 4 2 40 39 38 37
7 WIDE DRIVER
7 WIDE LATCH EN
PROGRAMMABLE 4 TO 7 DECODER
DATA INPUT
27 B0
28 B1
29 B2
30 B3
FOUR BIT LATCH
ENABLE
DIGIT SELECT INPUT
31 DS1
32 DS2
TWO BIT LATCH
ENABLE
2 TO 4 DECODER
ENABLE
CHIP SELECT 1 33
CHIP SELECT 2 34
ONE SHOT
OSCILLATOR INPUT 36
OSCILLATOR 16KHz FREE-RUNNING
÷128
BACK-PLANE DRIVER
ENABLE
5 BACKPLANE
ENABLE DETECTOR

Functional Block Diagram

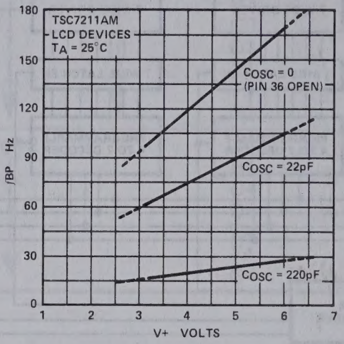

TSC7212AM
V+ 1
GND 35
D4 SEGMENT OUTPUTS
g a
25 26 24 23 22 21 20
D3 SEGMENT OUTPUTS
18 19 17 16 15 14 13
D2 SEGMENT OUTPUTS
11 12 10 9 8 7 6
D1 SEGMENT OUTPUTS
3 4 2 40 39 38 37
7 WIDE DRIVER
5 BRIGHTNESS
7 WIDE LATCH EN
PROGRAMMABLE 4 TO 7 DECODER
DATA INPUT
27 B0
28 B1
29 B2
30 B3
FOUR BIT LATCH
ENABLE
DIGIT SELECT INPUT
31 DS1
32 DS2
TWO BIT LATCH
ENABLE
2 TO 4 DECODER
ENABLE
CHIP SELECT 1 33
CHIP SELECT 2 34
ONE SHOT

Typical Operating Characteristics

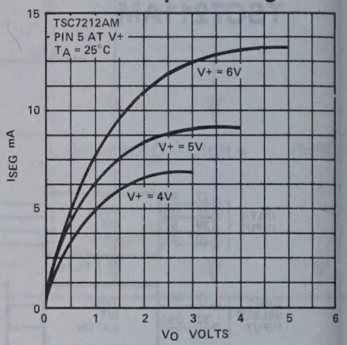
TSC7211AM Operating Supply Current as a Function of Supply Voltage



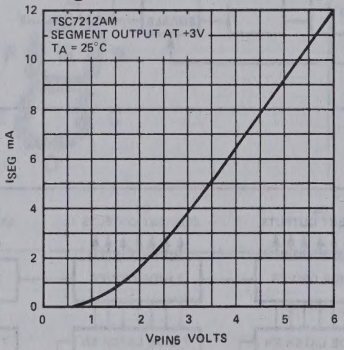
TSC7211AM Backplane Frequency as a Function of Supply Voltage



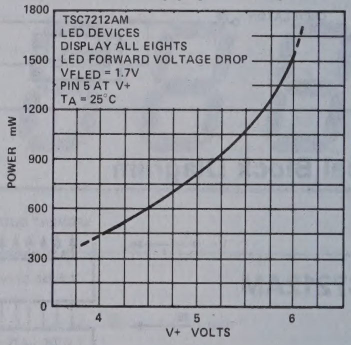
TSC7212AM LED Segment Current as a Function of Output Voltage



TSC7212AM LED Segment Current as a Function of Brightness Control Voltage



TSC7212AM Operating Power (LED Display) as a Function of Supply Voltage



Basic Operation
TSC7211AM (LCD) Decoder/Driver

The TSC7211AM drives four digit, seven segment LCD displays. The device contains 28 individual segment drivers, a backplane driver, a self contained oscillator and a divider chain to generate the backplane signal.

The 28 CMOS segment drivers and backplane driver contain ratioed N and P channel transistors for identical "ON" resistance. The equal resistances eliminate the d.c. output driver component resulting from unequal rise and fall times. This ensures maximum LCD display life.

The backplane output driver can be disabled by grounding the oscillator input (pin 36). The 28 output segment drivers can therefore be synchronized directly to an input signal at the backplane terminal (pin 5). Several slave devices may be cascaded to the backplane output of a master device. The backplane signal may also be derived from an external source. These features permit interfacing to single backplane LCD displays with characters in multiples of four.

Each slave's backplane input represents only a 200 pF capacitive load to the master backplane driver (comparable to one additional segment). The number of slave devices driveable by a master device is therefore set by the larger display backplane capacitive load. The master backplane output will drive the display backplane of 16 one-half inch characters with rise and fall times under 5 µsec. This represents a system with 3 slave devices and a fourth master TSC7211AM driving the backplane (Figure 3).

If more than four devices are slaved together, the backplane signal should be derived externally and all TSC7211AM devices slaved to it. The external drive signal must drive a high capacitive load with 1-2 µsec rise and fall times. The backplane frequency is normally 125 Hz. At lower display ambient temperatures the frequency may be reduced to compensate for display response time.

The on chip RC oscillator free runs at approximately 16 kHz. A divide by 128 circuit provides the 125 Hz backplane frequency. The oscillator frequency may be reduced by connecting an external capacitor between the oscillator terminal (pin 36) and V+ (see typical operating characteristic curve).

The free running oscillator may be overriden, if desired, by an external clock. The backplane driver, however, must not be disabled during the external clock's negative or low portion as this will result in a d.c. drive component being applied to the LCD display. This would limit the LCD's display's life. To prevent backplane driver disabling, the oscillator input should be driven from the positive supply to no less than one-fifth the supply voltage above ground. A backplane disable signal will not be sensed if the driving signal remains above ground by one-fifth the supply voltage. An alternate method for externally driving the oscillator permits the oscillator input to swing the full supply voltage range. The oscillator input signal duty cycle is skewed so the low portion duration is less than 1 μsec. The backplane disable sensing circuit will not respond to such a short signal.

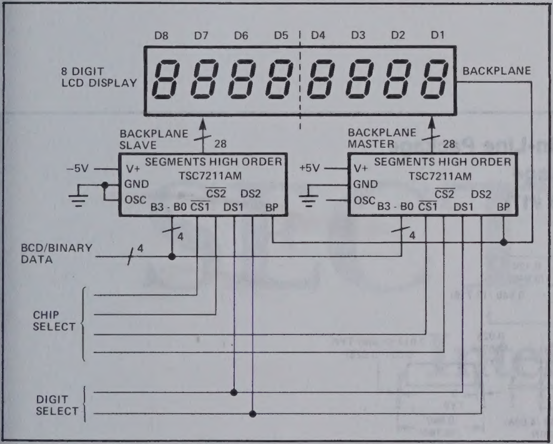


Figure 3: TSC7211AM Driving 8-Digit LCD Display in Master Slave Configuration.

TSC7212AM LED Decoder/Driver

The TSC7212AM directly drives four digit, seven segment, common-anode LED displays. The 28 segment drivers are low leakage, current controlled, open drain N-channel MOS transistors.

A brightness input (pin 5) can be used in two ways to control output transistor drain current. The voltage at the brightness control input is transferred to the output transistor gate for "ON" segments. The brightness voltage directly modulates the segment drivers "ON" resistance. A variable brightness control may be implemented with a single potentiometer (Figure 4). A high value potentiometer (100 kΩ to 1 MΩ) will minimize power consumption.

The brightness input may also be operated digitally as a display enable. At a logic 1 the display is fully "ON" and at a logic 0 fully "OFF." The display brightness may be controlled by a logic signal of varying duty cycle also. When operating with LEDs at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperature rise. The maximum power dissipation is 1 watt at 25°C. Derate linearly above 35°C to 500 mW at 70°C (-15 mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V^{+} - V_{FLED})\,(I_{SEG})\,(n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "ON" segments. If the device is operated at elevated temperatures, the segment current can be limited through the brightness input to keep power dissipation within the limits described above.

The display may be blanked (all segments OFF) by applying the input code 1111 or by driving the brightness pin with a logic 0. If brightness control is not needed, pin 5 should be tied to 5.0 V.

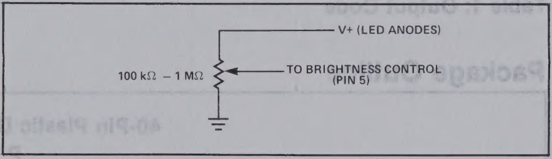


Figure 4: Brightness Control

Input Configuration and Output Codes

The TSC7211AM/TSC7212AM accept a four bit, true binary (positive level = logic 1) input at pins 27 (LSB) through 30 (MSB). The output display format is 0 to 9, —, E, H, L,P and blank (see Table 1). Segment assignments are shown in Figure 5. The TSC7211AM and TSC7212AM will correctly decode binary and BCD true codes to a seven segment output.

The TSC7211AM and TSC7212AM are designed to interface with a data bus and display data under microprocessor control. Four data input bits (Pins 27-30) and two digit select input bits (Pins 31, 32) are written into input buffer latches. The rising edge of either chip select causes data to be latched, decoded and stored in the selected digit output data latch. The two bit digit code selects the appropriate output digit latch. The four bit display data word is decoded to the "Code B" seven segment output format.

For applications where bus compatibility is not required refer to the TSC7211A (LCD), TSC7212A (LED) and TSC700A (LED) four digit decoder driver data sheets. These devices are designed to accept multiplexed BCD/Binary input data for display under the control of four separate digit select control signals.

BINARY INPUT				CODE B TSC7211AM TSC7212AM
B3	**B2**	**B1**	**B0**	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	—
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

Table 1: Output Code

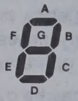


Figure 5: Segment Assignment

Special Order Decoder Option

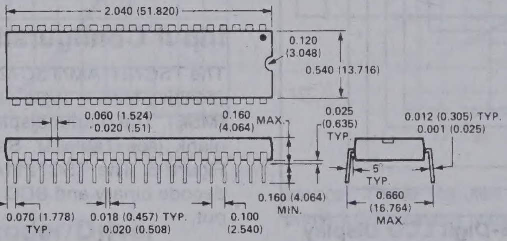
The TSC7211AM and TSC7212AM are mask programmed to give the 16 seven segment output codes. For large volume orders (25 k pieces minimum) custom decoder options are available. Contact factory for details.

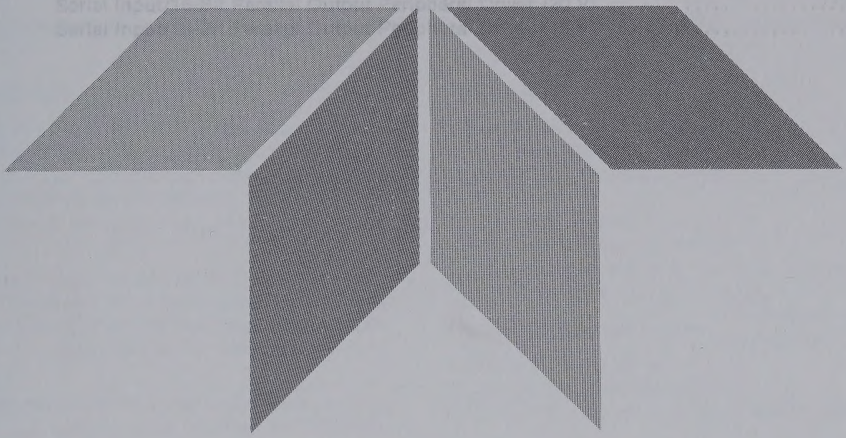
Applications Information

The TSC7212AM has two ground pins. These pins should be connected together.

Package Outline

40-Pin Plastic Dual-In-Line Package
P Package
(Package #17)


2.040 (51.820)
0.120
(3.048)
0.540 (13.716)
0.060 (1.524)
0.020 (.51)
0.160
(4.064)
MAX.
0.025
(0.635)
TYP.
0.012 (0.305) TYP.
0.001 (0.025)
5°
TYP.
0.160 (4.064)
MIN.
0.660
(16.764)
MAX.
0.070 (1.778)
TYP.
0.018 (0.457) TYP.
0.020 (0.508)
0.100
(2.540)



SECTION 11

Interface ICs

Section 11

Interface ICs 11-3

TSC426/427/428 Dual High Speed Power MOSFET Driver 11-5
TSC450 Dual Power MOSFET Driver 11-15
TSC7660 DC to DC Voltage Converter 11-19
TSC9403 Serial Input/16-Bit Parallel Output Peripheral Driver (20 V) 11-31
TSC9404 Serial Input/16-Bit Parallel Output Peripheral Driver (15 V) 11-31

TELEDYNE
SEMICONDUCTOR

TSC426/427/428
Dual Power MOSFET Driver
• 30 ns Rise Time
• Low Power CMOS

ieneral Description

he TSC426/427/428 are dual CMOS high speed drivers. TTL/CMOS input voltage level is translated into an output oltage level swing equalling the supply. The CMOS output ill be within 25 mV of ground or positive supply. Bipolar esigns are capable of swinging only within 1 volt of the upply.

he low impedance high current driver outputs will swing a 000 pf load 18 V in 30 ns. The unique current and voltage rive qualities make the TSC426/427/428 ideal power MOS-ET drivers, line drivers and DC to DC converter building locks.

nput logic signals may equal the power supply voltage. Input urrent is a low 1 μA making direct interface to CMOS/BI-POLAR switch mode power supply control integrated cir-uits possible as well as open collector analog comparators.

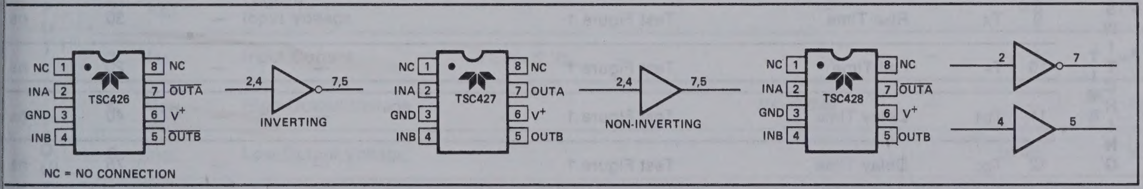
uiescent power supply current is 8 mA maximum. The SC426 requires 1/5 the current of the pin compatible bipolar S0026 device. This is important in DC to DC converter pplications with power efficiency constraints and high fre-uency switch mode power supply applications. Quiescent current is typically 6 mA when driving a 1000 pf load 18 V at 100 kHz.

The inverting TSC426 driver is pin compatible with the bipolar DS0026 and MMH0026 devices. The TSC427 is non-inverting; the TSC428 contains an inverting and non-inverting driver.

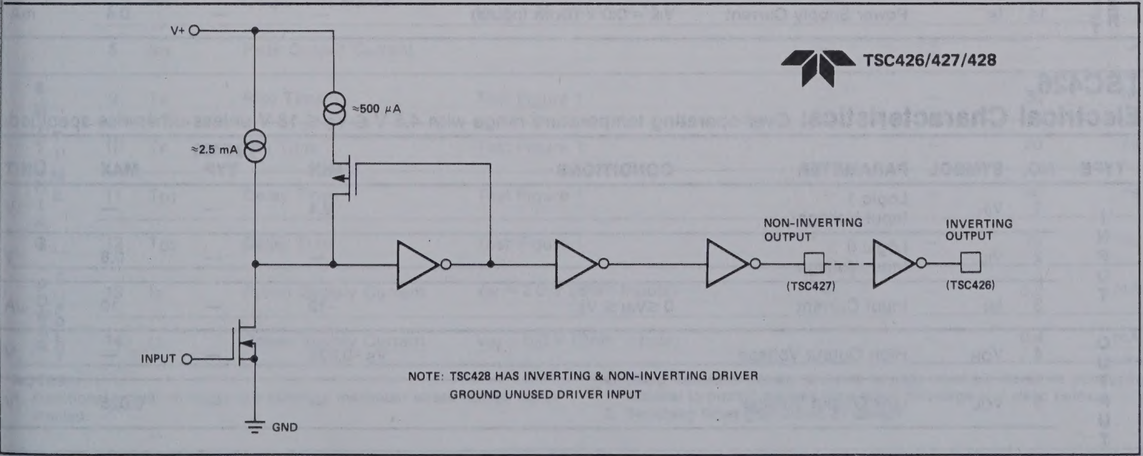
Features

- High Speed Switching (C_H = 1000 pf) .... 30 ns
- High Peak Output Current .... 1.5 A
- High Output Voltage Swing .... V_S - 25 mV
  GND + 25 mV
- Low Input Current (Logic "0" or "1") .... 1 μA
- TTL/CMOS Input Compatible
- Available in Inverting & Non-Inverting Configurations
- Wide Operating Supply Voltage .... 4.5 V to 18 V
- Low Power Consumption (Inputs Low) .... 0.4 mA
  (Inputs High) .... 8 mA
- Single Supply Operation
- Low Output Impedance .... 6 Ω
- Pin Out Equivalent to DS0026 & MMH0026

ʼin Configuration (See Ordering Information on Page 4)


NC 1
INA 2
GND 3
INB 4
8 NC
7 OUTA
6 V+
5 OUTB
TSC426
2,4
7,5
INVERTING
NC 1
INA 2
GND 3
INB 4
8 NC
7 OUTA
6 V+
5 OUTB
TSC427
2,4
7,5
NON-INVERTING
NC 1
INA 2
GND 3
INB 4
8 NC
7 OUTA
6 V+
5 OUTB
TSC428
2
7
4
5
NC = NO CONNECTION

ʼunctional Diagram


V+
≈500 μA
≈2.5 mA
INPUT
GND
TSC426/427/428
NON-INVERTING OUTPUT
(TSC427)
INVERTING OUTPUT
(TSC426)
NOTE: TSC428 HAS INVERTING & NON-INVERTING DRIVER
GROUND UNUSED DRIVER INPUT

©1984

Absolute Maximum Ratings (Notes 1, 2, 3)

Power Dissipation	
Plastic	500 mW
CerDIP	800 mW
Derating Factors	
Plastic	5.6 mW/° C Above 36° C
CerDIP	6.0 mW/° C
Supply Voltage	20 V
Input Voltage Any Terminal	Vs + 0.3 V to Ground -0.3 V
Operating Temperature	
M Version	-55° C to +125° C
I Version	-25° C to +85° C
C Version	0° C to +70° C
Maximum Chip Temperature	+150° C
Storage Temperature	-55° C to +150° C
Lead Temperature (10 Sec)	300° C

TSC426
Electrical Characteristics: $T_A = 25°$ C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC426 MIN	 TYP	 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	-1	—	1	μA
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	V_{IN} = 0.8 V I_{OUT} = 10 mA, V_S = 18 V	—	10	15	Ω
	7	R_O	Output Resistance	V_{IN} = 2.4 V I_{OUT} = 10 mA, V_S = 18 V	—	6	10	Ω
	8	I_{PK}	Peak Output Current		—	1.5	—	A
SWITCHING TIME	9	T_R	Rise Time	Test Figure 1	—	—	30	ns
	10	T_F	Fall Time	Test Figure 1	—	—	20	ns
	11	T_{D1}	Delay Time	Test Figure 1	—	—	40	ns
	12	T_{D2}	Delay Time	Test Figure 1	—	—	75	ns
POWER SUPPLY	13	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	8.0	mA
	14	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.4	mA

TSC426
Electrical Characteristics: Over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC426 MIN	 TYP	 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	-10	—	10	μA
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V

TSC426

Electrical Characteristics: Over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

						TSC426		
TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT	6	R_O	Output Resistance	$V_{IN} = 0.8$ V $I_{OUT} = 10$ mA, $V_S = 18$ V	—	13	20	Ω
	7	R_O	Output Resistance	$V_{IN} = 2.4$ V $I_{OUT} = 10$ mA, $V_S = 18$ V	—	8	15	Ω
SWITCHING TIME	8	T_R	Rise Time	Test Figure 1	—	—	60	ns
	9	T_F	Fall Time	Test Figure 1	—	—	40	ns
	10	T_{D1}	Delay Time	Test Figure 1	—	—	60	ns
	11	T_{D2}	Delay Time	Test Figure 1	—	—	120	ns
POWER SUPPLY	12	I_S	Power Supply Current	$V_{IN} = 3.0$ V (Both Inputs)	—	—	12.0	mA
	13	I_S	Power Supply Current	$V_{IN} = 0.0$ V (Both Inputs)	—	—	0.6	mA

TSC427

Electrical Characteristics: $T_A = 25°C$ with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

						TSC427		
TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	$0 \le V_{IN} \le V_S$	-1	—	1	μA
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	$V_{IN} = 2.4$ V $I_{OUT} = 10$ mA, $V_S = 18$ V	—	10	15	Ω
	7	R_O	Output Resistance	$V_{IN} = 0.8$ V $I_{OUT} = 10$ mA, $V_S = 18$ V	—	6	10	Ω
	8	I_{PK}	Peak Output Current		—	1.5	—	A
SWITCHING TIME	9	T_R	Rise Time	Test Figure 1	—	—	30	ns
	10	T_F	Fall Time	Test Figure 1	—	—	20	ns
	11	T_{D1}	Delay Time	Test Figure 1	—	—	40	ns
	12	T_{D2}	Delay Time	Test Figure 1	—	—	75	ns
POWER SUPPLY	13	I_S	Power Supply Current	$V_{IN} = 3.0$ V (Both Inputs)	—	—	8.0	mA
	14	I_S	Power Supply Current	$V_{IN} = 0.0$ V (Both Inputs)	—	—	0.4	mA

NOTES:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

TSC427

Electrical Characteristics: Over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	MIN	TSC427 TYP	MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	-10	—	10	μA
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	V_{IN} = 2.4 V I_{OUT} = 10 mA, V_S = 18 V	—	13	20	Ω
	7	R_O	Output Resistance	V_{IN} = 0.8 V I_{OUT} = 10 mA, V_S = 18 V	—	8	15	Ω
SWITCHING TIME	8	T_R	Rise Time	Test Figure 1	—	—	60	ns
	9	T_F	Fall Time	Test Figure 1	—	—	40	ns
	10	T_{D1}	Delay Time	Test Figure 1	—	—	60	ns
	11	T_{D2}	Delay Time	Test Figure 1	—	—	120	ns
POWER SUPPLY	12	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	12.0	mA
	13	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.6	mA

TSC428

Electrical Characteristics: T_A = 25° C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	MIN	TSC428 TYP	MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	-1	—	1	μA
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	Output High I_{OUT} = 10 mA, V_S = 18 V	—	10	15	Ω
	7	R_O	Output Resistance	Output Low I_{OUT} = 10 mA, V_S = 18 V	—	6	10	Ω
	8	I_{PK}	Peak Output Current		—	1.5	—	A

NOTES:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

TSC428

Electrical Characteristics: $T_A = 25°C$ with $4.5 V \le V_S \le 18 V$ unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC428 MIN	TSC428 TYP	TSC428 MAX	UNIT
SWITCHING TIME	9	T_R	Rise Time	Test Figure 1	—	—	30	ns
	10	T_F	Fall Time	Test Figure 1	—	—	20	ns
	11	T_{D1}	Delay Time	Test Figure 1	—	—	40	ns
	12	T_{D2}	Delay Time	Test Figure 1	—	—	75	ns
POWER SUPPLY	13	I_S	Power Supply Current	$V_{IN} = 3.0 V$ (Both Inputs)	—	—	8.0	mA
	14	I_S	Power Supply Current	$V_{IN} = 0.0 V$ (Both Inputs)	—	—	0.4	mA

TSC428

Electrical Characteristics: Over operating temperature range with $4.5 V \le V_S \le 18 V$ unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC428 MIN	TSC428 TYP	TSC428 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	$0 \le V_{IN} \le V_S$	-10	—	10	µA
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	Output High $I_{OUT} = 10 mA$, $V_S = 18 V$	—	13	20	Ω
	7	R_O	Output Resistance	Output Low $I_{OUT} = 10 mA$, $V_S = 18 V$	—	8	15	Ω
SWITCHING TIME	8	T_R	Rise Time	Test Figure 1	—	—	60	ns
	9	T_F	Fall Time	Test Figure 1	—	—	40	ns
	10	T_{D1}	Delay Time	Test Figure 1	—	—	60	ns
	11	T_{D2}	Delay Time	Test Figure 1	—	—	120	ns
POWER SUPPLY	12	I_S	Power Supply Current	$V_{IN} = 3.0 V$ (Both Inputs)	—	—	12.0	mA
	13	I_S	Power Supply Current	$V_{IN} = 0.0 V$ (Both Inputs)	—	—	0.6	mA

NOTES:

1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

Ordering Information

Part No.	Package	Configuration	Temperature Range
TSC426CPA	8-Pin Plastic Dip	Inverting	0° C to +70° C
TSC426IJA*	8-Pin CerDIP	Inverting	-25° C to +85° C
TSC426MJA*	8-Pin CerDIP	Inverting	-55° C to +125° C
TSC427CPA	8-Pin Plastic Dip	Non-Inverting	0° C to +70° C
TSC427IJA*	8-Pin CerDIP	Non-Inverting	-25° C to +85° C
TSC427MJA*	8-Pin CerDIP	Non-Inverting	-55° C to +125° C
TSC428CPA	8-Pin Plastic Dip	Non-Inv. & Inv.	0° C to +70° C
TSC428IJA*	8-Pin CerDIP	Non-Inv. & Inv.	-25° C to +85° C
TSC428MJA*	8-Pin CerDIP	Non-Inv. & Inv.	-55° C to +125° C
TSC426C/Y	CHIP	Inverting	25° C
TSC427C/Y	CHIP	Non-Inverting	25° C
TSC428C/Y	CHIP	Non-Inv. & Inv.	25° C

* For devices with 125° C, 160 Hour Burn In add /BI to part number suffix.

Switching Time Test Circuits

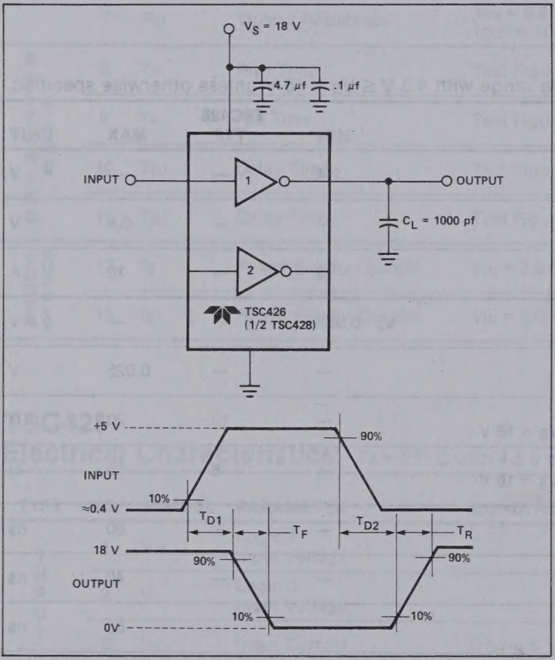

V_S = 18 V
4.7 µf
.1 µf
INPUT
1
2
OUTPUT
C_L = 1000 pf
TSC426
(1/2 TSC428)
+5 V
90%
INPUT
10%
≈0.4 V
T_{D1}
T_F
T_{D2}
T_R
18 V
90%
OUTPUT
90%
10%
10%
0V

Figure 1: Inverting Driver Switching Time

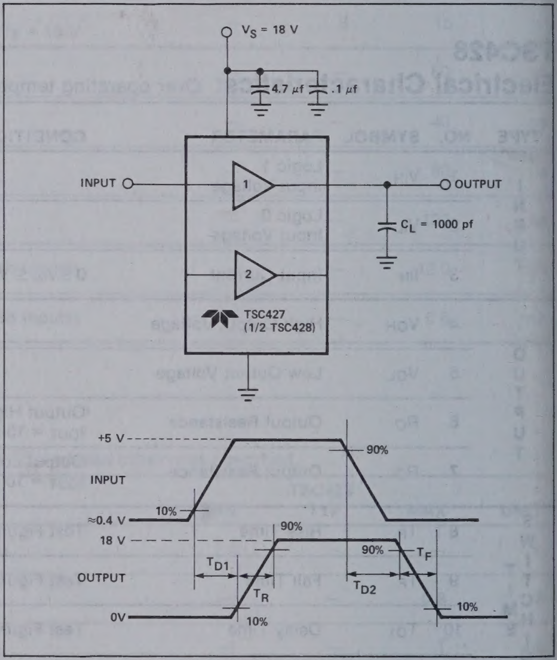
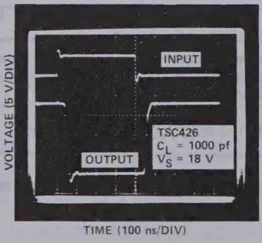
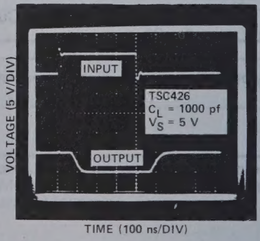

V_S = 18 V
4.7 µf
.1 µf
INPUT
1
2
OUTPUT
C_L = 1000 pf
TSC427
(1/2 TSC428)
+5 V
90%
INPUT
10%
≈0.4 V
18 V
90%
90%
T_F
T_{D1}
OUTPUT
T_R
T_{D2}
10%
0V
10%

Figure 2: Non-Inverting Driver Switching Time

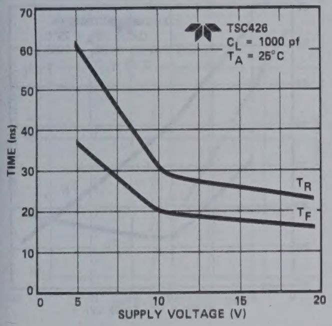
TSC426 Switching Speed



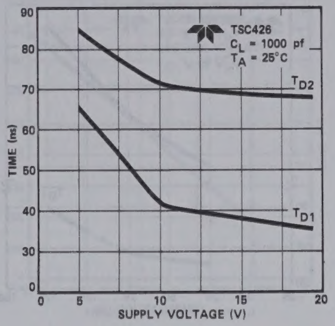


Typical Characteristic Curves

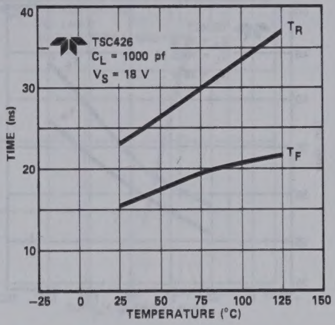
Rise and Fall Time vs Supply Voltage



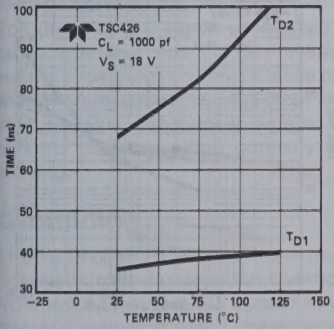
Delay Time vs Supply Voltage



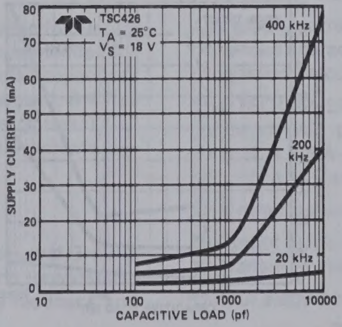
Rise and Fall Time vs Temperature



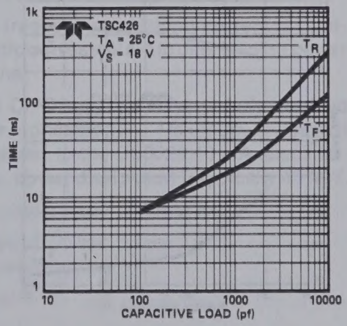
Delay Time vs Temperature



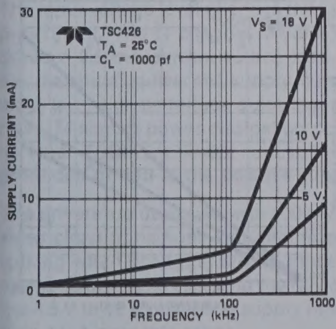
Supply Current vs Capacitive Load



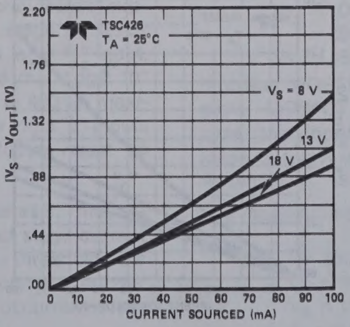
Rise and Fall Time vs Capacitive Load



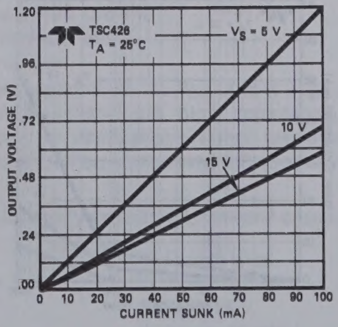
Supply Current vs Frequency



High Output vs Voltage

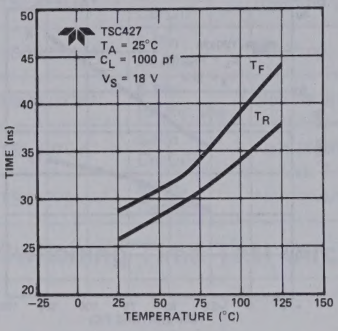


Low Output Voltage

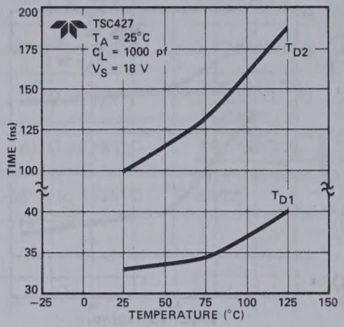


Typical Characteristic Curves

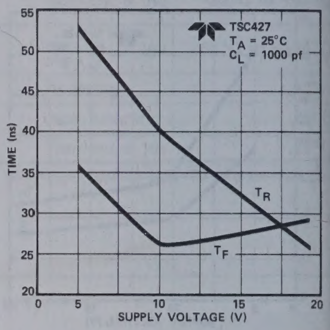
Rise and Fall Time vs Temperature



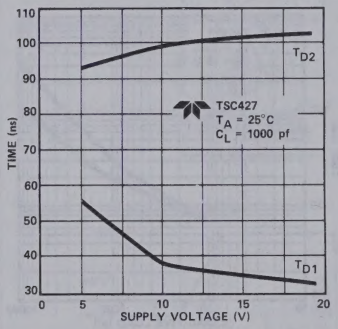
Delay Time vs Temperature



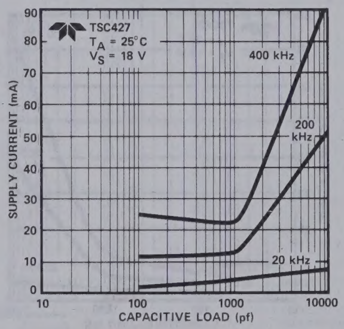
Rise and Fall Time vs Supply Voltage



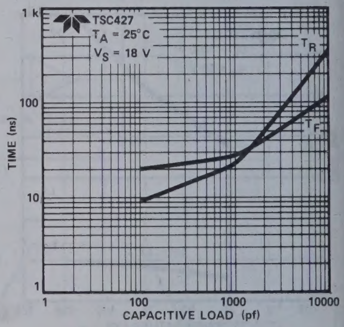
Delay Time vs Supply Voltage



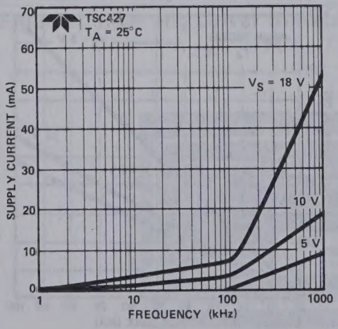
Supply Current vs Capacitive Load



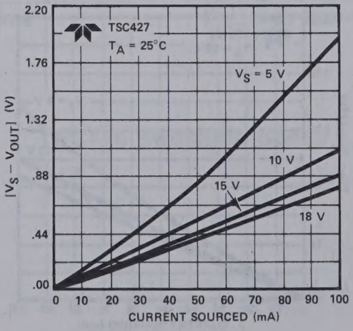
Rise and Fall Time vs Capacitive Load



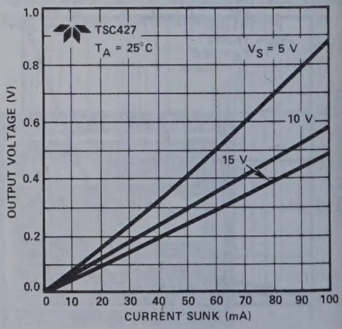
Supply Current vs Frequency



High Output Voltage

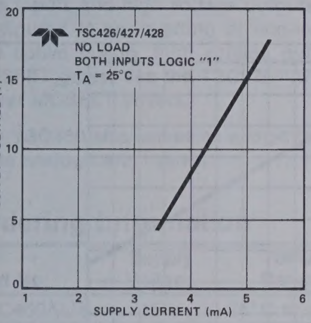


Low Output Voltage

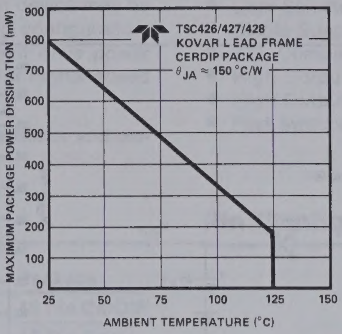


Typical Characteristic Curves

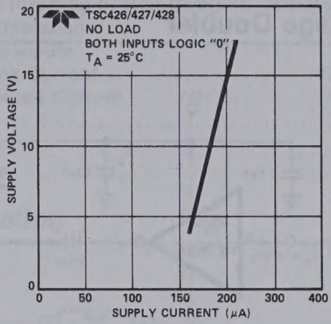
Quiescent Power Supply Current vs Supply Voltage



Package Power Dissipation



Quiescent Power Supply Current vs Supply Voltage



Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, changing a 1000 pf load 18 volts in 25 ns requires a 0.8 A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (<0.5 inch) should be used. A 4.7 μf solid tantalum capacitor in parallel with one or two 0.1 uf ceramic disk capacitors normally provides adequate bypassing.

Grounding

The TSC426 and TSC428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits or a ground plane should be used.

Input Stage

The input voltage level changes the no load or quiescent supply current. The N channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic "1" input, the maximum quiescent supply current is 8 mA. Logic "0" input level signals reduce quiescent current to 400 μA maximum. Minimum power dissipation occurs for logic "0" inputs for the TSC426/427/428; unused driver inputs **must be grounded or tied to the positive supply.**

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5 V making the device TTL compatible over the 4.5 V to 18 V operating supply range. Input current is less than 1 μA over this range.

The TSC426/427/428 may be directly driven by the TL494, SG1526/1527, SG1524, SE5560 and similar switch mode power supply integrated circuits.

Power Dissipation

The supply current vs frequency and supply current vs capacitive load characteristic curves will aid in determining power dissipation calculations.

The TSC426/427/428 CMOS drivers have greatly reduced quiescent DC power consumption. Maximum quiescent current is 8 mA compared to the DS0026 40 mA specification. For a 15 V supply, power dissipation is typically 40 mW.

Two other power dissipation components are:

- Output stage AC and DC load power.
- Transition state power.

Output stage power is:

$$\begin{aligned} P_O &= P_{DC} + P_{AC} \\ &= V_O\,(I_{DC}) + f\,C_L\,V_S^2 \end{aligned}$$

Where:

V_O = DC output voltage
I_{DC} = DC output load current
f = Switching frequency
V_S = Supply voltage

In power MOSFET drive applications the P_{DC} term is negligible. MOSFET power transistors are high impedance, capacitive input devices. In applications where resistive loads or relays are driven the P_{DC} component will normally dominate.

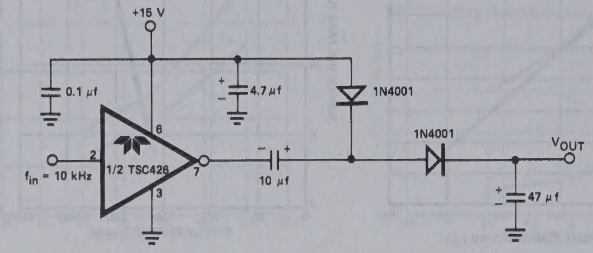
The magnitude of P_{AC} is readily estimated for several cases:

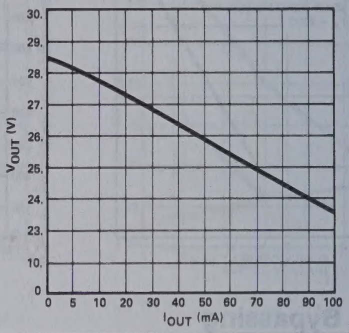
A.
1. $f = 200$ kHz
2. $C_L = 1000$ pf
3. $V_S = 18$ V
4. $P_{AC} = 65$ mW

B.
1. $f = 200$ kHz
2. $C_L = 1000$ pf
3. $V_S = 15$ V
4. $P_{AC} = 45$ mW

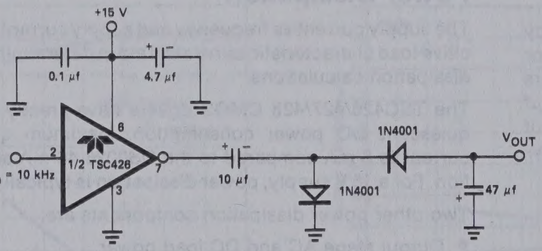
During output level state changes, a current surge will flow through the series connected N and P channel output MOSFETS as one device is turning "ON" while the other is turning "OFF." The current spike flows only during output transitions. The input levels should not be maintained between the logic "0" and logic "1" levels. **Unused driver inputs must be tied to ground and not be allowed to float.** Average power dissipation will be reduced by minimizing input rise times. As shown in the characteristic curves, average supply current is frequency dependent.

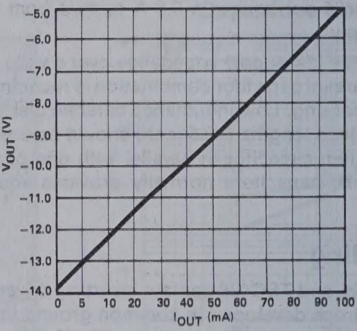
Voltage Doubler


+15 V
0.1 µf
4.7 µf
1N4001
6
2
1/2 TSC426
7
3
f_in = 10 kHz
10 µf
1N4001
V_OUT
47 µf



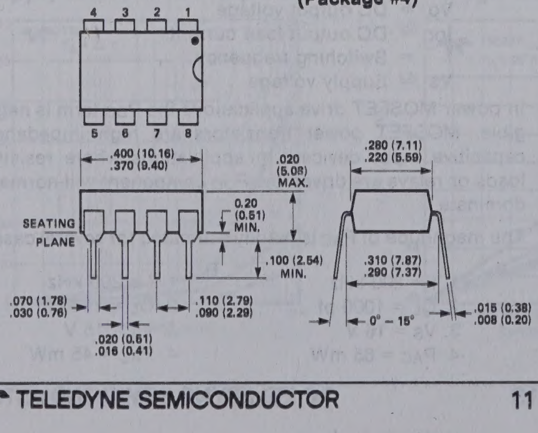
Voltage Inverter


+15 V
0.1 µf
4.7 µf
6
2
1/2 TSC426
7
3
f_in = 10 kHz
10 µf
1N4001
1N4001
V_OUT
47 µf

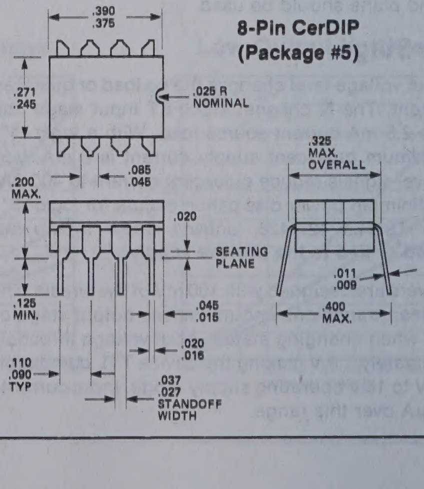


Package Information

8-Pin Plastic Dip (Package #4)


4 3 2 1
5 6 7 8
.400 (10.16)
.370 (9.40)
.280 (7.11)
.220 (5.59)
.020 (5.08) MAX.
0.20 (0.51) MIN.
SEATING PLANE
.100 (2.54) MIN.
.310 (7.87)
.290 (7.37)
.070 (1.78)
.030 (0.76)
.110 (2.79)
.090 (2.29)
0° – 15°
.015 (0.38)
.008 (0.20)
.020 (0.51)
.016 (0.41)

8-Pin CerDIP (Package #5)


.390
.375
.271
.245
.025 R NOMINAL
.085
.045
.325 MAX. OVERALL
.200 MAX.
.020
SEATING PLANE
.011
.009
.125 MIN.
.045
.015
.400 MAX.
.020
.016
.110
.090
TYP
.037
.027
STANDOFF WIDTH

TELEDYNE
SEMICONDUCTOR

TSC450
Dual Driver

eneral Description

he TSC450 is a low cost bipolar dual driver with TTL compatible inputs and high voltage outputs. Each device may be onfigured in an inverting or non-inverting configuration. he active pullup, high voltage outputs will drive power OSFET gates. See the TSC426/427/428 for higher speed ower MOSFET drivers.

he TSC450 also serves as a logic level translator and disrete analog switch driver.

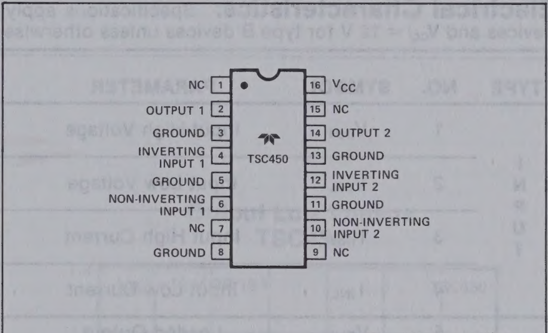
Features

- Dual Device for High Packing Density
- User Selectable Inverting or Non-Inverting Operation
- Single Supply Operation
- TTL Compatible Inputs
- High Output Sink Current .... 12 mA
- High Output Source Current .... 6 mA
- Fast Switching .... 125 ns

rdering Information

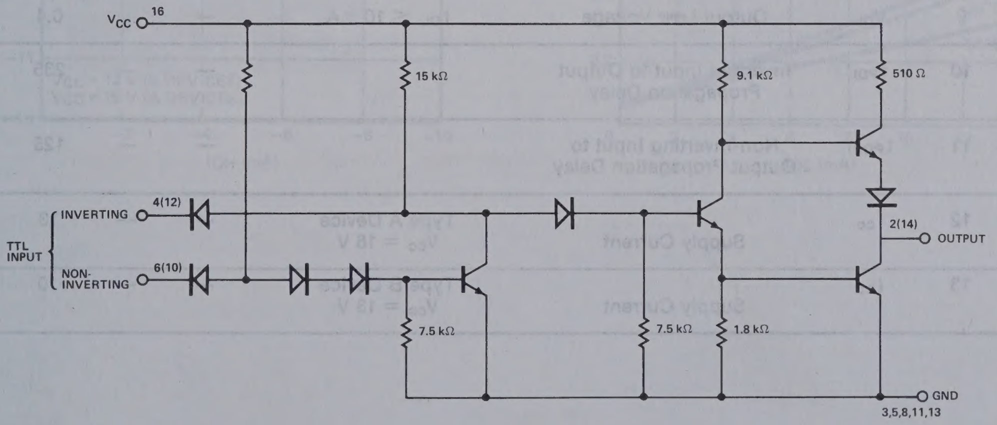
art No.	Supply Voltage	Temp. Range	Package
TSC450AIJE	15 V	-25°C to +85°C	16 Pin CerDIP
TSC450ACPE	15 V	0°C to +70°C	16 Pin Epoxy
TSC450BIJE	12 V	-25°C to +85°C	16 Pin CerDIP
TSC450BCPE	12 V	0°C to +70°C	16 Pin Epoxy
TSC450AMJE	15 V	-55°C to +125°C	16 Pin CerDIP
TSC450BMJE	12 V	-55°C to +125°C	16 Pin CerDIP

Pin Configuration


NC 1
OUTPUT 1 2
GROUND 3
INVERTING INPUT 1 4
GROUND 5
NON-INVERTING INPUT 1 6
NC 7
GROUND 8
TSC450
16 V_{CC}
15 NC
14 OUTPUT 2
13 GROUND
12 INVERTING INPUT 2
11 GROUND
10 NON-INVERTING INPUT 2
9 NC

NC = No Connection

unctional Diagram (1/2 Circuit)


V_{CC} 16
15 kΩ
9.1 kΩ
510 Ω
TTL INPUT
INVERTING 4(12)
NON-INVERTING 6(10)
2(14) OUTPUT
7.5 kΩ
7.5 kΩ
1.8 kΩ
GND
3,5,8,11,13

Absolute Maximum Ratings

	J Package, CerDIP	P Package, Plastic
Storage Temperature	-65°C to +150°C	-55°C to +100°C
Lead Temperature (1/16 inch from case, 10 sec max)	300°C	300°C
Continuous Supply Voltage		
Type B Device	+15.0 V	+15.0 V
Type A Device	+16.5 V	+16.5 V

	J Package, CerDIP	P Package, Plastic
Pulsed Supply Voltage (less than 100 msec)	+18.0 V	+18.0 V
Input Voltage (any input)		
Type B Device	-0.5 to +15 V	-0.5 to +15 V
Type A Device	-0.5 to +18 V	-0.5 to +18 V
Surge Sink Current (less than 100 msec at $T_A = 25°C$)	20 mA	20 mA

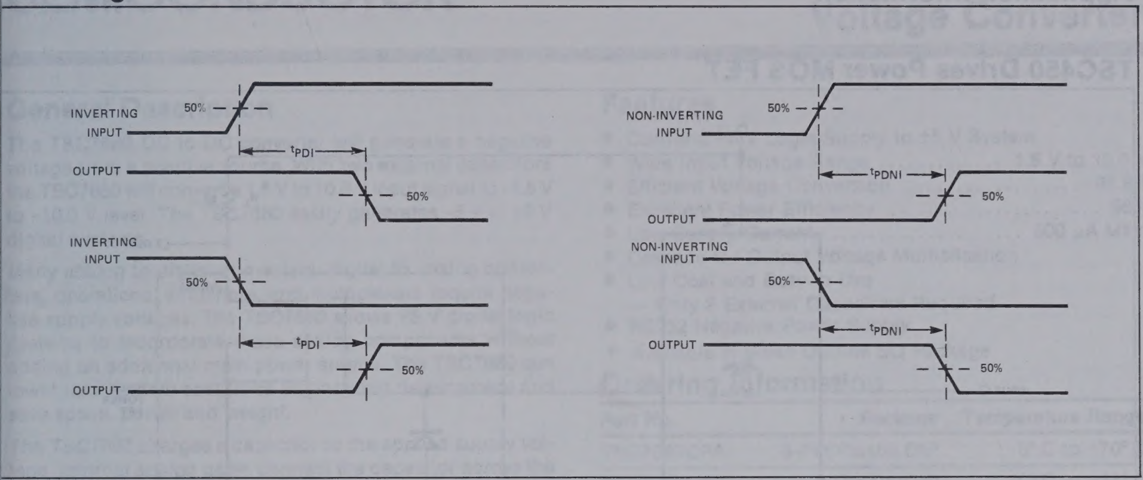
Note: Exceeding the absolute maximum ratings may cause permanent damage. Operation at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Electrical Characteristics:

Specifications apply over full operating temperature range. $V_{CC} = +15$ V for type A devices and $V_{CC} = 12$ V for type B devices unless otherwise indicated.

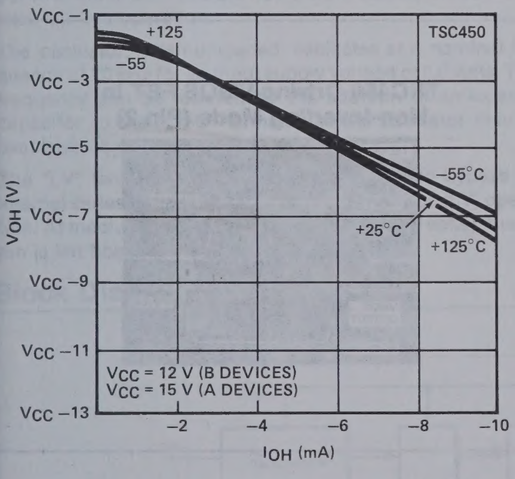
TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC450 MIN	TSC450 TYP	TSC450 MAX	UNIT
INPUT	1	V_{INH}	Input High Voltage	$I_{IN} \leq 40\ \mu A$	2.0	—	—	V
	2	V_{INL}	Input Low Voltage		—	—	0.8	V
	3	I_{INH}	Input High Current		—	—	10	µA
	4	I_{INL}	Input Low Current	$V_{IN} = 0.4$ V	—	—	1.6	mA
OUTPUT	5	V_{OHL}	Loaded Output High Voltage	$V_{CC} = 12$ V, $I_{OH} = 5$ mA (Type B Device)	6.0	—	—	V
	6	V_{OH}	Output High Voltage	$V_{CC} = 11$ V (Type B Device)	9.0	—	—	V
	7	V_{OHL}	Loaded Output High Voltage	$V_{CC} = 15$ V, $I_{OH} = 5$ mA (Type A Device)	9.0	—	—	V
	8	V_{OH}	Output High Voltage	$V_{CC} = 14$ V (Type A Device)	12.0	—	—	V
	9	V_{OL}	Output Low Voltage	$I_{OL} \leq 10$ mA	—	—	0.4	V
SYSTEM	10	t_{PDI}	Inverting Input to Output Propagation Delay		—	—	235	ns
	11	t_{PDNI}	Non-Inverting Input to Output Propagation Delay		—	—	125	ns
SUPPLY	12	I_{CC}	Supply Current	Type A Device $V_{CC} = 16$ V	—	—	13	mA
	13	I_{CC}	Supply Current	Type B Device $V_{CC} = 13$ V	—	—	10	mA

Switching Time Definitions

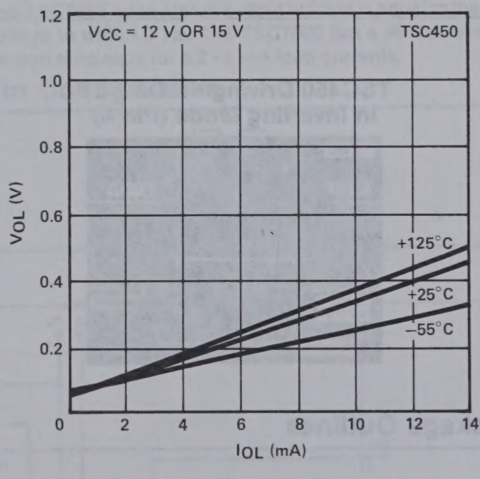

INVERTING
INPUT
50%
tPDI
OUTPUT
50%
INVERTING
INPUT
50%
tPDI
50%
OUTPUT
NON-INVERTING
INPUT
50%
tPDNI
50%
OUTPUT
NON-INVERTING
INPUT
50%
tPDNI
OUTPUT
50%

Operating Characteristics

Output High Voltage TSC450

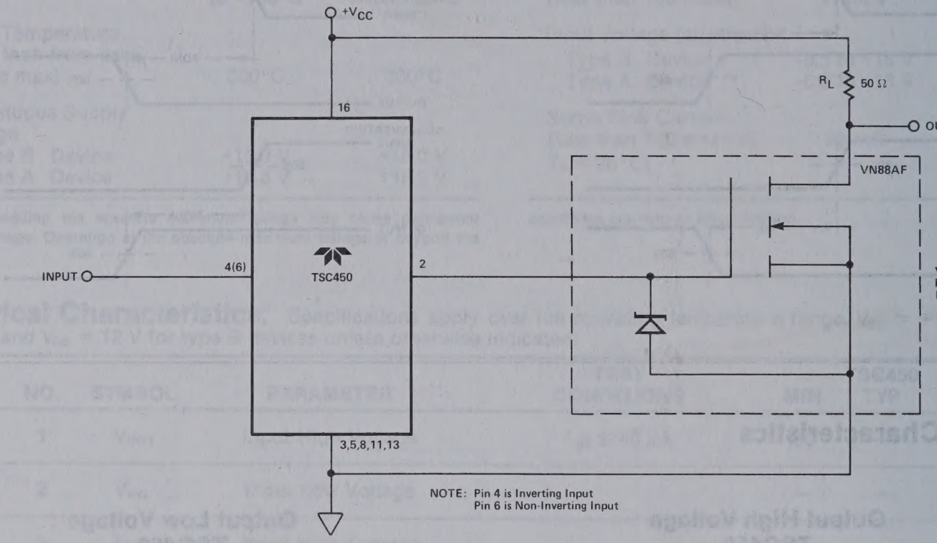


Output Low Voltage TSC450



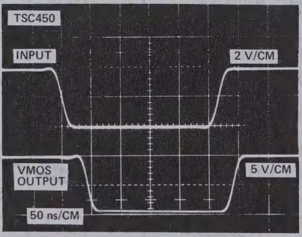
Application Information

TSC450 Drives Power MOS FET

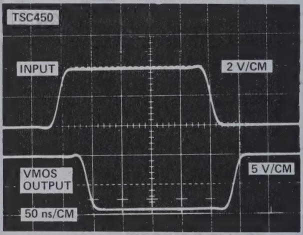

+VCC
16
RL
50 Ω
OUTPUT
VN88AF
INPUT
4(6)
TSC450
2
VMOS
POWER
FET
3,5,8,11,13

NOTE: Pin 4 is Inverting Input
Pin 6 is Non-Inverting Input

TSC450 Driving VMOS FET in Inverting Mode (Pin 4)

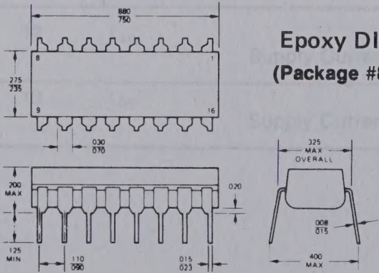


TSC450 Driving VMOS FET in Non-Inverting Mode (Pin 2)

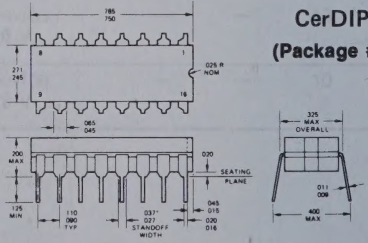


Package Outlines

Epoxy DIP
(Package #8)


880
750
8
1
275
235
9
16
030
070
200
MAX
020
125
MIN
110
090
015
023
325
MAX
OVERALL
008
015
400
MAX

CerDIP
(Package #9)


785
750
8
1
271
245
025 R
NOM
9
16
065
045
200
MAX
020
SEATING
PLANE
125
MIN
110
090
TYP
037"
027
STANDOFF
WIDTH
045
015
020
016
325
MAX
OVERALL
011
009
400
MAX

ALL DIMENSIONS IN INCHES (MILLIMETERS)

TELEDYNE SEMICONDUCTOR

TSC7660
DC to DC Voltage Converter

General Description

The TSC7660 DC to DC converter will generate a negative voltage from a positive source. With two external capacitors the TSC7660 will convert a 1.5 V to 10.0 V input signal to -1.5 V to -10.0 V level. The TSC7660 easily generates -5 V in +5 V digital systems.

Many analog to digital converters, digital to analog converters, operational amplifiers, and multiplexers require negative supply voltages. The TSC7660 allows +5 V digital logic systems to incorporate these analog components without adding an additional main power source. The TSC7660 can lower total system cost, ease engineering development and save space, power and weight.

The TSC7660 charges a capacitor to the applied supply voltage. Internal analog gates connect the capacitor across the output. Charge is transferred to an output storage capacitor completing the voltage conversion. Operation requires only two external capacitors for supply voltage <6.5 V.

Contained on-chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic element which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

Features

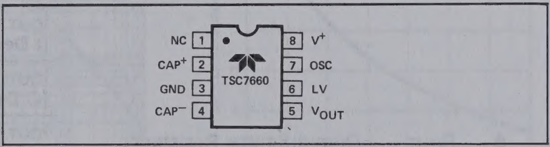
- Converts +5 V Logic Supply to ±5 V System
- Wide Input Voltage Range .... 1.5 V to 10.0 V
- Efficient Voltage Conversion 99.9%
- Excellent Power Efficiency 98%
- Low Supply Current .... 500 μA Max.
- Cascade for Output Voltage Multiplication
- Low Cost and Easy to Use
  - — Only 2 External Capacitors Required
- RS232 Negative Power Supply
- Available in Small Outline SO Package

Ordering Information

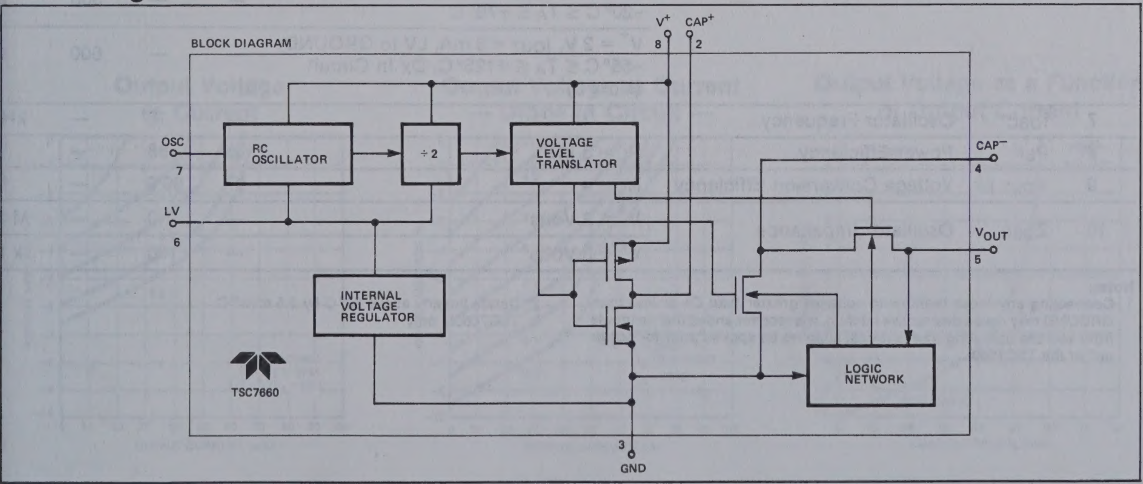
Part No.	Package	Temperature Range
TSC7660CPA	8-Pin Plastic DIP	0° C to +70° C
TSC7660IJA	8-Pin CerDIP	-40° C to +85° C
TSC7660MJA	8-Pin CerDIP	-55° C to +125° C
TSC7660COA	8-Pin SO	0° C to +70° C
TSC7660/Y	Chip	25° C
Devices with MIL-STD-883 Processing		
TSC7660MJA/883	8-Pin CerDIP	-55° C to +125° C

The TSC7660 open circuit output voltage is equal to the input voltage to within 0.1%. The TSC7660 has a 98% power conversion efficiency for a 2 -5 mA load currents.

Pin Configuration



Block Diagram



© 1983

Absolute Maximum Ratings

Supply Voltage	10.5 V
LV and OSC Input Voltage	
(Note 1)	-0.3 V to (V^+ +0.3 V) for $V^+ < 5.5$ V
	(V^+ -5.5 V) to (V^+ +0.3 V) for $V^+ > 5.5$ V
Current into LV (Note 1)	20 µA for $V^+ > 3.5$ V
Output Short Duration ($V_{SUPPLY} \leq 5.5$ V)	Continuous
Power Dissipation (Note 2)	
CerDIP Package	500 mW
Plastic Package	375 mW
Operating Temperature Range	
TSC7660I	-40°C to +85°C
TSC7660M	-55°C to +125°C
TSC7660C	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
(Soldering, 10 sec.)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Characteristics $V^+ = 5$ V, $T_A = 25$°C, $C_{OSC} = 0$, Test Circuit Figure 1 (unless otherwise specified)

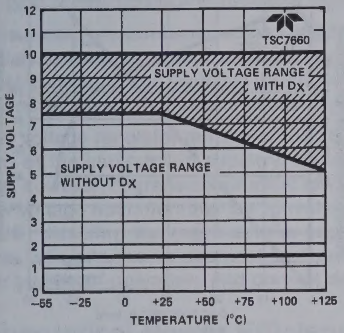
NO.	SYMBOL	PARAMETER	CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
1	I^+	Supply Current	$R_L = \infty$	—	170	500	µA
2	V^+_{H1}	Supply Voltage Range - Hi	0°C ≤ T_A ≤ 70°C, R_L = 10 kΩ, LV Open	3.0	—	6.5	V
		(Dx Out of Circuit) (Note 3)	-55°C ≤ T_A ≤ 125°C, 10 kΩ, LV to GROUND	3.0	—	5.0	V
3	V^+_{L1}	Supply voltage Range - Lo (Dx Out of Circuit)	MIN ≤ T_A ≤ MAX, R_L = 10 kΩ, LV to GROUND	1.5	—	3.5	V
4	V^+_{H2}	Supply Voltage Range - Hi (Dx In Circuit)	MIN ≤ T_A ≤ MAX, R_L = 10 kΩ, LV Open	3.0	—	10.0	V
5	V^+_{L2}	Supply Voltage Range - Lo (Dx In Circuit)	MIN ≤ T_A ≤ MAX, R_L = 10 kΩ, LV to GROUND	1.5	—	3.5	V
6	R_{OUT}	Output Source Resistance	I_{OUT} = 20 mA, T_A = 25°C	—	55	100	Ω
			I_{OUT} = 20 mA, -40°C ≤ T_A ≤ +85°C [I Device]	—	—	130	Ω
			I_{OUT} = 20 mA, -20°C ≤ T_A ≤ +70°C [C Device]	—	—	120	Ω
			I_{OUT} = 20 mA, -55°C ≤ T_A ≤ +125°C (Note 3)	—	—	150	Ω
			V^+ = 2 V, I_{OUT} = 3 mA, LV to GROUND -20°C ≤ T_A ≤ +70°C	—	—	300	Ω
			V^+ = 2 V, I_{OUT} = 3 mA, LV to GROUND, -55°C ≤ T_A ≤ +125°C, Dx In Circuit (Note 3)	—	—	600	Ω
7	f_{OSC}	Oscillator Frequency		—	10	—	kHz
8	P_{EF}	Power Efficiency	R_L = 5 kΩ	95	98	—	%
9	$V_{OUT\,EF}$	Voltage Conversion Efficiency	$R_L = \infty$	97	99.9	—	%
10	Z_{OSC}	Oscillator Impedance	V^+ = 2 Volts	—	1.0	—	MΩ
			V^+ = 5 Volts	—	100	—	kΩ

Notes:

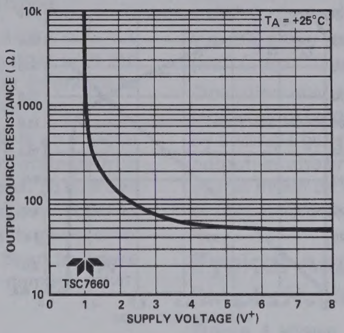
1. Connecting any input terminal to voltages greater than C+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TSC7660.
2. Derate linearly above 50°C by 5.5 mW/°C.
3. TSC7660M only.

Typical Performance Characteristics (Circuit of Figure 1)

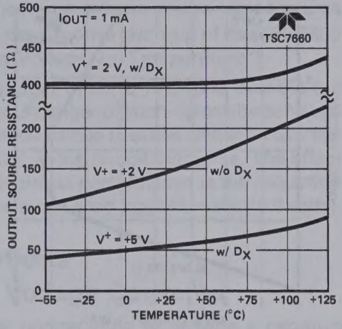
Operating Voltage as a Function of Temperature



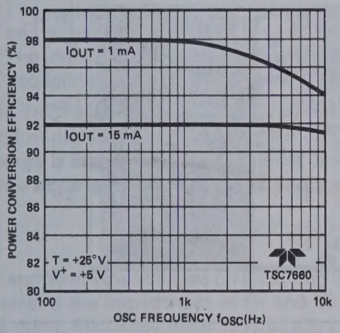
Output Source Resistance as a Function of Supply Voltage



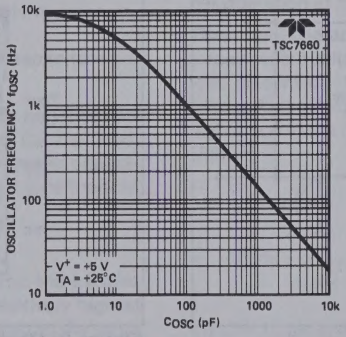
Output Source Resistance as a Function of Temperature



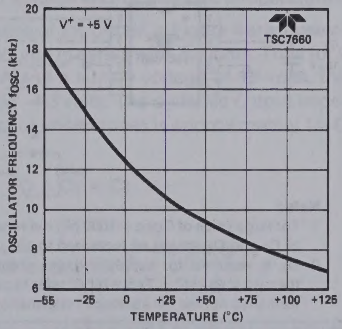
Power Conversion Efficiency as a Function of Osc. Frequency



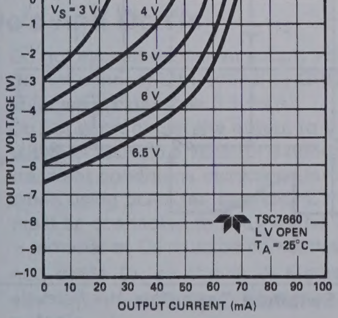
Frequency of Oscillation as a Function of External Osc. Capacitance



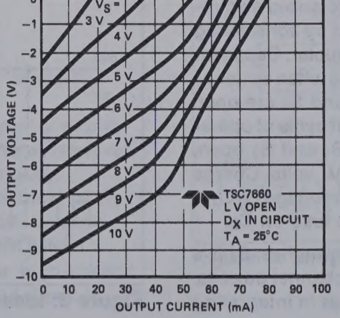
Unloaded Oscillator Frequency as a Function of Temperature



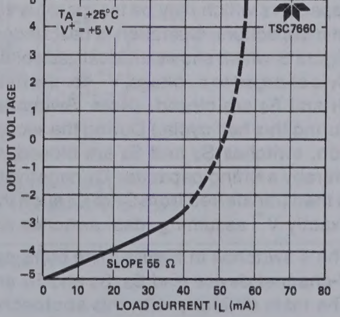
Output Voltage vs Current



Output Voltage vs Current — Diode In Circuit —

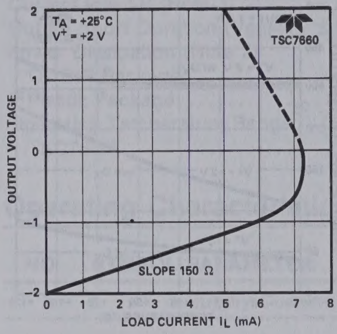


Output Voltage as a Function of Output Current

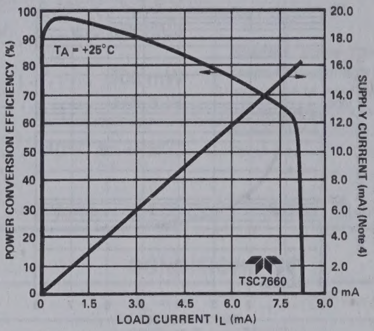


Typical Performance Characteristics (Circuit of Figure 1)

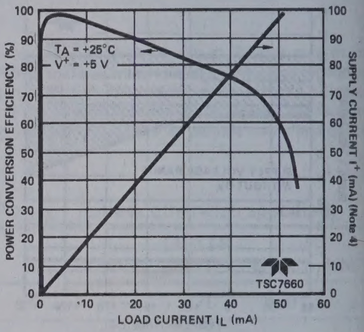
Output Voltage as a Function of Output Current



Supply Current & Power Conversion Efficiency as a Function of Load Current

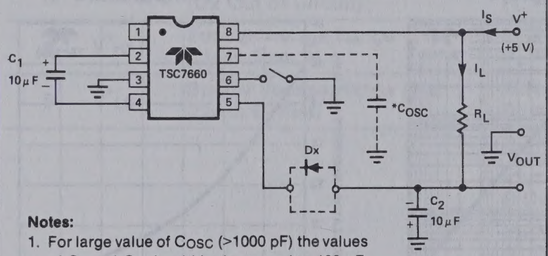


Supply Current Power Conversion Efficiency as a Function of Load Current



Note 4.
Note that the curves on the right include in the supply current that current fed directly into the load (R_L) from V^+ (see Figure 1). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the TSC7660, to the negative side of the load. Ideally, $V_{OUT} = 2 V_{IN}$, $I_S \simeq 2 I_L$, so $V_{IN} \cdot I_S \simeq V_{OUT} \cdot I_L$.

Test Circuit



Notes:

1. For large value of C_{OSC} (>1000 pF) the values of C_1 and C_2 should be increased to 100 μF.
2. D_X is required for supply voltages greater than 6.5 V @ −55° ≤ T_A ≤ +70° C; refer to performance curves for additional information.

Figure 1: TSC7660 Test Circuit

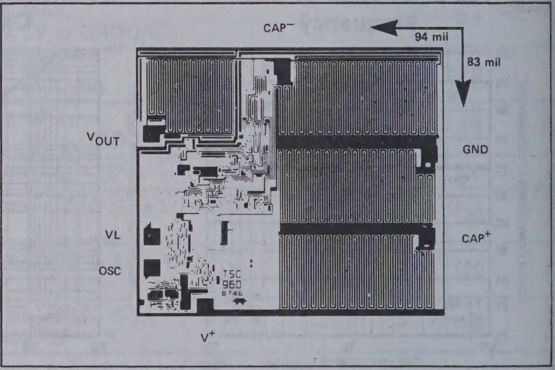


Figure 2: Chip Topography

Circuit Description

The TSC7660 contains all the necessary circuitry to complete a voltage doubler, with the exception of two external capacitors which may be inexpensive 10 μF polarized electrolytic capacitors. Operation is best understood by considering Figure 3, which shows an idealized voltage doubler. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2.

The 4 switches in Figure 3 are MOS power switches; S_1 is a P-channel device and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating

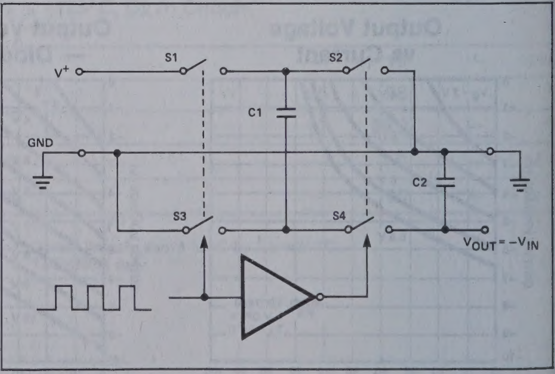


Figure 3: Idealized Switched Capacitor

the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the TSC7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators and switches the substrates or S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the TSC7660 is an integral part of the anti-latchup circuitry. It's inherent voltage drop can, however, degrade operation at low voltages. To improve low voltage operation the "LV" pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

Theoretical Power Efficiency Considerations

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

- The drive circuitry consumes minimal power
- The output switches have extremely low ON resistance and virtually no offset.
- The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TSC7660 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 3) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore, it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Do's And Don'ts

- Do not exceed maximum supply voltages.
- Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
- Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
- When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the TSC7660 and the + terminal of C_2 must be connected to GROUND.
- Add diode D_X as shown in Figure 1 for high-voltage, elevated temperature applications. A1N914 diode is suitable.

Considerations for High Voltage and Elevated Temperature

The TSC7660 will operate efficiently over its specified temperature range with only two external passive components (storage and pump capacitors), provided the operating supply voltage does not exceed 6.5 volts at +70° C and 5.0 volts at +125° C. Exceeding these maximums at the temperatures indicated may result in desctructive latch-up of the TSC7660 (Ref: Graph "Operating Voltage Vs. Temperature")

Operation at supply voltages of up to 10.0 volts over the full temperature range without danger of latch-up can be achieved by adding a general purpose diode in series with the TSC7660 output, as shown by "D_X" in the circuit diagrams. The effect of this diode on overall circuit performance is the reduction of output voltage by one diode drop (approximately 0.6 volts).

Typical Applications

Simple Negative Voltage Converter

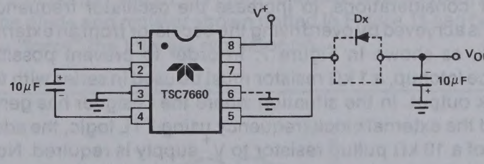
Figure 4 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5 V to +10.0 V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5 volts, and that diode D_X must be included for proper operation at higher voltage and/or elevated temperatures.

The output characteristics of the circuit in Figure 4 are those of a nearly ideal voltage source in series with 70 ohms. Thus for a load current of -10 mA and a supply voltage of +5 volts, the output voltage would be -4.3 volts. The dynamic output impedance due to the capacitor impedances is approximately $1/\omega C$ where:

$$C = C_1 = C_2$$

$$\text{giving} \quad \frac{1}{\omega C} = \frac{1}{2\pi\ f_{OSC} \times 10^{-5}} = 3 \text{ ohms}$$

for $C = 10\ \mu F$ and $f_{OSC} = 5$ kHZ (1/2 of oscillator frequency)



*Note:
1. $V_{OUT} = -n\ V^+$ FOR $1.5\ V \le V^+ \le 6.5\ V$
2. $V_{OUT} = -n\ (V^+ - V_{FDX})$ FOR $6.5\ V \le V^+ \le 10.0\ V$

Figure 4: Simple Negative Converter

Paralleling Devices

Any number of TSC7660 voltage convertors may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately

$$R_{OUT} = \frac{R_{OUT}\text{ (of TSC7660)}}{n\text{ (number of devices)}}$$

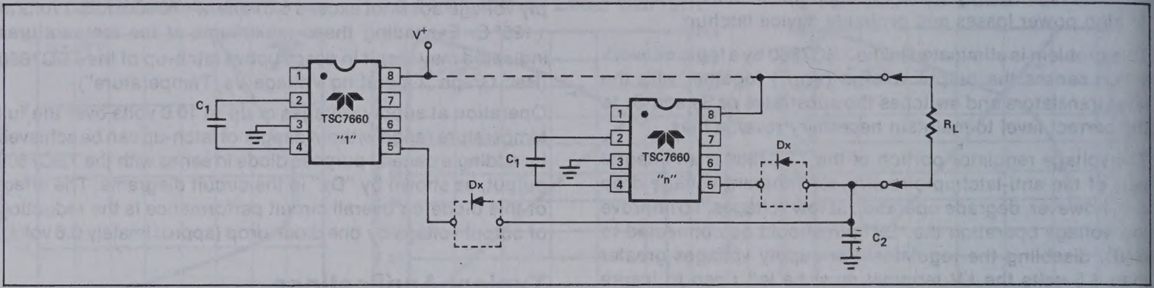


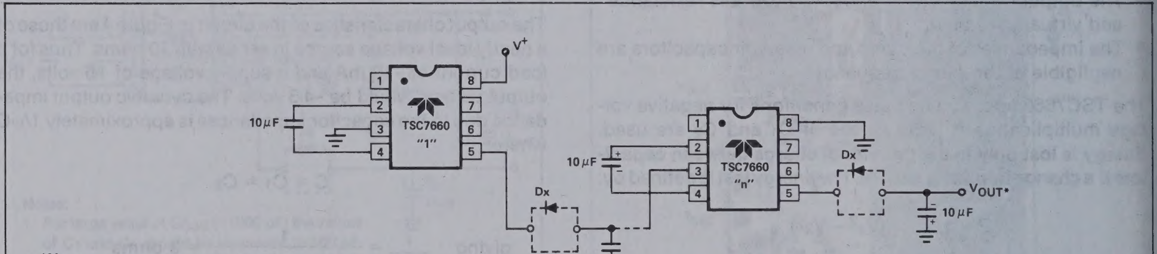
Figure 5: Paralleling Devices Lowers Output Impedance

Cascading Devices

The TSC7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage, however, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TSC7660 R_{OUT} values.



*Note:
1. $V_{OUT} = -n\ V^+$ FOR $1.5\ V \le V^+ \le 6.5\ V$
2. $V_{OUT} = -n\ (V^+ - V_{FDX})$ FOR $6.5\ V \le V^+ \le 10.0\ V$

Figure 6: Increased Output Voltage By Cascading Devices

Changing the TSC7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 7. In order to prevent possible device latchup, a 1 kΩ resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

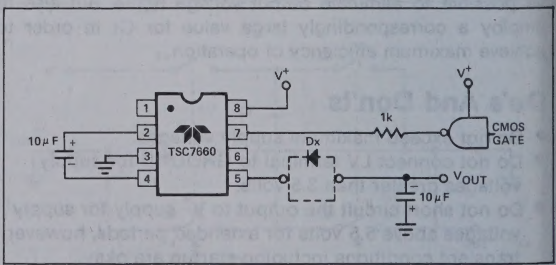


Figure 7: External Clocking

It is also possible to increase the conversion efficiency of the TSC7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 8. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and the reservoir (C_2) capacitors. To overcome this increase the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100 pf capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1 kHz from its nominal frequency of 10 kHz (a multiple of 10), and necessitate a corresponding increase in the value of C_1 and C_2 (from 10 μF to 100 μF).

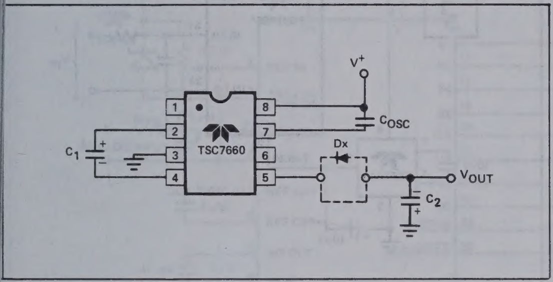


Figure 8: Lowering Oscillator Frequency

Positive Voltage Multiplication

The TSC7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 9. In this application, the pump inverter switches of the TSC7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2\,V^+) - (2\,V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10 mA it will be approximately 60 ohms.

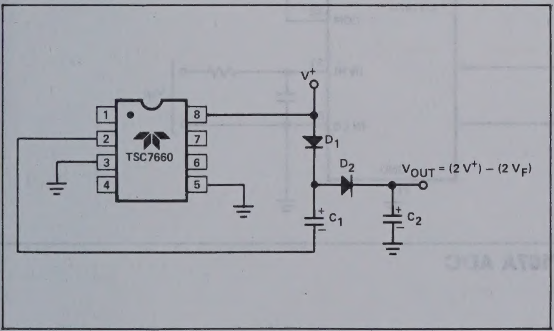


Figure 9: Positive Voltage Multiplier

Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 10 combines the functions shown in Figures 4 and 9 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9 volts and -5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

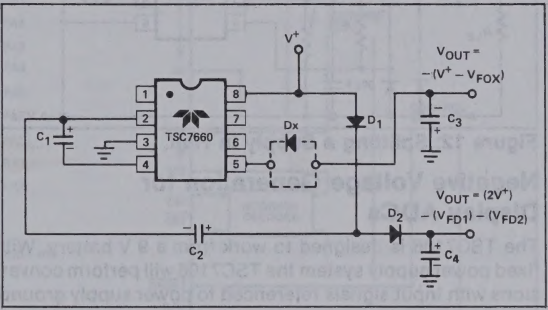


Figure 10: Combined Negative Converter and Positive Multiplier

Efficient Positive Voltage Multiplication/Conversion

Since the switches that allow the charge pumping operation are bidirectional, the charge transer can be performed backwards as easily as forwards. Figure 11 shows a TSC7660 transforming -5 V to +5 V (or +5 V to +10 V, etc.). The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in Figure 10, could be used to start this circuit up, after which it will bypass the other (D1 and D2 in Figure 10 would never turn on) or else the diode and resistor shown dotted in Figure 11 can be used to "force" the internal regulator on.

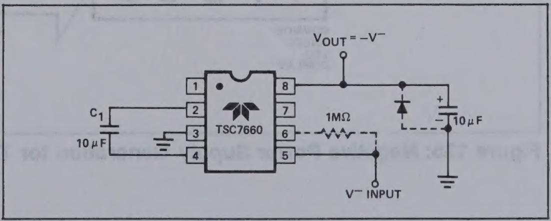


Figure 11: Positive Voltage Conversion

Voltage Splitting

The same bidirectional characteristics used in Figure 11 can also be used to split a higher supply in half, as shown in Figure 12. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 6, +15 V can be converted (via +7.5, and -7.5 V) to a nominal -15 V, though with rather high series resistance (~250 Ω).

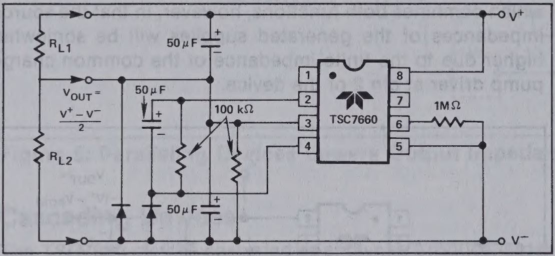

V^+
R_{L1}
50 µF
$V_{OUT} = \frac{V^+ - V^-}{2}$
50 µF
100 kΩ
1
2
3
4
TSC7660
8
7
6
5
1MΩ
R_{L2}
50 µF
V^-

Figure 12: Splitting a Supply in Half.

Negative Voltage Generation for Display ADCs

The TSC7106 is designed to work from a 9 V battery. With fixed power supply system the TSC7106 will perform conversions with input signals referenced to power supply ground.

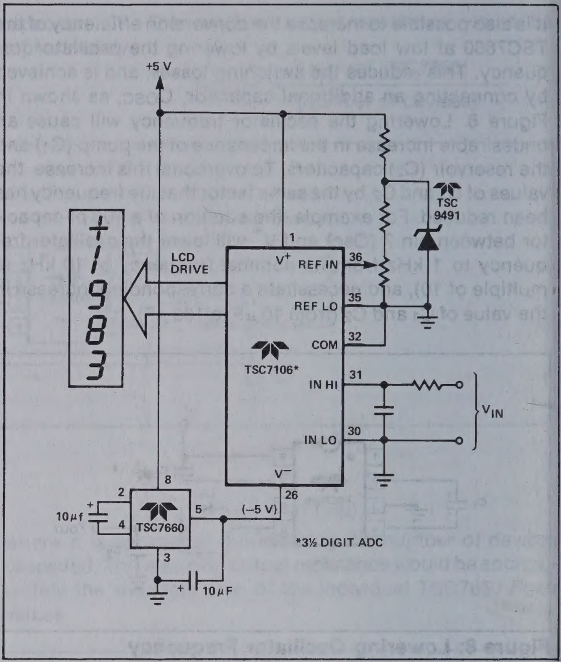

+5 V
+1983
LCD DRIVE
TSC 9491
1
V^+
REF IN
36
35
REF LO
32
COM
TSC7106*
31
IN HI
V_{IN}
30
IN LO
V^-
26
8
2
10 µf
4
TSC7660
5
(−5 V)
3
10 µF
*3½ DIGIT ADC

Figure 13a: Fixed Power Supply Operation of TSC7106 ADC.

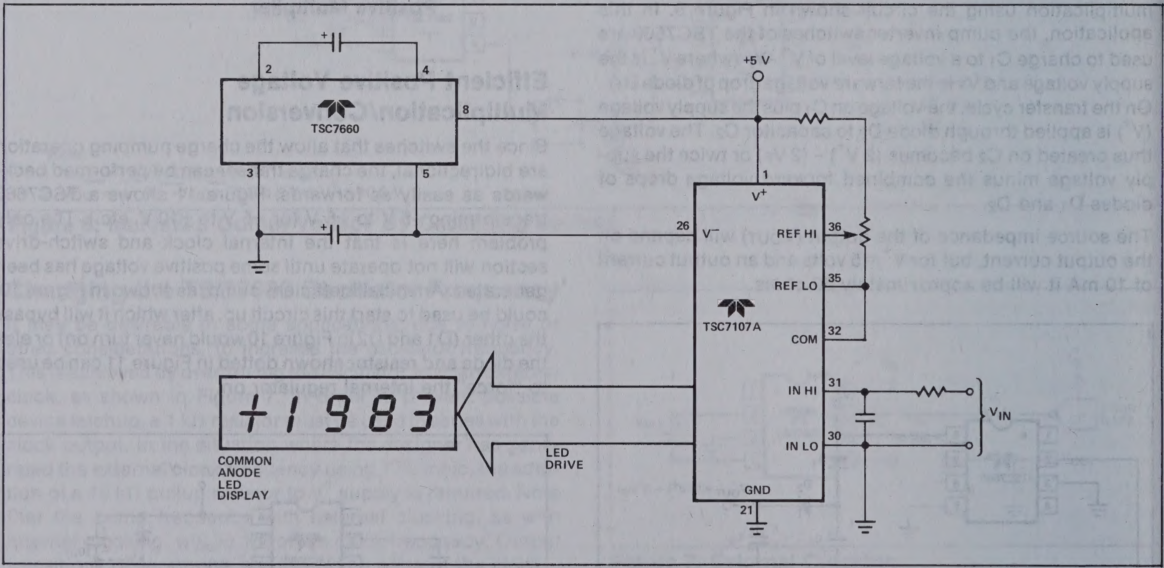

2
4
TSC7660
8
3
5
+5 V
1
V^+
26
V^-
REF HI
36
35
REF LO
TSC7107A
32
COM
31
IN HI
V_{IN}
30
IN LO
GND
21
+1983
COMMON ANODE LED DISPLAY
LED DRIVE

Figure 13b: Negative Power Supply Generation for TSC7107A ADC

Negative Supply Generation for 4 1/2 Digit Data Acquisition System

The TSC7136 is a 4 1/2 Digit ADC operating from ±5 V supplies. The TSC7660 inexpensively provides a -5 V source. see AN16 and AN17 for TSC7135 interface details and software routines.

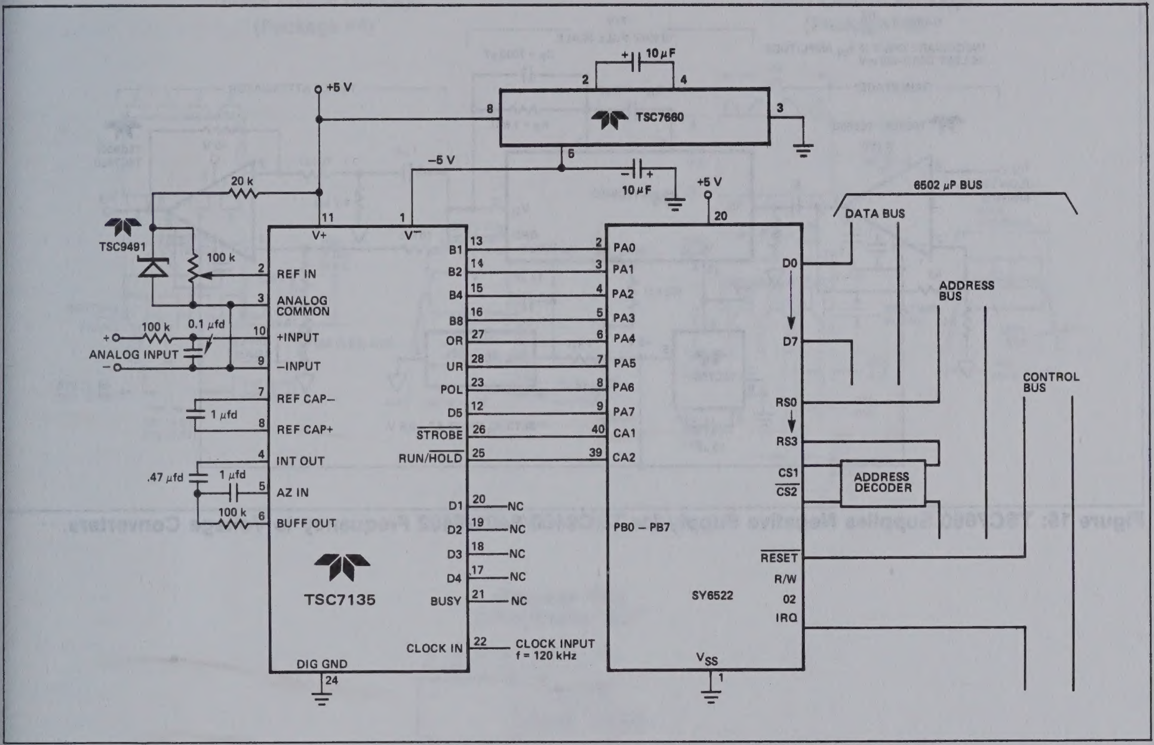

+5 V
10 µF
2
4
8
TSC7660
3
5
-5 V
10 µF
+5 V
20
6502 µP BUS
DATA BUS
20 k
TSC9491
100 k
11
1
V+
V−
REF IN
ANALOG COMMON
100 k
0.1 µfd
+INPUT
ANALOG INPUT
−INPUT
REF CAP−
1 µfd
REF CAP+
INT OUT
.47 µfd
1 µfd
AZ IN
100 k
BUFF OUT
TSC7135
DIG GND
24
B1
B2
B4
B8
OR
UR
POL
D5
STROBE
RUN/HOLD
D1
D2
D3
D4
BUSY
CLOCK IN
NC
CLOCK INPUT f = 120 kHz
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
CA1
CA2
PB0 – PB7
SY6522
VSS
D0
D7
ADDRESS BUS
CONTROL BUS
RS0
RS3
CS1
CS2
ADDRESS DECODER
RESET
R/W
02
IRQ

Figure 14: TSC7660 Supplies -5 V for Converters in Microprocessor Controlled Data Acquisition Systems.

Negative Supply Generation for TSC94XX Frequency to Voltage Converters.

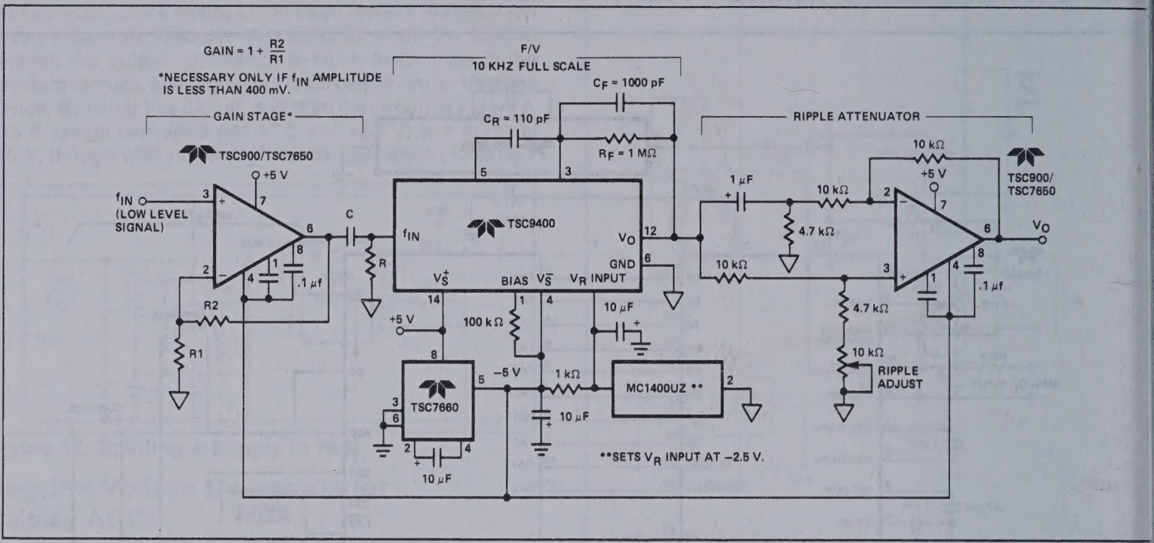
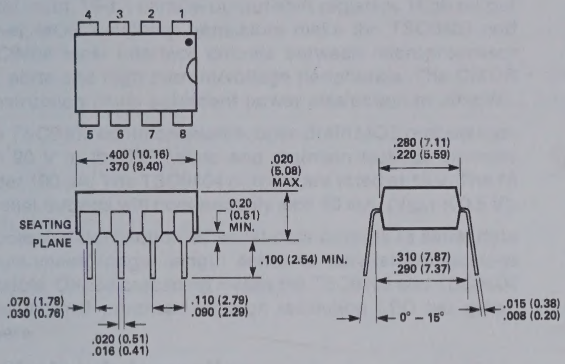

GAIN = 1 + R2/R1
*NECESSARY ONLY IF fIN AMPLITUDE IS LESS THAN 400 mV.
GAIN STAGE*
TSC900/TSC7650
+5 V
fIN
(LOW LEVEL SIGNAL)
R2
R1
C
R
.1 µf
F/V
10 KHZ FULL SCALE
CF = 1000 pF
CR = 110 pF
RF = 1 MΩ
TSC9400
fIN
VO
GND
VS+
BIAS
VS−
VR INPUT
+5 V
100 kΩ
10 µF
TSC7660
10 µF
−5 V
1 kΩ
10 µF
MC1400UZ **
**SETS VR INPUT AT −2.5 V.
RIPPLE ATTENUATOR
1 µF
10 kΩ
4.7 kΩ
10 kΩ
4.7 kΩ
10 kΩ
RIPPLE ADJUST
10 kΩ
+5 V
TSC900/
TSC7650
VO
.1 µf

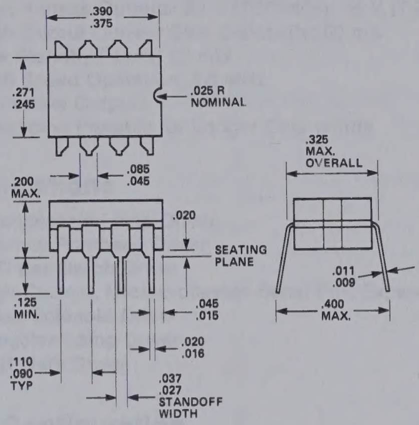
Figure 15: TSC7660 Supplies Negative Supply for TSC9400/9401/9402 Frequency to Voltage Converters.

Package Outline

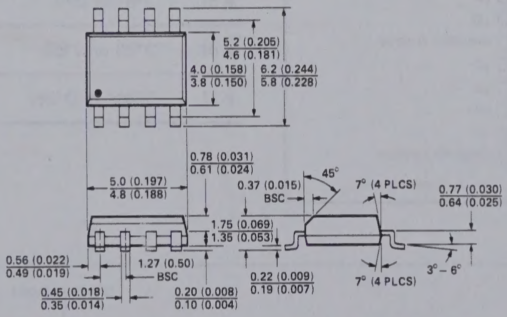
8-Pin Plastic Package
(Package #4)


4 3 2 1
5 6 7 8
.400 (10.16)
.370 (9.40)
.020 (5.08) MAX.
.280 (7.11)
.220 (5.59)
0.20 (0.51) MIN.
SEATING PLANE
.100 (2.54) MIN.
.310 (7.87)
.290 (7.37)
.070 (1.78)
.030 (0.76)
.110 (2.79)
.090 (2.29)
.015 (0.38)
.008 (0.20)
0° – 15°
.020 (0.51)
.016 (0.41)

8-Pin CerDIP Package
(Package #5)


.390
.375
.271
.245
.025 R NOMINAL
.325 MAX. OVERALL
.200 MAX.
.085
.045
.020
SEATING PLANE
.011
.009
.125 MIN.
.045
.015
.400 MAX.
.020
.016
.110
.090 TYP
.037
.027 STANDOFF WIDTH

(Package #25)
8-Pin Plastic "SO"


5.2 (0.205)
4.6 (0.181)
4.0 (0.158)
3.8 (0.150)
6.2 (0.244)
5.8 (0.228)
0.78 (0.031)
0.61 (0.024)
45°
5.0 (0.197)
4.8 (0.188)
0.37 (0.015) BSC
7° (4 PLCS)
0.77 (0.030)
0.64 (0.025)
1.75 (0.069)
1.35 (0.053)
0.56 (0.022)
0.49 (0.019)
1.27 (0.50) BSC
0.45 (0.018)
0.35 (0.014)
0.20 (0.008)
0.10 (0.004)
0.22 (0.009)
0.19 (0.007)
3° – 6°
7° (4 PLCS)

TELEDYNE SEMICONDUCTOR

TSC9403
TSC9404
Serial Input/16-Bit Parallel Output Peripheral Driver
• High Voltage, High Current Outputs

General Description

The Teledyne Semiconductor TSC9403 and TSC9404 are serial input, 16-bit parallel output shift registers. High output power MOS switching transistors make the TSC9403 and TSC9404 ideal interface circuits between microprocessor I/O ports and high current/voltage peripherals. The CMOS construction limits quiescent power dissipation to 20 mW.

The TSC9403 common source, open drain MOS outputs sustain 20 V in the OFF state and maintain leakage currents under 100 μA. The TSC9404 outputs are rated at 15 V. The 16 parallel outputs will continuously sink 60 mA. ($V_{SAT} \leq 0.5$ V).

Successive connection of serial data outputs to serial data inputs make longer length serial to parallel conversions possible. Device cascading makes the TSC9403 and TSC9404 ideal thermal printhead or high resolution LED bar graph drivers.

Ordering Information

Part	Package	Temperature Range	Output Voltage
TSC9403CJ	24-Pin Epoxy Dip	0°C to 70°C	20 V
TSC9403IL	24-Pin CerDIP	-25°C to 85°C	20 V
TSC9404CJ	24-Pin Epoxy Dip	0°C to 70°C	15 V
TSC9404IL	24-Pin CerDIP	-25°C to 85°C	15 V
TSC9404ML	24-Pin CerDIP	-55°C to 125°C	15 V

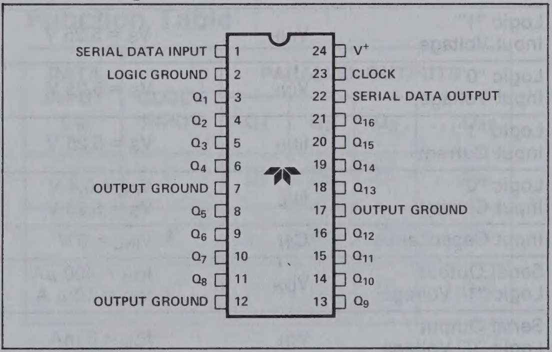
Features

- High Voltage Outputs: 20 V (TSC9403), 15 V (TSC9404)
- High Output Current Sink Capability: 60 mA
- Low Standby Power: 20 mW
- High Speed Operation: 3.0 MHz
- 16 Parallel Outputs
- Cascading Possible for Longer Data Words

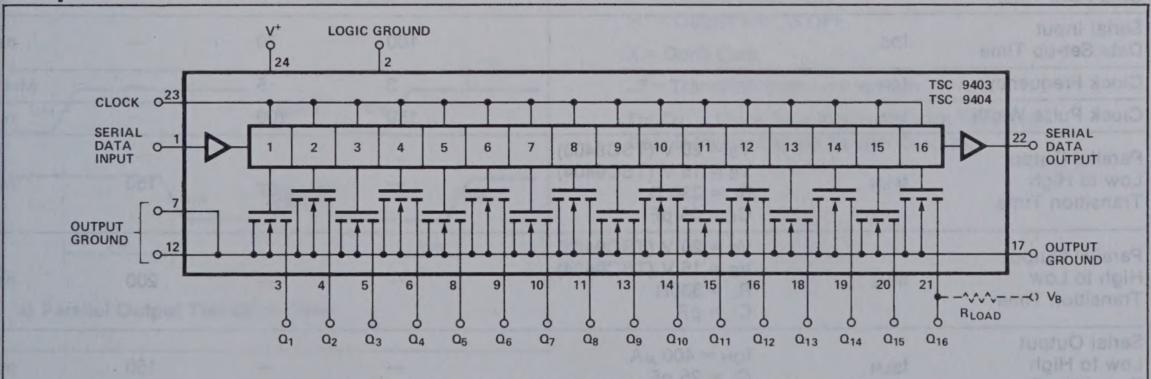
Applications

- Incandescent Lamp Driver
- Thermal Printhead Driver
- LED Bar Graph Driver
- High Current, Microprocessor Serial Port Expander
- Relay/Solenoid Driver
- Tungsten Lamp Driver
- SCR Gate Driver

Pin Configuration


SERIAL DATA INPUT 1
LOGIC GROUND 2
Q1 3
Q2 4
Q3 5
Q4 6
OUTPUT GROUND 7
Q5 8
Q6 9
Q7 10
Q8 11
OUTPUT GROUND 12
24 V+
23 CLOCK
22 SERIAL DATA OUTPUT
21 Q16
20 Q15
19 Q14
18 Q13
17 OUTPUT GROUND
16 Q12
15 Q11
14 Q10
13 Q9

Simplified Schematic


V+
24
LOGIC GROUND
2
CLOCK
23
SERIAL DATA INPUT
1
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
TSC 9403
TSC 9404
22
SERIAL DATA OUTPUT
OUTPUT GROUND
7
12
17
OUTPUT GROUND
3
4
5
6
8
9
10
11
13
14
15
16
18
19
20
21
VB
RLOAD
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16

NOTE: LOGIC 1 SERIAL DATA INPUT BIT TURNS OUTPUT NMOS ON.

© 1983

Absolute Maximum Ratings

Supply Voltage (V+ to Logic Ground)	7.0 V
Digital Logic Input Voltage	5.5 V
Parallel Output Drain Voltage	22 V
Parallel Output Drain Current	80 mA
Logic Ground to Output Ground Potential Difference	100 mV
Package Power Dissipation	
CerDIP Package	1 W @ 85° C
CerDIP Package	0.4 W @ +125° C
Epoxy Package	1 W @ 70° C
Operating Temperature	
CerDIP Package (IL)	$-25°C \le T_A \le +85°C$
CerDIP Pacakge (ML)	$-55°C \le T_A \le +125°C$
Epoxy Package (CJ)	$0°C \le T_A \le +70°C$
Storage Temperature	$-65°C \le T_A \le +150°C$
Lead Temperature (Soldering, 60 Sec)	+300° C

Electrical Characteristics

(V_S = 5.0 V, $0°C \le T_A \le +70°C$ for TSC9403CJ, TSC9404CJ and $-25°C \le T_A$ +85° C for TSC9403IL, TSC9404IL, and -55° C to +125° C for TSC9404ML unless otherwise stated).

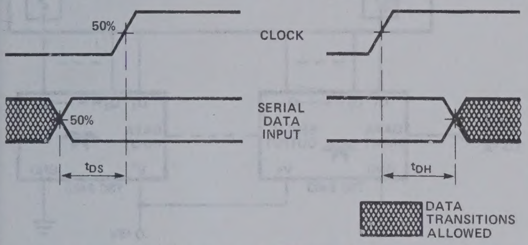
PARAMETER	SYMBOL	CONDITIONS	TSC9403/TSC9404 MIN	TYP	MAX	UNITS
Output ON Voltage	V_{SAT}	I_O = 60 mA V_S = 4.75 V	—	0.35	0.5	V
Output OFF Voltage	V_B	TSC9403	—	—	20	V
		TSC9404	—		15	V
Output Sink Current	I/O	$V_{SAT} \le 0.5$ V (Note 1)	60	—	—	mA
Output Leakage Current	I_{OX}	V_S = 4.75 V V_B = 20 V (TSC9403) V_B = 15 V (TSC9404)	—	—	100	μA
Logic "1" Input Voltage	V_{INH}	V_S = 5.25 V	3.3	—	—	V
Logic "0" Input Voltage	V_{INL}	V_S = 5.25 V	—	—	0.8	V
Logic "1" Input Current	I_{INH}	V_S = 5.25 V	—	—	20	μA
Logic "0" Input Current	I_{INL}	V_{INL}= 0.4 V V_S = 5.25 V	—	—	400	μA
Input Capacitance	C_{IN}	V_{INL} = 0 V	—	15	—	pF
Serial Output Logic "1" Voltage	V_{OH}	I_{OH} = 400 μA I_{OH} = 10 μ A	2.4 4.5	— —	— —	V V
Serial Output Logic "0" Voltage	V_{OL}	I_{OL} = 5 mA	—	—	0.4	V
Serial Input Data Hold Time	t_{DH}		20	0	—	ns
Serial Input Data Set-up Time	t_{DS}		100	70	—	ns
Clock Frequency	t_{CP}		3	5	—	MHz
Clock Pulse Width	t_{PW}		150	100	—	ns
Parallel Output Low to High Transition Time	t_{PLH}	V_B = 20 V (TSC9403) V_B = 15 V (TSC9404) R_L = 330 Ω C_L = 25 pF	—	—	150	ns
Parallel Output High to Low Transition Time	t_{PHL}	V_B = 20 V (TSC9403) V_B = 15 V (TSC9404) R_L = 330Ω C_L = pF	—	—	200	ns
Serial Output Low to High Transition Time	t_{SLH}	I_{OH} = 400 μA C_L = 25 pF	—	—	150	ns

Electrical Characteristics (Cont.)

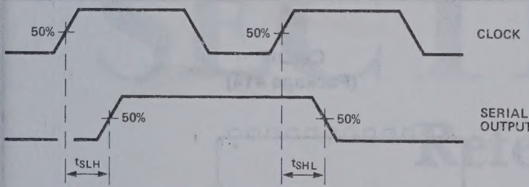
PARAMETER	SYMBOL	CONDITIONS	TSC9403/TSC9404 MIN	 TYP	 MAX	UNITS
Serial Output High to Low Transition Time	t_{SHL}	$I_{OL} = 5$ mA $C_L = 25$ pF	—	—	75	ns
Operating Supply Voltage	V_S		4.75	5.0	5.25	V
Quiescent Power Supply	I_S	$V_S = 5.25$ V $f_C = 0$ Hz $V_{IHL} = 0$ V $I_O = 0$ mA Pin 22 Open	—	1.0	4.0	mA

Note 1: Maintain Chip Temperature ≤ 150° C.

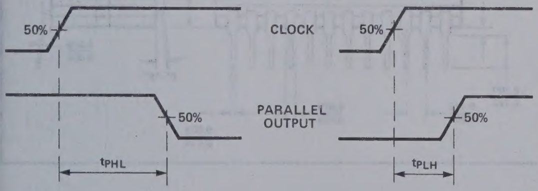
Timing Diagrams


50%
CLOCK
50%
SERIAL
DATA
INPUT
tDS
tDH
DATA
TRANSITIONS
ALLOWED

a) Serial Input Data Hold and Set-up Time


50%
50%
CLOCK
50%
50%
SERIAL
OUTPUT
tSLH
tSHL

b) Serial Output Transition Time


50%
CLOCK
50%
50%
PARALLEL
OUTPUT
50%
tPHL
tPLH

c) Parallel Output Transition Time

Function Table

DATA INPUT D_N	CLOCK INPUT	PARALLEL OUTPUTS Q_1	 Q_2	 Q_3	 $\ldots Q_{16}$
X	L	$\overline{D_1}$	$\overline{D_2}$	$\overline{D_3}$	$\ldots\overline{D_{16}}$
H	↑	L*	$\overline{D_1}$	$\overline{D_2}$	$\ldots\overline{D_{15}}$
L	↑	H*	$\overline{D_1}$	$\overline{D_2}$	$\overline{D_{15}}$

L = Logic 0
H = Logic 1

L* = Output NMOS ON
H* = Output NMOS OFF

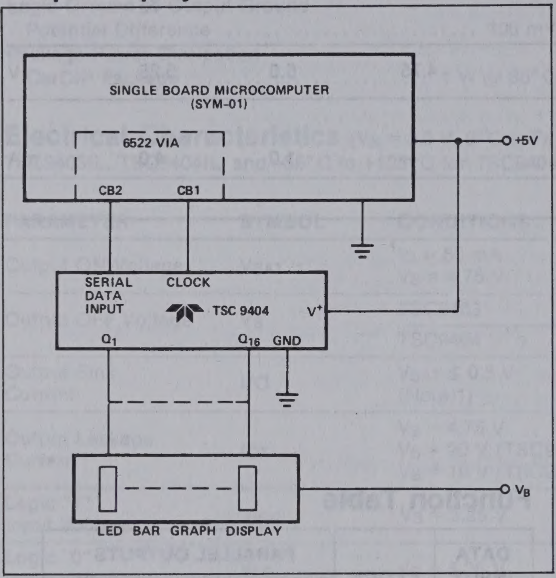
X = Don't Care

↑ = Transition from Low to High

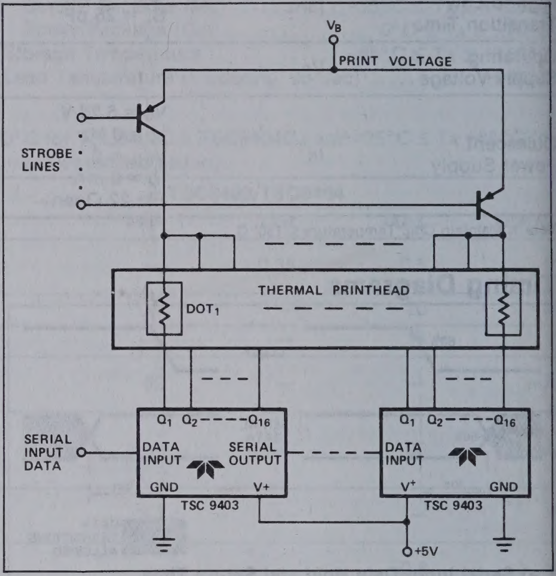
$D_1, D_2, \ldots D_{16}$ = Data Inputs at Clock Time T_{-N}.
Data is Inverted at the Parallel Outputs.

Applications

Microprocessor Controlled LED Bar Graph Display

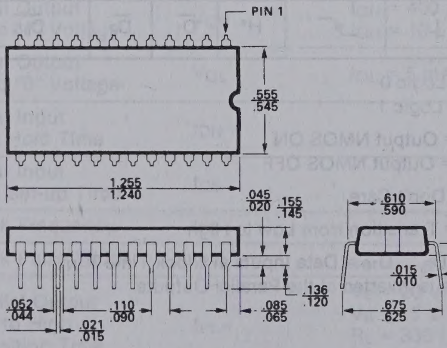

SINGLE BOARD MICROCOMPUTER
(SYM-01)
6522 VIA
CB2
CB1
+5V
SERIAL DATA INPUT
CLOCK
TSC 9404
V+
Q1
Q16
GND
VB
LED BAR GRAPH DISPLAY

Thermal Printhead Driver

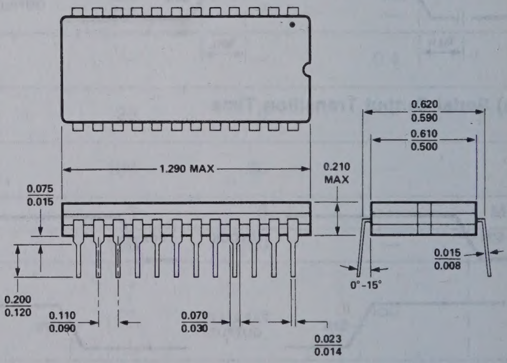

VB
PRINT VOLTAGE
STROBE LINES
THERMAL PRINTHEAD
DOT1
Q1
Q2
Q16
SERIAL INPUT DATA
DATA INPUT
SERIAL OUTPUT
GND
V+
TSC 9403
DATA INPUT
V+
GND
TSC 9403
+5V

Package Outline

Plastic Dip
(Package #12)


PIN 1
.555
.545
1.255
1.240
.045
.020
.155
.145
.610
.590
.075
.065
.015
.010
.136
.120
.052
.044
.110
.090
.021
.015
.085
.065
.675
.625

CerDIP
(Package #14)


0.620
0.590
0.610
0.500
1.290 MAX
0.210
MAX
0.075
0.015
0.015
0.008
0°-15°
0.200
0.120
0.110
0.090
0.070
0.030
0.023
0.014

SECTION 12

References

ection 12

eferences 12-3

SC9491	1.22 V Bandgap Voltage Reference	12-5
SC9495	+5 V Bandgap Voltage Reference/Temperature Transducer	12-7
SC9496	+10 V Bandgap Voltage Reference	12-11

TELEDYNE SEMICONDUCTOR

TSC9491
1.22 V. Bandgap Reference

Features

- Guaranteed temperature coefficient: 50 or 100 ppm/°C
- Low bias current: 50μA
- Low breakdown voltage: 1.22V
- Low dynamic impedance 2Ω max.
- TO-18 or TO-92 package
- Low Cost

Applications

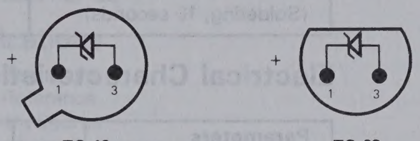
- Reference for A/D and D/A converters
- Threshold detectors
- Voltage Regulators
- VOM and VTVM's
- Amplifier biasing
- Battery operated equipment

General Description

The TSC9491 is a 1.22 V temperature compensated voltage reference. It uses the band-gap principal to achieve extremely tight regulation over a wide range of operating currents. The use of thin film resistors assures long term stability and low noise.

Connection Diagram

Bottom Views



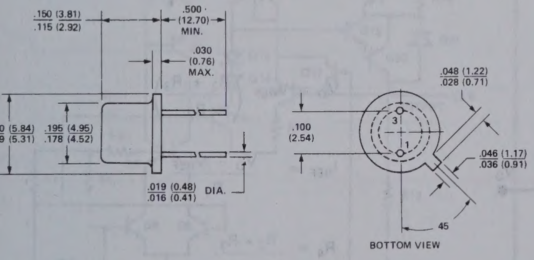
TO-18 **TO-92**

Ordering Information

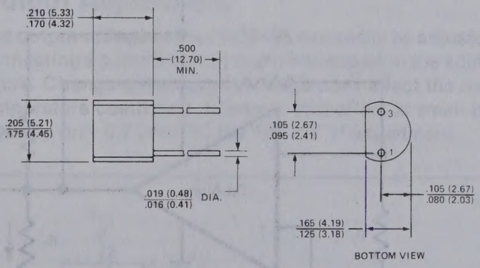
Temp. Coeff.	Temperature Range −55°C to +125°C (TO-18)	 0°C to 70°C (TO-92)
50 ppm/°C	TSC9491AM	TSC9491AJ
100 ppm/°C	TSC9491BM	TSC9491BJ

Packaging Information

TO-18
(2 PIN)


.150 (3.81)
.115 (2.92)
.500
(12.70)
MIN.
.030
(0.76)
MAX.
.230 (5.84)
.209 (5.31)
.195 (4.95)
.178 (4.52)
.019 (0.48)
.016 (0.41)
DIA.
.048 (1.22)
.028 (0.71)
.100
(2.54)
3
1
.046 (1.17)
.036 (0.91)
45
BOTTOM VIEW

TO-92
(2 PIN)


.210 (5.33)
.170 (4.32)
.500
(12.70)
MIN.
.205 (5.21)
.175 (4.45)
.019 (0.48)
.016 (0.41)
DIA.
.105 (2.67)
.095 (2.41)
3
1
.105 (2.67)
.080 (2.03)
.165 (4.19)
.125 (3.18)
BOTTOM VIEW

All dimensions in inches (millimeters)

Absolute Maximum Ratings

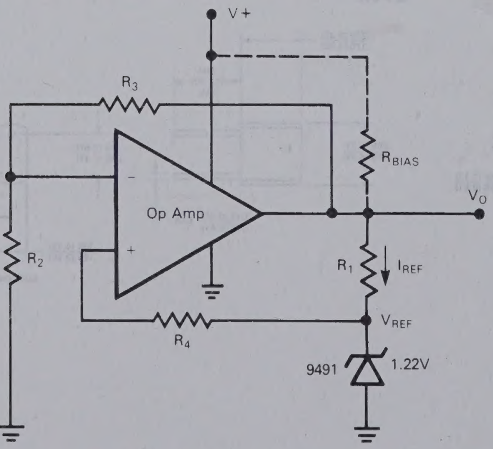
	TO-18	TO-92
Storage Temperature	−65°C to +200°C	−55°C to +150°C
Operating Temperature	−55°C to +125°C	0°C to +70°C
Forward Current, Max.	5mA	5mA
Reverse Current, Max.	1mA	1mA
Power Dissipation	Limited by max forward/reverse current	
Lead Temperature (Soldering, 10 seconds)	300°C	260°C

Electrical Characteristics (T$_A$ = 25°C unless otherwise noted)

Parameters		Min	Typ	Max	Units	Conditions
Reverse Breakdown Voltage	B_{VR}	1.20	1.22	1.25	V	$I_R = 500\mu A$
Reverse Breakdown Voltage Change	ΔB_{VR}	—	15	20	mV	$50\mu A < I_R < 500\mu A$
Temp. Coefficient TSC9491B TSC9491A	$\frac{\Delta B_{VR}}{\Delta T}$		.003 .003	0.01 0.005	%/°C	$I_R = 500\mu A$
Reverse Current	I_R	0.05	—		mA	

Applications/Design Circuits

Adjustable Voltage Reference



$$V_O = V_{REF}\left(\frac{R_2 + R_3}{R_2}\right)$$

$$I_{REF} = \frac{V_O - V_{REF}}{R_1}$$

$$R_4 = \frac{R_2 \cdot R_3}{R_2 + R_3}$$

TELEDYNE SEMICONDUCTOR

TSC9495
+5 V Band Gap Voltage Reference

General Description

The TSC9495, Precision Voltage Reference, uses the band gap principle to generate an extremely stable 5 volt reference. Included in the TSC9495 are a band gap reference, an output amplifier and a voltage which varies linearly with temperature. The reference is ideal because of its low cost, low output noise and low power requirement. The TSC9495 is exceptionally stable over wide variations in temperature, line voltage and load current. The reference operates on a single supply with voltages of 7 volts to 40 volts.

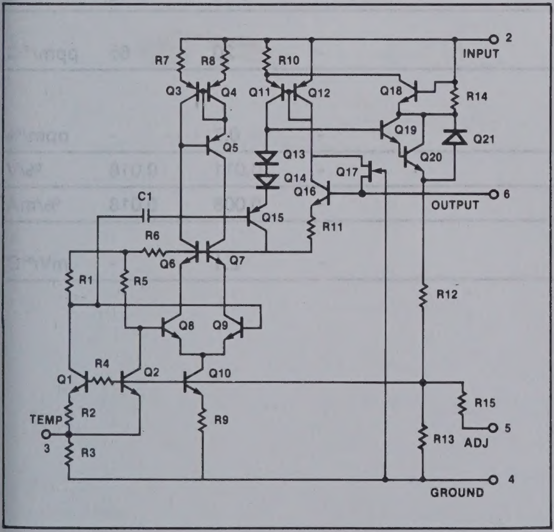
The TSC9495 is available with an initial accuracy of ±1%. An external potentiometer can be used to vary the output voltage ±6% with little effect on the temperature coefficient. The potentiometer can also be used to adjust the voltage for binary applications such as 5.12 volts.

Pin 3 of the TSC9495 has available a voltage which varies linearly with temperature. The typical change is 2.1 mv/°C. By using a buffer amplifier, the output voltage can be scaled to the desired resolution and range.

Ordering Information

Part No.	Package	Max. Voltage	Initial Accuracy	Temp. Range	Max. Temp Coefficient
TSC9495CJ	8-Pin Mini-Dip	30 V	1.0%	0 - 70°C	65 ppm

Schematic Diagram


2
INPUT
R7
R8
R10
Q3
Q4
Q11
Q12
Q18
R14
Q19
Q21
Q5
Q13
Q20
Q14
Q17
Q16
C1
OUTPUT
6
Q15
R11
R6
Q6
Q7
R1
R5
R12
Q8
Q9
R4
Q1
Q2
Q10
R15
TEMP
R2
R9
5
3
R3
R13
ADJ
4
GROUND

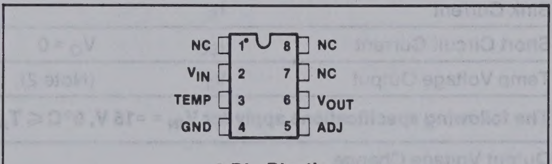
Features

- Excellent Temperature Stability: 20ppm/°C
- Tight Output Tolerance: 1%
- Adjustable Output
- Input Voltage Range: 7V to 40V
- Low Noise: 15 μVpp max.
- 10mA Output Current
- Short Circuit Proof
- Low Power: 1.4mA
- Temperature Output
- Replaces REF-02

Applications

- A/D Reference
- D/A Reference
- Current Source
- Transducer Reference
- Calibration Standard
- Thermometer

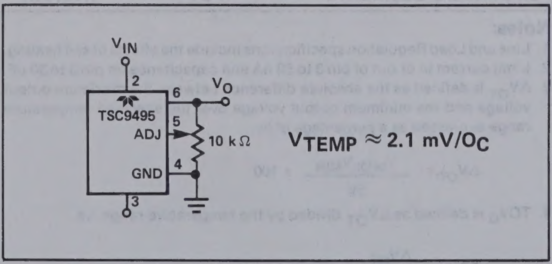
Pin Configuration


NC
1
8
NC
V_{IN}
2
7
NC
TEMP
3
6
V_{OUT}
GND
4
5
ADJ

8 Pin Plastic Mini Dip

Output Adjustment

The output voltage of the TSC9495 can easily be adjusted by connecting a potentiometer to pin 5 as shown in the adjacent figure. Changing the output voltage does affect the overall temperature coefficient, however, this effect is small being typically only 0.7 ppm/°C per 100 mV of adjustment.


V_{IN}
2
6
V_O
TSC9495
5
ADJ
10 kΩ
GND
4
3
$V_{TEMP} \approx 2.1$ mV/O_C

Absolute Maximum Ratings

Input Voltage	30 V	Operating Temperature	0°C to 70°C
Power Dissipation	500 mW	Storage Temperature	−65°C to +150°C
Derating: Mini Dip, above 30°C ambient	5.6mW/°C	Lead Temperature (Soldering, 60 sec.)	300°C

Electrical Characteristics: These specifications apply for V_{IN} = +15 V, T_A = 25°C, unless otherwise noted.

			TSC9495CJ			
PARAMETER	**SYMBOL**	**TEST CONDITION**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	V_O	I_L = 0 mA	4.950	5.000	5.050	V
Output Adjustment Range	ΔV_{trim}	R_p = 10 kΩ	±2.7	±6.0	-	%
Output Voltage Noise	$e_{np\text{-}p}$	0.1 Hz to 10 Hz	-	12	18	μVp-p
Input Voltage Range	V_{IN}		7	-	30	V
Line Regulation (Note 1)		V_{IN} = 8 to 30 V	-	0.009	0.015	5/V
Load Regulation (Note 1)		I_L = 0 to 8 mA	-	0.006	0.015	%/mA
Load Regulation (Note 1)		I_L = 0 to 4 mA	-	-	-	%/mA
Turn-on-Settling Time	t_{on}	To ±0.1% of final value	-	5.0	-	μsec
Quiescent Supply Current	I_{SY}	No Load	-	1.0	1.6	mA
Load Current	I_L		8	21	-	mA
Sink Current	I_S		-0.2	-0.5	-	mA
Short Circuit Current	I_{SC}	V_O = 0	-	30	-	mA
Temp Voltage Output	V_T	(Note 2)	-	630	-	mV

The following specifications apply for V_{IN} = =15 V, 0°C ⩽ T_A ⩽ = 70°C and I_L = 0mA, unless otherwise noted.

Output Voltage Change with Temperature	ΔV_{OT}	(Note 3)	-	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 4)	-	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10 kΩ	-	0.7	-	ppm/%
Line Regulation (Note 1)		V_{IN} = 8 to 30 V	-	0.011	0.018	%/V
Load Regulation (Note 1)		I_L = 0 to 5 mA	-	0.008	0.018	%/mA
Temp Voltage Output Temperature Coefficient	TCV_T	(Note 2)	-	2.1	-	mV/°C

Notes:

1. Line and Load Regulation specifications include the effects of self heating.
2. Limit current in or out of pin 3 to 50 nA and capacitance on pin 3 to 30 pF.
3. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5v:

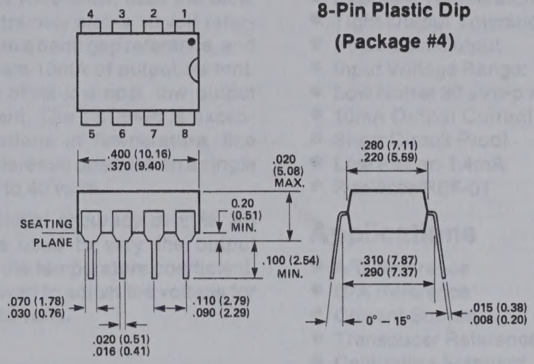
$$\Delta V_{OT} = \frac{V_{MAX}\text{-}V_{MIN}}{5V} \times 100$$

4. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

Package Information

8-Pin Plastic Dip
(Package #4)


4 3 2 1
5 6 7 8
.400 (10.16)
.370 (9.40)
.020 (5.08) MAX.
.280 (7.11)
.220 (5.59)
0.20 (0.51) MIN.
SEATING PLANE
.100 (2.54) MIN.
.310 (7.87)
.290 (7.37)
.070 (1.78)
.030 (0.76)
.110 (2.79)
.090 (2.29)
.020 (0.51)
.016 (0.41)
0° – 15°
.015 (0.38)
.008 (0.20)

12

Notes

TELEDYNE SEMICONDUCTOR

TSC9496
+10 V Band Gap Voltage Reference

General Description

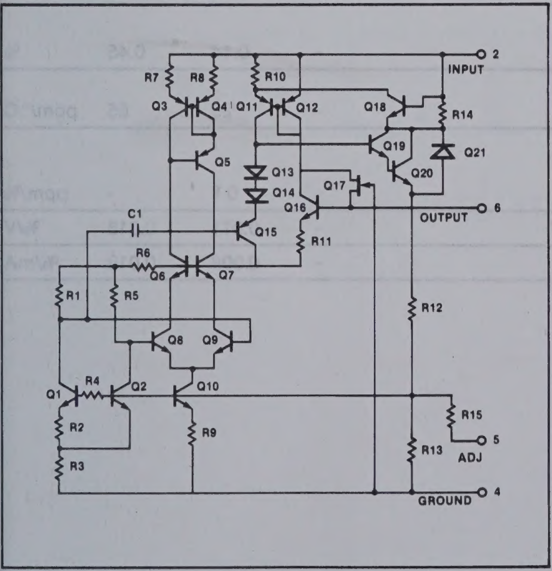
The TSC9496, Precision Voltage Reference, uses the band gap principle to generate an extremely stable 10 volt reference. Included in the TSC9496 are a band gap reference, and an output amplifier, which delivers 10mA of output current. The reference is ideal because of its low cost, low output noise and low power requirement. The TSC9496 is exceptionally stable over wide variations in temperature, line voltage and load current. The reference operates on a single supply with voltages of 12 volts to 40 volts.

The 9496 is available with an initial accuracy of ±1%. An external potentiometer can be used to vary the output voltage ±3% with little effect on the temperature coefficient. The potentiometer can also be used to adjust the voltage for binary applications such as 10.24 volts.

Ordering Information

Part No.	Package	Max. Voltage	Initial Accuracy	Temp. Range	Max. Temp Coefficient
TSC9496CJ	8-Pin Mini-Dip	30 V	1.0%	0 - 70°C	65 ppm

Schematic Diagram


2
INPUT
R7
R8
R10
Q3
Q4
Q11
Q12
Q18
R14
Q5
Q19
Q21
Q13
Q20
Q14
Q17
Q16
6
OUTPUT
C1
Q15
R11
R6
Q6
Q7
R1
R5
R12
Q8
Q9
R4
Q1
Q2
Q10
R15
R2
R9
5
R13
ADJ
R3
4
GROUND

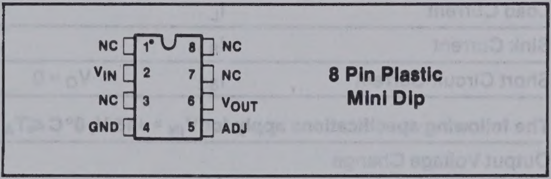
Features

- Excellent Temperature Stability: 20ppm/°C
- Tight Output Tolerance: 1%
- Adjustable Output
- Input Voltage Range: 12V to 40V
- Low Noise: 30 μVp-p max.
- 10mA Output Current
- Short Circuit Proof
- Low Power: 1.4mA
- Replaces REF-01

Applications

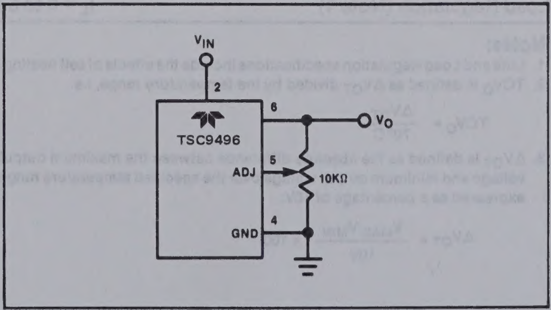
- A/D Reference
- D/A Reference
- Current Source
- Transducer Reference
- Calibration Standard

Pin Configuration


NC 1
V_IN 2
NC 3
GND 4
8 NC
7 NC
6 V_OUT
5 ADJ
8 Pin Plastic Mini Dip

Output Adjustment

The output voltage of the TSC9496 can easily be adjusted by connecting a potentiometer to pin 5 as shown in the figure below. Changing the output voltage does affect the overall temperature coefficient, however, this effect is small being typically only 0.7 ppm/°C per 100 mV of adjustment.


V_IN
2
TSC9496
6
V_O
5
ADJ
10KΩ
4
GND

Absolute Maximum Ratings

Input Voltage	30 V	Operating Temperature	0°C to 70°C
Power Dissipation	500 mW	Storage Temperature	−65°C to +150°C
Derating: Mini Dip, above 30°C ambient	5.6mW/°C	Lead Temperature (Soldering, 60 sec.)	300°C

Electrical Characteristics:

These specifications apply for V_{IN} = +15 V, T_A = 25°C, unless otherwise noted.

			TSC9496CJ			
PARAMETER	**SYMBOL**	**TEST CONDITION**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	V_O	I_L = 0 mA	9.90	10.000	10.10	V
Output Adjustment Range	ΔV_{trim}	R_p = 10 kΩ	±2.7	±3.3	-	%
Output Voltage Noise	$e_{np\text{-}p}$	0.1 Hz to 10 Hz	-	25	35	μVp-p
Input Voltage Range	V_{IN}		12	-	30	V
Line Regulation (Note 1)		V_{IN} = 13 to 30 V	-	0.009	0.015	%/V
Load Regulation (Note 1)		I_L = 0 to 8 mA	-	0.006	0.015	%/mA
Load Regulation (Note 1)		I_L = 0 to 4 mA	-	0.006	0.015	%/mA
Turn-on-Settling Time	t_{on}	To ±0.1% of final value	-	5.0	-	μsec
Quiescent Supply Current	I_{SY}	No Load	-	1.0	1.6	mA
Load Current	I_L		8	21	-	mA
Sink Current	I_S		-0.2	-0.5	-	mA
Short Circuit Current	I_{SC}	V_O = 0	-	30	-	mA
The following specifications apply for V_{IN} = +15 V, 0°C $\leqslant T_A \leqslant$ + 70°C, unless otherwise noted.						
Output Voltage Change with Temperature	ΔV_{OT}	(Note 3)	-	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 4)	-	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10 kΩ	-	0.7	-	ppm/%
Line Regulation (Note 1)		V_{IN} = 13 to 30 V	-	0.011	0.018	%/V
Load Regulation (Note 1)		I_L = 0 to 5 mA	-	0.008	0.018	%/mA

Notes:

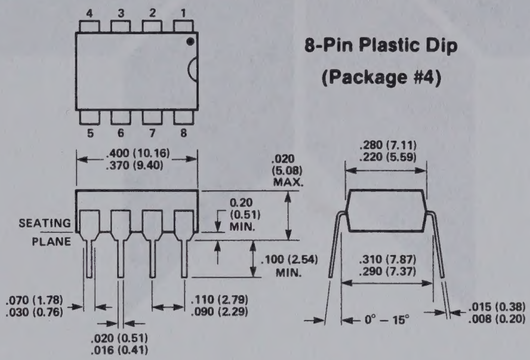
1. Line and Load Regulation specifications include the effects of self heating.
2. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

3. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and minimum output voltage over the specified temperature range expressed as a percentage of 10V:

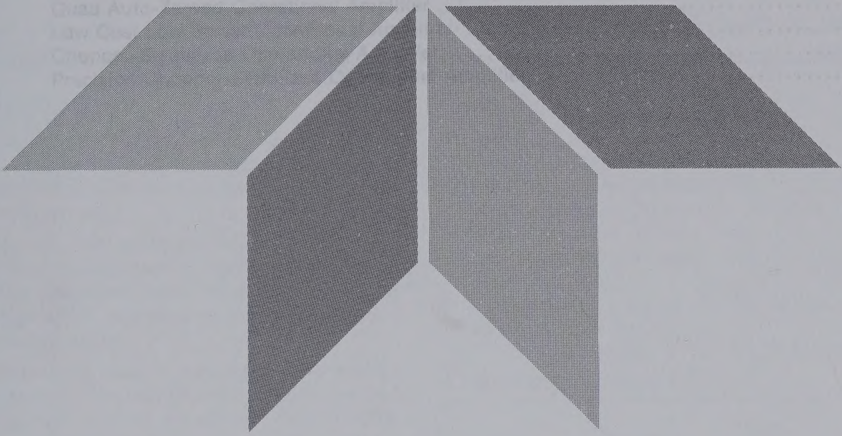
$$\Delta V_{OT} = \frac{V_{MAX}\text{-}V_{MIN}}{10V} \times 100$$

Package Information


8-Pin Plastic Dip
(Package #4)

4 3 2 1
5 6 7 8
.400 (10.16)
.370 (9.40)
.020
(5.08)
MAX.
0.20
(0.51)
MIN.
SEATING
PLANE
.100 (2.54)
MIN.
.070 (1.78)
.030 (0.76)
.020 (0.51)
.016 (0.41)
.110 (2.79)
.090 (2.29)
.280 (7.11)
.220 (5.59)
.310 (7.87)
.290 (7.37)
0° – 15°
.015 (0.38)
.008 (0.20)

Notes



SECTION 13

Operational Amplifiers

Section 13

Operational Amplifiers 13-3

TSC900 Low Power Chopper-Stabilized Operational Amplifier 13-5
TSC911 Auto-Zeroed Monolithic Operational Amplifier 13-13
TSC913 Dual Auto-Zeroed Operational Amplifier 13-21
TSC914 Quad Auto-Zeroed Operational Amplifier 13-23
TSC918 Low Cost Low Power Operational Amplifier 13-25
TSC7650A Chopper-Stablilized Operational Amplifier 13-29
TSC7650 Precision Chopper-Stabilized Operational Amplifier 13-37

TELEDYNE SEMICONDUCTOR

Preliminary

TSC900
Low Power Chopper-Stabilized Operational Amplifier

- 2 mW Power Dissipation
- 0.05 μV/°C Offset Voltage Drift

General Description

The TSC900 is a low power precision operational amplifier. The 200 μA maximum supply current reduces device power requirement by over fifteen times when compared to the pin compatible ICL7650 device.

Offset voltage is a low 5 μV with drift at 0.05 μV/°C. V_{OS} errors are removed and adjustment potentiometers made unnecessary. The chopper stabilized error correction technique keeps offset voltage errors near zero throughout the device operating temperature range.

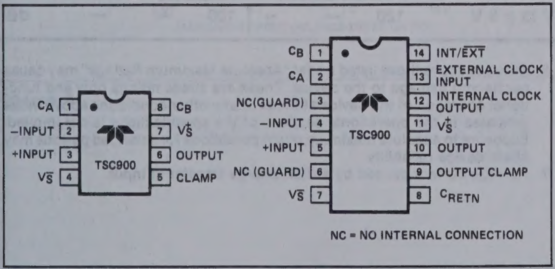
The TSC900 performance advantages are achieved without the additional manufacturing complexity and cost incurred with laser or "zener zap" V_{OS} trim techniques. The TSC900 is one of the lowest cost low power precision operational amplifiers available.

The TSC900 nulling scheme corrects both DC V_{OS} errors and V_{OS} drift errors with temperature. A nulling amplifier alternately corrects its own V_{OS} errors and the main amplifier V_{OS} error. Offset nulling voltages are stored on two user supplied external capacitors. The capacitors connect to the internal amplifier V_{OS} null points. The main amplifier input signal is never switched. Switching spikes are not present at the TSC900 output. The null scheme keeps V_{OS} errors low throughout the operating temperature range. Laser and "zener zap" trimming can correct for V_{OS} at only one temperature.

The nulling circuit oscillator and control circuits are integrated on chip. Only two external V_{OS} error storage capacitors are required. The TSC900 operates as a conventional operational amplifier with vastly improved input specifications. The low V_{OS} and V_{OS} drift errors make the TSC900 ideal for thermocouple, thermistor, and strain gauge applications. Low dc errors and high open loop gain make the TSC900 an excellent preamplifier for precision analog to digital converters like the TSC7135, TSC800 and TSC7109.

The 14-pin dual-in-line package (DIP) has an external oscillator input to drive the nulling circuitry. Both the 8 and 14-pin DIP have an output voltage clamp circuit to minimize overload recovery time.

Pin Configuration


C_A 1
−INPUT 2
+INPUT 3
V_S^- 4
8 C_B
7 V_S^+
6 OUTPUT
5 CLAMP
TSC900
C_B 1
C_A 2
NC(GUARD) 3
−INPUT 4
+INPUT 5
NC (GUARD) 6
V_S^- 7
14 INT/$\overline{\text{EXT}}$
13 EXTERNAL CLOCK INPUT
12 INTERNAL CLOCK OUTPUT
11 V_S^+
10 OUTPUT
9 OUTPUT CLAMP
8 C_{RETN}
TSC900

NC = NO INTERNAL CONNECTION

Features

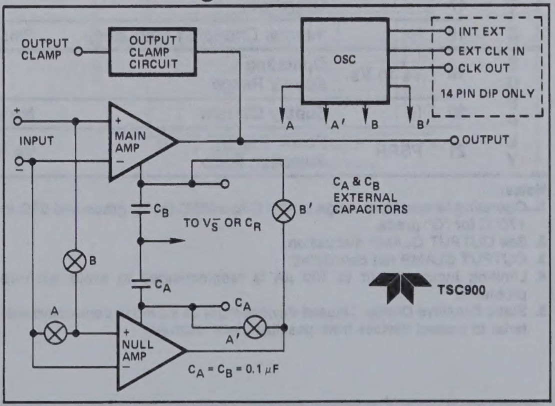
- Low Power Supply Current .... 140 μA
- Low Input Offset Voltage .... 5 μV Max.
- Low Input Offset Voltage Drift .... 0.05 μV/°C Max.
- High Impedance Differential CMOS Inputs ..... 10^{12} Ω
- High Open Loop Voltage Gain .... 120 dB Min.
- Low Input Noise Voltage .... 0.3 μVp-p
- High Slew Rate .... 0.2 V/μs
- Compensated Internally for Stable Unity Gain Operation
- Available in 8-Pin Dip
- Pin Compatible to ICL7650/TSC7650A/TSC7650

Ordering Information

Part No.	Package	Temp. Range	Max. V_{OS}	Max. Supply Current
*TSC900ACPA	8-Pin Plastic Dip	COM	5 μV	200 μA
*TSC900AIJA	8-Pin CerDIP	IND	5 μV	200 μA
*TSC900ACPD	14-Pin Plastic Dip	COM	5 μV	200 μA
*TSC900AIJD	14-Pin CerDIP	IND	5 μV	200 μA
*TSC900BCPA	8-Pin Plastic Dip	COM	15 μV	400 μA
*TSC900BIJA	8-Pin CerDIP	IND	15 μV	400 μA
*TSC900BCPD	14-Pin Plastic Dip	COM	15 μV	400 μA
*TSC900BIJD	14-Pin CerDIP	IND	15 μV	400 μA

*Available with 160 hour, +125°C burn-in. Add /BI to part number suffix.

Functional Diagram


OUTPUT CLAMP
OUTPUT CLAMP CIRCUIT
OSC
INT EXT
EXT CLK IN
CLK OUT
14 PIN DIP ONLY
A
A′
B
B′
+
INPUT
−
+
MAIN AMP
−
OUTPUT
C_B
B′
C_A & C_B EXTERNAL CAPACITORS
TO V_S^- OR C_R
B
C_A
A
C_A
A′
+
NULL AMP
−
TSC900
$C_A = C_B = 0.1\ \mu$F

©1984

TSC900

Low Power Chopper-Stablized Operational Amplifier

• 2 mW Power Dissipation
• 0.05 μV/°C Offset Voltage Drift

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-) .... 18 Volts
Input Voltage .... (V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range .... -55°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C
Voltage on Oscillator Control Pins .... V_S^+ to V_S^-
Output Short Circuit Duration .... Indefinite
Current into Any Pin .... 10 mA
While Operating (Note 4) .... 100 μA
Operating Temp. Range
I Device .... -25°C to +85°C
C Device .... 0°C to +70°C
Package Power Dissipation (T_A = 25°C)
CerDIP Package .... 500 mV
Plastic Package .... 500 mW

Electrical Characteristics: $V_S^+ = +5$ V, $V_S^- = -5$ V, $C_A = C_B = 0.1$ μf. $T_A = 25°$C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC900A MIN	TSC900A TYP	TSC900A MAX	TSC900B MIN	TSC900B TYP	TSC900B MAX	UNIT
INPUT	1	V_{OS}	Input Offset Voltage	$T_A = +25°C$	—	—	5	—	—	15	μV
	2	$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Average Temp. Coefficient	Operating Temp Range (Note 1)	—	0.02	0.05	—	0.1	0.3	μV/°C
	3	I_{BIAS}	Average	$T_A = +25°C$	—	—	50	—	—	80	pA
			Input Bias Current	$0°C \leq T_A \leq +70°C$	—	—	70	—	—	100	
			(Note 7)	$-25°C \leq T_A \leq +85°C$	—	—	100	—	—	140	
	4	I_{OS}	Input Offset Current	$T_A = 25°C$	—	0.5	—	—	0.5	—	pA
	5	$e_{np\text{-}p}$	Input Noise Voltage	$R_S = 100\Omega$ 0.1 to 10 Hz	—	4	—	—	4	—	$\mu V_{p\text{-}p}$
	6	$e_{np\text{-}p}$	Input Noise Voltage	$R_S = 100\Omega$ 0.1 Hz to 1 Hz	—	0.3	—	—	0.3	—	$\mu V_{p\text{-}p}$
	7	R_{IN}	Input Resistance		—	10^{12}	—	—	10^{12}	—	Ω
	8	CMVR	Common-Mode Voltage Range		-5.0	—	+1.5 V	-5.0	—	+1.5	V
	9	CMRR	Common-Mode Rejection Ratio	CMVR = -5 V to +1. 5 V	110	130	—	100	—	—	dB
OUTPUT	10	A_V	Large-Signal Voltage Gain	$R_L = 10$ kΩ	120	130	—	100	—	—	dB
	11	V_{OUT}	Output Voltage Swing	$R_L = 10$ kΩ	-4.7	—	+3.5	-4.7	—	+3.5	V
			(Note 3)	$R_L = 100$ kΩ	-4.9	—	+3.9	-4.9	—	+3.9	
	12		Clamp ON Current (Note 2)	$R_L = 100$ kΩ	20	90	200	20	90	200	μA
	13		Clamp OFF Current (Note 2)	$-4.0 V < V_{OUT} < +4.0 V$	—	1	—	—	1	—	pA
DYNAMIC	14	B_W	Unity Gain Bandwidth	Unity Gain (+1)	—	0.7	—	—	0.7	—	MHz
	15	S_R	Slew Rate	$C_L = 50$ pF, $R_L = 100$k	—	0.2	—	—	0.2	—	V/μs
	16		Rise Time		—	0.5	—	—	0.5	—	μs
	17		Overshoot		—	18	—	—	18	—	%
	18	f_{ch}	Internal Chopping Frequency	Pins 12-14 open (DIP)	—	150	—	—	150	—	Hz
SUPPLY	19	V_S^+ to V_S^-	Operating Supply Range		4.5	—	16	4.5	—	16	V
	20	I_S	Supply Current	No Load	—	140	200	—	—	400	μA
	21	PSRR	Power Supply Rejection Ratio	$V_S = \pm 3$ V to ± 8 V	120	—	—	100	—	—	dB

Notes:

1. Operating temperature range is -25°C to +85°C for "I" grade and 0°C to +70°C for "C" grade.
2. See OUTPUT CLAMP discussion.
3. OUTPUT CLAMP not connected.
4. Limiting input current to 100 μA is recommended to avoid latch-up problems.
5. Static Sensitive Device. Unused devices must be stored in conductive material to protect devices from possible static damage.
6. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
7. Average current caused by switch charge transfer at input.

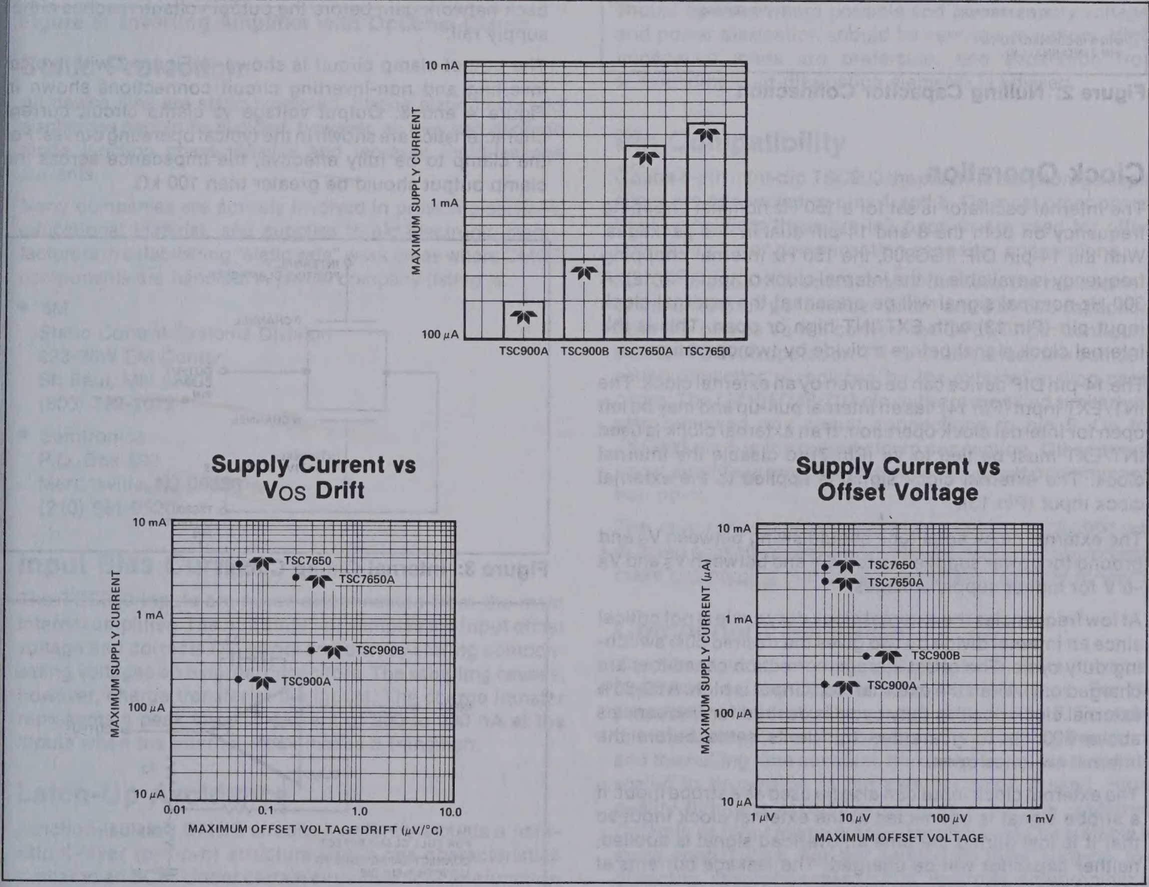
Chopper Stabilized Operational Amplifiers

The TSC900 is the first low power chopper stabilized amplifier commercially available. The TSC900 maximum supply current is 15 times lower than the pin compatible TSC7650 amplifier. As Figure 1 shows the low supply current is achieved without sacrificing offset voltage or offset voltage drift performance.

Nulling Capacitor Connection

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (Pin 4) on the 8-pin packages and to capacitor return (C_R, Pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops.

Internally V_S^- is connected to C_R.



Supply Current vs V_{OS} Drift

Supply Current vs Offset Voltage

Figure 1

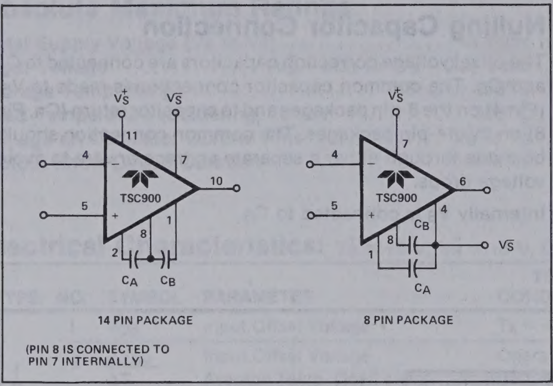


Figure 2: Nulling Capacitor Connection

Clock Operation

The internal oscillator is set for a 150 Hz nominal chopping frequency on both the 8 and 14-pin dual in line packages. With the 14-pin DIP TSC900, the 150 Hz internal chopping frequency is available at the internal clock output (Pin 12). A 300 Hz nominal signal will be present at the external clock input pin (Pin 13) with EXT/INT high or open. This is the internal clock signal before a divide by two operation.

The 14-pin DIP device can be driven by an external clock. The INT/EXT input (Pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used INT/EXT must be tied to V_S^- (Pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (Pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6 V and between V_S^+ and V_S^+ -6 V for higher supply voltages.

At low frequencies the external clock duty cycle is not critical since an internal divide by two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50-80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitor pins are very low.

Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TSC900 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3 with typical inverting and non-inverting circuit connections shown in Figure 4 and 5. Output voltage vs clamp circuit current characteristics are shown in the typical operating curves. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 kΩ.

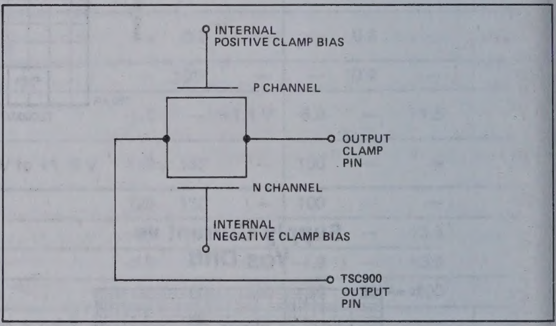
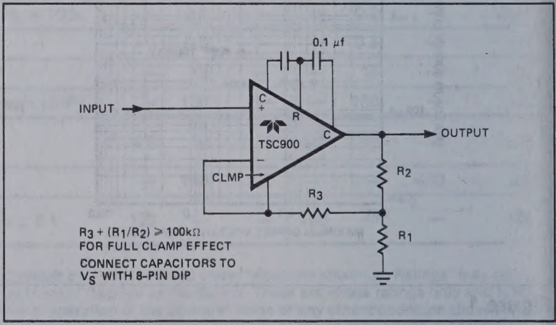


Figure 3: Internal Clamp Circuit



$R_3 + (R_1/R_2) \geq 100k\Omega$
FOR FULL CLAMP EFFECT

CONNECT CAPACITORS TO
V_S^- WITH 8-PIN DIP

Figure 4: Non-Inverting Amplifier with Optional Clamp

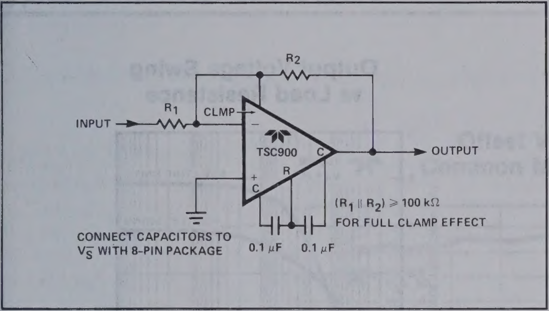


Figure 5: Inverting Amplifier with Optional Clamp

Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational material, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520

Input Bias Current

The TSC900 inputs are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. The sampling causes, however, charge transfer at the inputs. The charge transfer represents a peak impulse current of 200 to 290 nA at the inputs when the internal clock makes a transition.

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low impedance state, resulting in excessive supply current. To avoid the condition, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latchup.

Thermo-Electric Potentials

Precision dc measurements are ultimately limited by thermo-electric potentials developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1 μV/° C, but up to tens of μV/° C for some materials, will be generated. In order to realize the benefits extremely low offset voltages provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially those caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and separation from surrounding heat-dissipating elements is advised.

Pin Compatibility

On the 8-pin mini-dip TSC900 the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or are used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, the replacement of the offset null pot between pins 1 and 8 by two capacitors from the pins to V_S^- will convert the OP05/07 pin configuration for TSC900 operation. For LM108 devices the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pin outs are modified similarly by also removing any circuit connections to pin 5. On the TSC900 pin 5 is the output clamp connection. Other operational amplifiers may use this pin as an offset or compensation point.

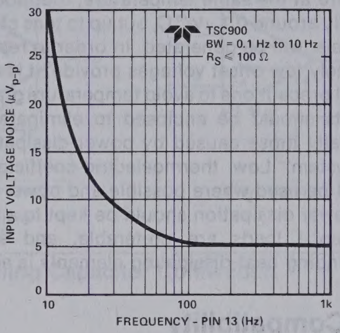
The minor modifications needed to retrofit a TSC900 into existing sockets operating at reduced power supply voltages make prototyping and circuit verification straight forward.

Component Selection

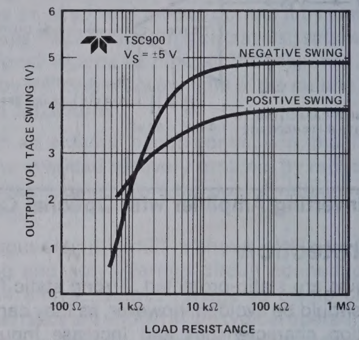
The two required capacitors, C_A C_B, have optimum values depending on the clock or chopping frequency. For the present internal clock, the correct value is 0.1 μF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock if used. High-quality film-type capacitors such as mylar are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to microvolt levels.

Typical Characteristic Curves

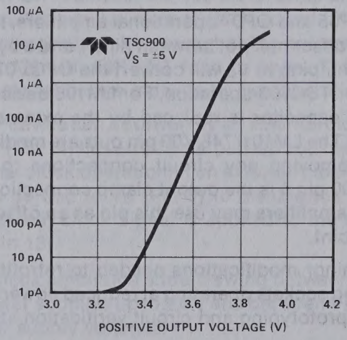
Input Voltage Noise vs External Clock Frequency (Pin 13)



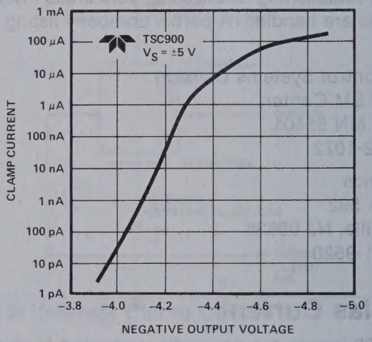
Output Voltage Swing vs Load Resistance



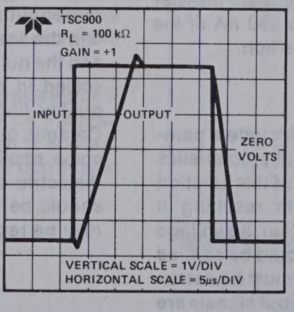
Positive Clamp Current



Negative Clamp Current



Slew Rate

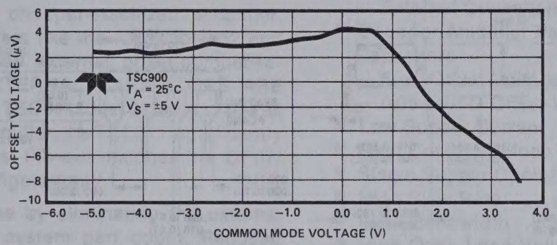


ow Power Chopper-Stablized
)perational Amplifier
2 mW Power Dissipation
0.05 μV/° C Offset Voltage Drift

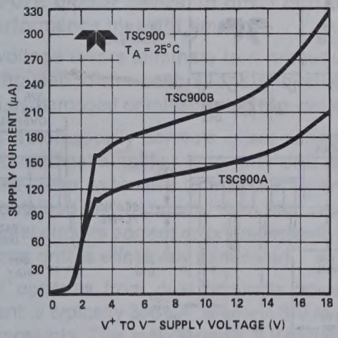
TSC900

'ypical Characteristic Curves

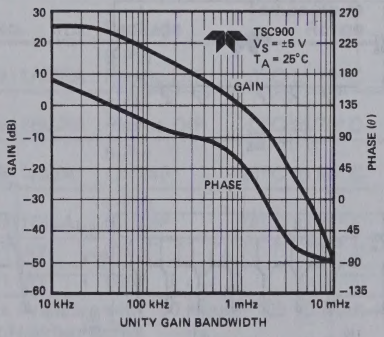
Offset Voltage vs Common Mode Voltage



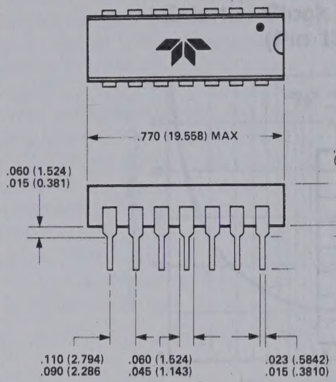
Supply Current vs Supply Voltage



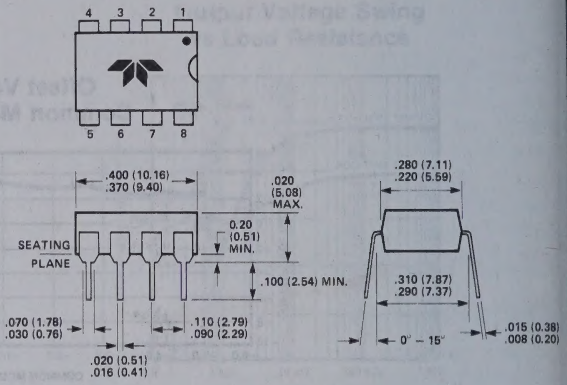
Gain and Phase vs Frequency



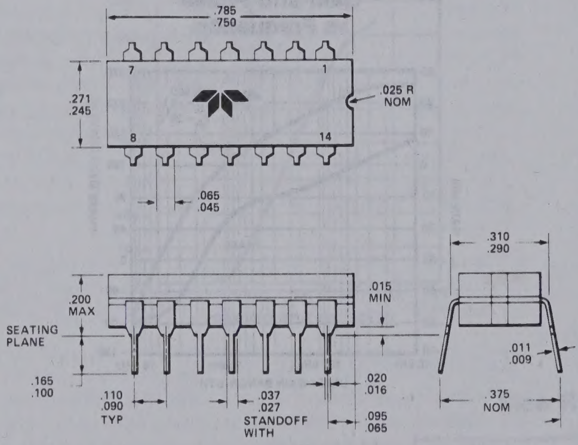
Package Outline


.310 (7.874)
.280 (7.112)
.235 (5.969)
.215 (5.461)
.770 (19.558) MAX
.160 MAX
(4.064)
.060 (1.524)
.015 (0.381)
.160 (4.064)
.100 (2.540)
.015 (0.381)
.008 (0.2032)
.110 (2.794)
.090 (2.286
.060 (1.524)
.045 (1.143)
.023 (.5842)
.015 (.3810)
.400 (10.160)
.330 (8.382)

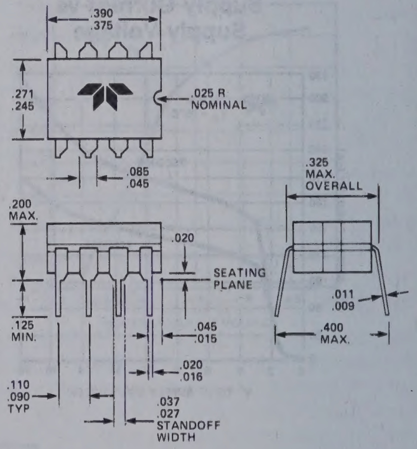
14-Pin Plastic Package
(Package #6)


4 3 2 1
5 6 7 8
.400 (10.16)
.370 (9.40)
.020
(5.08)
MAX.
0.20
(0.51)
MIN.
SEATING
PLANE
.100 (2.54) MIN.
.070 (1.78)
.030 (0.76)
.110 (2.79)
.090 (2.29)
.020 (0.51)
.016 (0.41)
.280 (7.11)
.220 (5.59)
.310 (7.87)
.290 (7.37)
0° – 15°
.015 (0.38)
.008 (0.20)

8-Pin Plastic Package
(Package #4)


.785
.750
7
1
8
14
.271
.245
.025 R
NOM
.065
.045
.200
MAX
SEATING
PLANE
.015
MIN
.165
.100
.110
.090
TYP
.037
.027
STANDOFF
WITH
.020
.016
.095
.065
.310
.290
.011
.009
.375
NOM

14-Pin CerDIP Package
(Package #7)


.390
.375
.271
.245
.025 R
NOMINAL
.085
.045
.325
MAX.
OVERALL
.200
MAX.
.020
SEATING
PLANE
.125
MIN.
.045
.015
.011
.009
.400
MAX.
.020
.016
.110
.090
TYP
.037
.027
STANDOFF
WIDTH

8-Pin CerDIP Package
(Package #5)

TELEDYNE SEMICONDUCTOR

Preliminary

TSC911

Auto-Zeroed Monolithic Operational Amplifier

- **No External Chopper Capacitors**
- **3.5 mW Power Dissipation**
- **5 μV Offset Voltage**

General Description

The CMOS TSC911 auto-zeroed operational amplifier is the first complete monolithic chopper-stabilized amplifier. Chopper operational amplifiers like the ICL7650/7652 and LTC1052 require user supplied, external, offset compensation storage capacitors. EXTERNAL CAPACITORS ARE NOT REQUIRED WITH THE TSC911. Just as easy to use as the conventional 741 type amplifier, the TSC911 significantly reduces offset voltage errors. Pin-out matches the OP07/741/7650 8-pin mini-dip configuration.

Several system benefits arise by eliminating the external chopper capacitors. Lower system part count. Reduced assembly time and cost. Greater system reliability. Reduced printed circuit board layout effort and greater pc board area utilization. Space savings can be significant in multiple amplifier designs.

Electrical specifications include a 15 μV maximum offset voltage, 0.15 μV/°C maximum offset voltage temperature coefficient. Offset voltage error is five times lower than the premium OP07E bipolar device. In offset drift the TSC911 improves performance by eight times.

Low offset voltage errors eliminate trim procedures during manufacturing, periodic re-calibrations, and reliability problems caused by damaged or misadjusted trim potentiometers.

The TSC911 automatically corrects offset voltage drift with time also. Operational amplifier long term drift is less easily controlled and more expensive to maintain when low offset errors are obtained by trimming thin film resistors. The TSC911 internal circuits correct errors repetitively at a 200 Hz rate. Long term drift is effectively eliminated.

The TSC911 operates from dual or single power supplies. Supply current is typically 350 μA. Single 4.5 V to 16 V supply operation is possible. This makes single 9 V battery operation possible. The TSC7660 DC to DC converter can easily supply a negative potential in dual supply applications where only a +5 V system supply is available.

Open-loop voltage gain is 115 dB minimum with a 10 kΩ load. Unity gain bandwidth is 1.5 MHz. Slew rate is 2.5 V/μs. Common-mode rejection ratio is 110 dB. Input common-mode range extends from 2 V below the positive supply to the negative supply.

The TSC911 is available in an 8-pin plastic or cerDIP package. Dice are available for hybrid applications.

For precision dual and quad monolithic chopper-stabilized amplifiers see the TSC913 dual and TSC914 quad data sheets.

Features

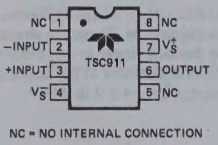
- First Monolithic Chopper-Stabilized Amplifier
  — External Capacitors Not Required
- Chopper Amplifier Performance Without External Capacitors
  — 5 μV Offset Voltage
  — 0.05 μV/°C Offset Voltage Drift
- Low Supply Current .... 350 μA
- High Common-Mode Rejection .... 116 dB
- Single Supply Operation .... 4.5 V to 16 V
- High Slew Rate .... 2.5 V/μs
- Wide Bandwidth .... 1.5 MHz
- High Open Loop Voltage Gain (R_L = 10 kΩ) ... 120 dB
- Low Input Voltage Noise (0.1 to 1 Hz) ...... 0.65 μV_{P-P}
- Pin Compatible with ICL7650
- Lower System Part Count

Ordering Information

Part No.	Package	Temperature Range	Max. Offset Voltage
*TSC911ACPA	8-Pin Plastic DIP	0° C to 70° C	15 μV
*TSC911BCPA	8-Pin Plastic DIP	0° C to 70° C	30 μV
*TSC911AIJA	8-Pin CerDIP	-25° C to 85° C	15 μV
*TSC911BIJA	8-Pin CerDIP	-25° C to 85° C	30 μV
TSC911AY	Chip	25° C	15 μV
TSC911BY	Chip	25° C	30 μV

* Parts Available with 160 Hour, +125 °C Burn-In. Add /BI to Part Number Suffix.

Pin Configuration



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Auto-Zeroed Monolithic Operational Amplifier

- **No External Chopper Capacitors**
- **3.5 mW Power Dissipation**
- **5 μV Offset Voltage**

TSC911

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-)	18 Volts
Input Voltage	(V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range	-55 °C to 150 °C
Lead Temperature (Soldering, 10 sec)	300 °C
Current into Any Pin	10 mA

Operating Temp. Range	
I Device	-25 °C to +85 °C
C Device	0 °C to +70 °C
Package Power Dissipation (T_A = 25 °C)	
CerDIP Package	500 mW
Plastic Package	375 mW

Electrical Characteristics: V_S = ±5 V, T_A = 25° C unless otherwise indicated.

				TSC911A			TSC911B			
NO.	**SYMBOL**	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
1	V_{OS}	Input Offset Voltage	T_A = 25° C	—	5	15	—	15	30	μV
2	V_{OS}/T	Average Temperature Coefficient of Input Offset Voltage	0° C ≤ T_A ≤ 70° C -25° C ≤ T_A ≤ 85° C	— —	0.05 0.05	0.15 0.15	— —	0.1 0.1	0.25 0.25	μV/° C μV/° C
3	I_B	Average Input Bias Current	T_A = 25° C 0° C ≤ T_A ≤ 70° C -25° C ≤ T_A ≤ 85° C	— — —	— — —	70 3 4	— — —	— — —	120 4 6	pA nA nA
4	I_{OS}	Average Input	Offset Current	—	5	20	—	10	40	pA
5	en	Input Voltage Noise	0.1 to 1.0Hz, R_S ≤ 100Ω	—	0.65	—	—	0.65	—	μV_{P-P}
6	en	Input Voltage Noise	0.1 to 10 Hz, R_S ≤ 100 Ω	—	11	—	—	11	—	μV_{P-P}
7	CMRR	Common-Mode Rejection Ratio	V_S^- ≤ V_{CM} ≤ V_S^+ - 2.2	110	116	—	105	110	—	dB
8	CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+ -2.0	V_S^-	—	V_S^+ -2.0	V
9	A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_O = ±4 V	115	120	—	110	120	—	dB
10	V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^- + .3 V	—	V_S^+ -.9 V	V_S^- + .3 V	—	V_S^+ -.9 V	V
11	BW	Closed Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
12	SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pf	—	2.5	—	—	2.5	—	V/μs
13	PSRR	Power Supply Rejection	±3.3 V to ± 5.5 V	112	—	—	105	—	-	dB
14	V_S	Operating Supply Voltage	Range (Note 3)	±3 V	—	±8 V	±3 V	—	±8 V	V
15	I_S	Quiescent Supply Current	V_S = ±5 V	—	350	600	—	—	800	μA

Notes:

1. Static Sensitive Device. Unused devices should be stored in conductive material.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.
3. Single Supply Operation: V_S^+ = +4.5 V to +16 V.

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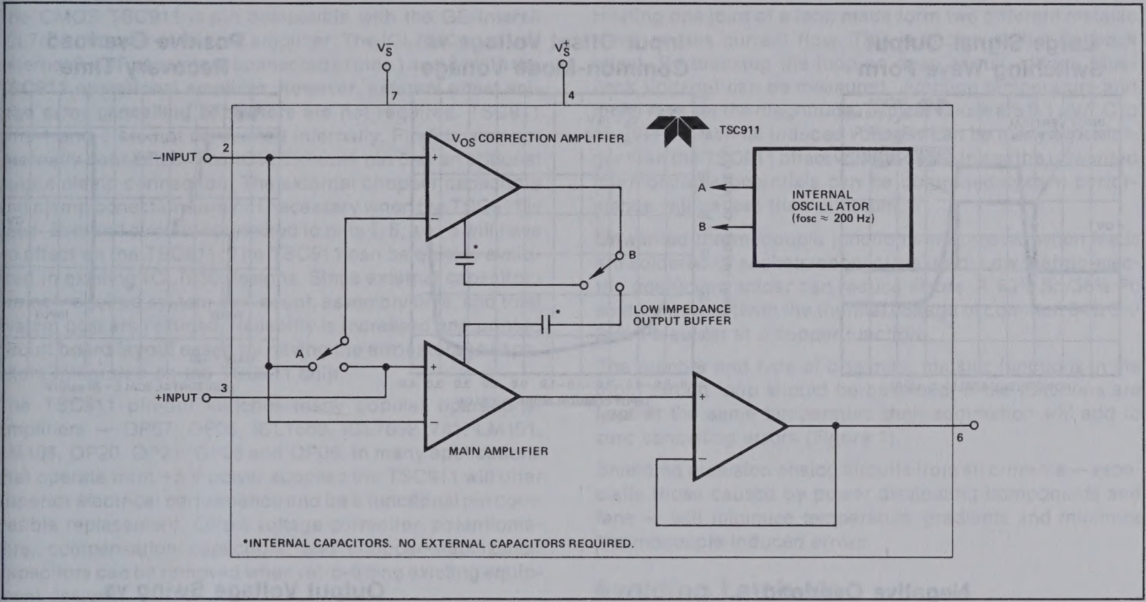
Auto-Zeroed Monolithic Operational Amplifier

- **No External Chopper Capacitors**
- **3.5 mW Power Dissipation**
- **5 μV Offset Voltage**

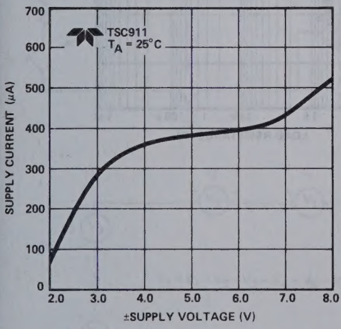
Functional Diagram


V_S^-
7
V_S^+
4
TSC911
−INPUT
2
V_{OS} CORRECTION AMPLIFIER
A
B
INTERNAL OSCILLATOR (fosc ≈ 200 Hz)
*
B
LOW IMPEDANCE OUTPUT BUFFER
*
A
+INPUT
3
MAIN AMPLIFIER
6

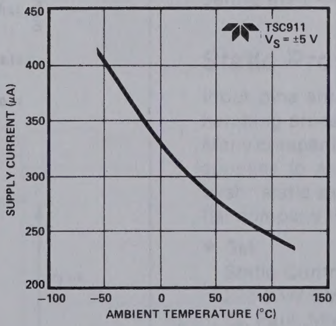
*INTERNAL CAPACITORS. NO EXTERNAL CAPACITORS REQUIRED.

Typical Characteristic Curves

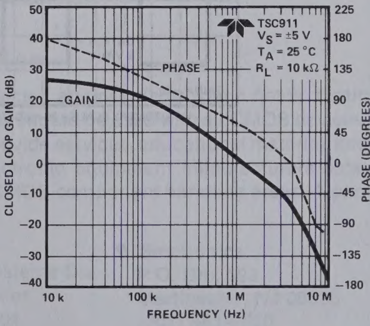
Supply Current vs ± Supply Voltage



Supply Current vs Temperature



Gain vs Phase



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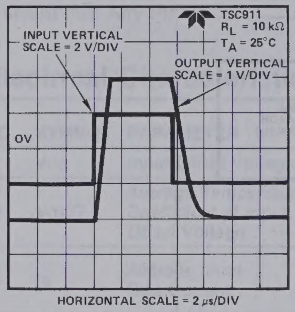
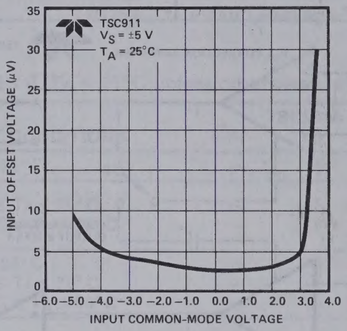
Typical Characteristic Curves (Cont.)

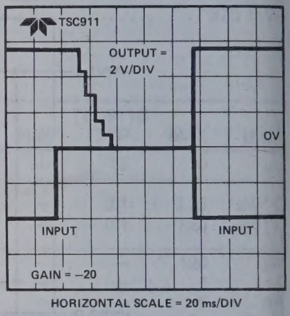
Large Signal Output Switching Wave Form



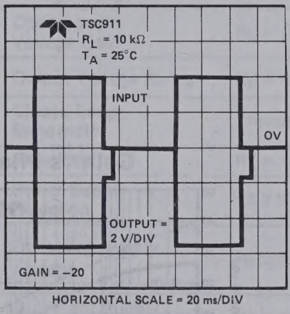
Input Offset Voltage vs Common-Mode Voltage



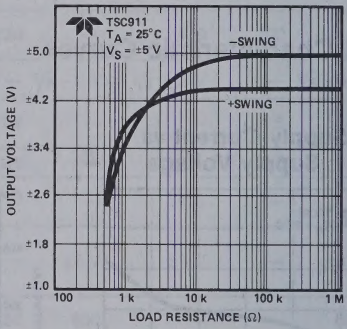
Positive Overload Recovery Time



Negative Overload Recovery Time



Output Voltage Swing vs Load Resistance



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uto-Zeroed Monolithic perational Amplifier

No External Chopper Capacitors
3.5 mW Power Dissipation
5 μV Offset Voltage

in Compatibility

he CMOS TSC911 is pin compatible with the GE/Intersil CL7650 chopper-stabilized amplifier. The ICL7650 must use xternal 0.1 μF capacitors connected at pins 1 and 8. **With the SC911 operational amplifier, however, external offset volge error cancelling capacitors are not required.** TSC911 ins 1 and 8 are not connected internally. Pin 5 is also not nternally connected. The ICL7650 uses pin 5 as an optional utput clamp connection. The external chopper capacitors nd clamp conections are not necessary when the TSC911 is sed. External circuits connected to pins 1, 8, and 5 will have o effect on the TSC911. The TSC911 can be quickly evaluted in existing ICL7650 designs. Since external capacitors re not required system part count, assembly time, and total ystem cost are reduced. Reliabilty is increased and printed ircuit board layout eased by having the error storage capaitors integrated on the TSC911 chip.

The TSC911 pin-out matches many popular operational mplifiers — OP07, OP05, ICL7650, ICL7652, 741, LM101, M108, OP20, OP21, OP08 and OP06. In many applications hat operate from +5 V power supplies the TSC911 will offer superior electrical performance and be a functional pin compatible replacement. Offset voltage correction potentiometers, compensation capacitors, and chopper-stabilization capacitors can be removed when retro-fitting existing equipment designs.

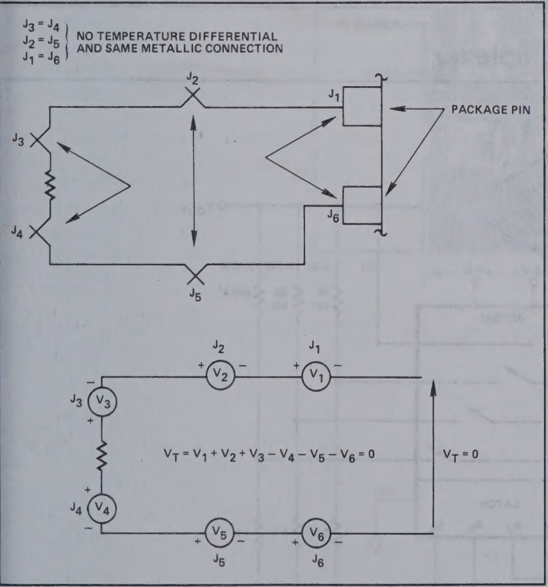

Figure 1: Unwanted Thermocouple Errors Eliminated by Reducing Thermal Gradients and Balancing Junctions.

Thermocouple Errors

Heating one joint of a loop made form two different metallic wires causes current flow. This is known as the Seebeck effect. By breaking the loop an open circuit voltage (Seebeck Voltage) can be measured. Junction temperature and metal type set the magnitude. Typical values are 0.1 μV/° C to 10 μV/° C. Thermal induced voltages can be many times larger than the TSC911 offset voltage drift. Unless the unwanted thermocouple potentials can be controlled system performance will be less than optimum.

Unwanted thermocouple junctions are created when leads are soldered or sockets/connectors used. Low thermo-electric coefficient solder can reduce errors. A 60% Sn/36% Pb solder has one tenth the thermal voltage of common 64% Sn/ 36% Pb solder at a copper junction.

The number and type of dissimilar metallic junctions in the input circuit loop should be balanced. If the junctions are kept at the same temperature their summation will add to zero cancelling errors (Figure 1).

Shielding precision analog circuits from air currents — especially those caused by power dissipating components and fans — will minimize temperature gradients and minimize thermocouple induced errors.

Avoiding Latch-Up

Junction isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3 V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on causing excessive device power supply current and excessive power dissipation. TSC911 power supplies should be established either at the same time or before input signals are applied. If this is not possible input current should be limited to 1 mA to avoid triggering the p-n-p-n structure.

Static Protection

Input pins are protected against electrostatic fields. Static handling procedures should be used with all CMOS devices. Many companies provide services, educational material, and supplies to aid electronic equipment manufacturers establish "static safe" CMOS component handling areas. A partial company list is:

- 3M
  Static Control Systems Div
  223-23W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (201) 561-9520

Overload Recovery

The TSC911 recovers quickly from output saturation. Typical recovery time from positive output saturation is 20 msec. Negative output saturation recovery time is typically 5 msec.

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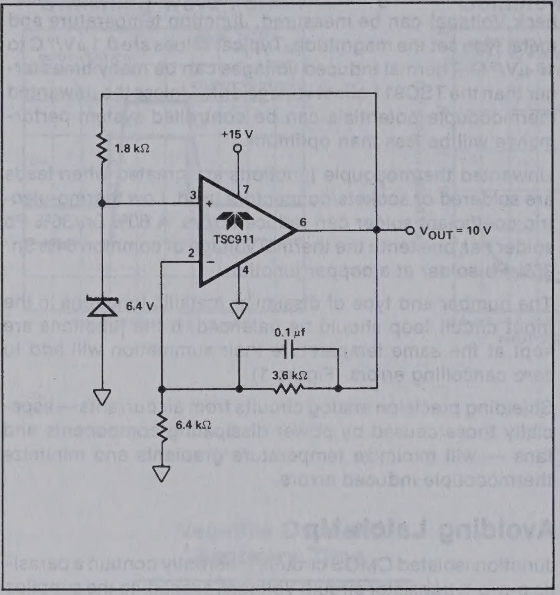
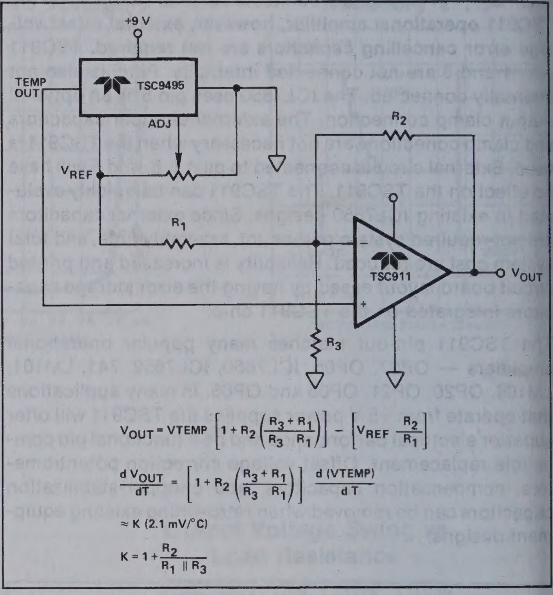
Typical Applications

10 Volt Precision Reference


+15 V
1.8 kΩ
3
7
TSC911
6
V_{OUT} = 10 V
2
4
6.4 V
0.1 µf
3.6 kΩ
6.4 kΩ

Thermometer Circuit


+9 V
TEMP OUT
TSC9495
ADJ
R_2
V_{REF}
R_1
TSC911
V_{OUT}
R_3

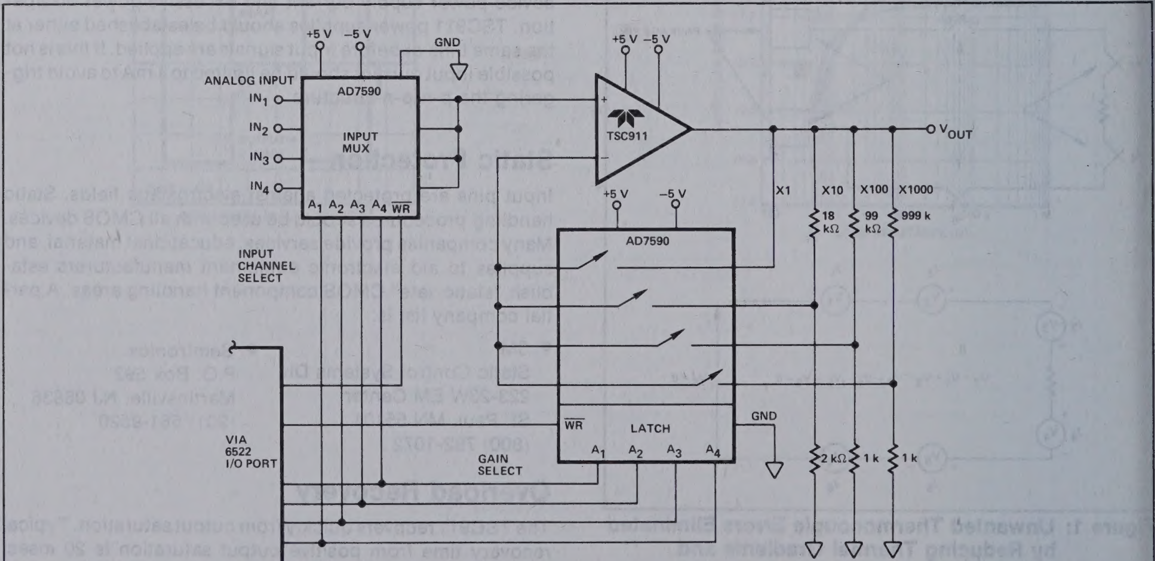
$$V_{OUT} = VTEMP\left[1 + R_2\left(\frac{R_3 + R_1}{R_3\ R_1}\right)\right] - \left[V_{REF}\ \frac{R_2}{R_1}\right]$$

$$\frac{d\,V_{OUT}}{dT} = \left[1 + R_2\left(\frac{R_3 + R_1}{R_3\ R_1}\right)\right]\ \frac{d\,(VTEMP)}{d\,T}$$

$$\approx K\ (2.1\ mV/°C)$$

$$K = 1 + \frac{R_2}{R_1 \parallel R_3}$$

Programmable Gain Amplifier with Imput Multiplexer


+5 V
–5 V
GND
ANALOG INPUT
AD7590
IN_1
IN_2
IN_3
IN_4
INPUT MUX
A_1 A_2 A_3 A_4 $\overline{WR}$
INPUT CHANNEL SELECT
VIA 6522 I/O PORT
+5 V –5 V
TSC911
V_{OUT}
X1
X10
X100
X1000
+5 V
–5 V
AD7590
18 kΩ
99 kΩ
999 k
$\overline{WR}$
LATCH
GND
A_1 A_2 A_3 A_4
GAIN SELECT
2 kΩ
1 k
1 k

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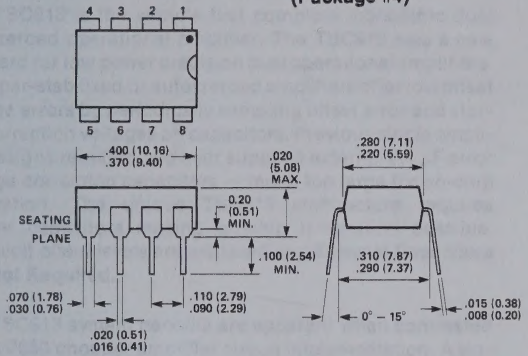
uto-Zeroed Monolithic
perational Amplifier

- No External Chopper Capacitors
- 3.5 mW Power Dissipation
- 5 μV Offset Voltage

TSC911

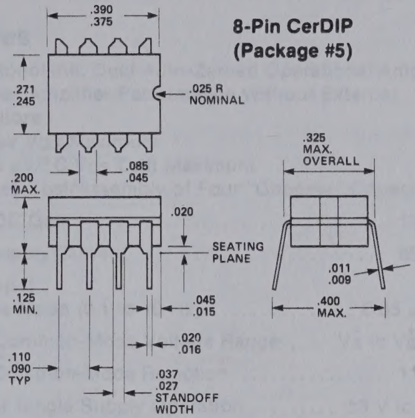
ackage Outline

8-Pin Plastic Dip (Package #4)



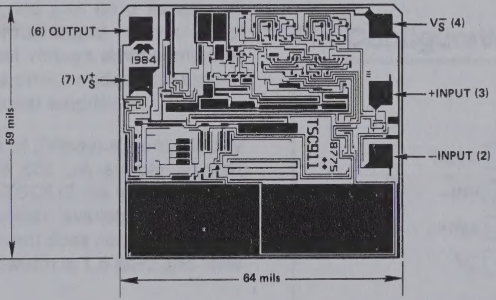
4 3 2 1
5 6 7 8
.400 (10.16)
.370 (9.40)
.020 (5.08) MAX.
.280 (7.11)
.220 (5.59)
0.20 (0.51) MIN.
SEATING PLANE
.100 (2.54) MIN.
.310 (7.87)
.290 (7.37)
.070 (1.78)
.030 (0.76)
.110 (2.79)
.090 (2.29)
.015 (0.38)
.008 (0.20)
0° – 15°
.020 (0.51)
.016 (0.41)

8-Pin CerDIP (Package #5)



.390
.375
.271
.245
.025 R NOMINAL
.325 MAX. OVERALL
.200 MAX.
.085
.045
.020
SEATING PLANE
.011
.009
.125 MIN.
.045
.015
.400 MAX.
.020
.016
.110
.090 TYP
.037
.027
STANDOFF WIDTH

Chip Pad Layout



(6) OUTPUT
(7) V_S^+
V_S^- (4)
+INPUT (3)
−INPUT (2)
59 mils
64 mils
1984
TSC911

13

Notes

TELEDYNE SEMICONDUCTOR

TSC913

Dual Auto-Zeroed Operational Amplifier

• 15 μV Offset Voltage
• 650 μA Supply Current
• No External Capacitors Required

Advance Product Information

eneral Description

he TSC913 is the world's first complete monolithic dual uto-zeroed operational amplifier. The TSC913 sets a new tandard for low power precision dual operational amplifiers. hopper-stabilized or auto-zeroed amplifiers offer low offset oltage errors by periodically sampling offset error and stor-ng correction voltages on capacitors. Previous single ampli-er designs required two user supplied external 0.1 μF error torage correction capacitors — much too large for on-chip ntegration. The unique TSC913 architecture requires maller capacitors making on-chip integration possible. icrovolt offset levels are achieved and **External Capacitors re Not Required.**

he TSC913 system benefits are apparent when contrasted ith a 7650 chopper amplifier circuit implementation. A sin-le TSC913 replaces two 7650s and four capacitors. Five omponents and assembly steps are eliminated.

The TSC913 pinout matches many popular dual operational mplifiers. The OP04, TLC322, LM358, and ICL7621 are typi-cal examples. In many applications operating from dual five volt power supplies or single supplies, the TSC913 offers superior electrical performance and can be a functional, drop-in replacement. Printed circuit board rework is not necessary. The TSC913 low offset voltage error eliminates offset voltage trim potentiometers often needed with bipolar and low accuracy CMOS operational amplifiers.

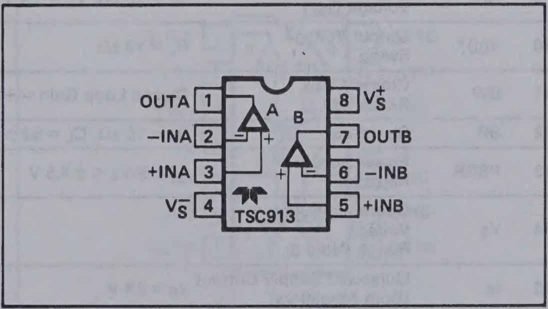
The TSC913 takes full advantage of Teledyne's proprietary CMOS technology. The TSC913 650 μA supply current 250 μA per amplifier) makes the TSC913 the lowest power, recision dual operational amplifier available. The 250 icroampere amplifier supply current does not compromise AC performance. Unity gain bandwidth is 1.5 MHz and slew rate is 2.5 V/μs.

For single and quad operational amplifiers see the TSC911 and TSC914 data sheets.

Features

- First Monolithic Dual Auto-Zeroed Operational Amplifier
- Chopper Amplifier Performance Without External Capacitors
  - — 15 μV V_{OS} Maximum
  - — 0.15 μV/°C V_{OS} Drift Maximum
  - — Saves Cost/Assembly of Four "Chopper" Capacitors
- High DC Gain .... 120 dB
- Low Supply Current .... 650 μA
- Low Input Voltage Noise (0.1 to 10 Hz) .... 0.65 μV_{P-P}
- Wide Common-Mode Voltage Range .... V_S^- to V_S^+ -2 V
- High Common-Mode Rejection .... 116 dB
- Dual or Single Supply Operation .... ±3 V to ±8 V
+4.5 V to +16 V
- Excellent AC Operating Characteristics
  - — 2.5 V/μs Slew Rate
  - — 1.5 MHz Unity Gain Bandwidth
- Pin Compatible to LM358, OP14, MC1458, ICL7621, TL082, TLC322

Pin Configuration



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TSC913

Dual Auto-Zeroed Operational Amplifier

- 15 μV Offset Voltage
- 650 μA Supply Current
- No External Capacitors Required

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-)	18 Volts
Input Voltage	(V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range	-55 °C to 150 °C
Lead Temperature (Soldering, 10 sec)	300 °C
Current into Any Pin	10 mA
Operating Temp. Range	
I Device	-25 °C to +85 °C
C Device	0 °C to +70 °C
Package Power Dissipation (T_A = 25 °C)	
CerDIP Package	500 mW
Plastic Package	375 mW

Electrical Characteristics: $V_S = \pm5$, $T_A = 25°C$ unless otherwise indicated.

				TSC913A			TSC913B			
NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
1	V_{OS}	Input Offset Voltage	$T_A = 25°C$	—	5	15	—	15	30	μV
2	V_{OS}/T	Average Temperature Coefficient of Input Offset Voltage	$0°C \leq T_A \leq 70°C$ $-25°C \leq T_A \leq 85°C$	— —	0.05 0.05	0.15 0.15	— —	— —	0.25 0.25	μV/°C μV/°C
3	I_B	Average Input Bias Current	$T_A = 25°C$ $0°C \leq T_A \leq 70°C$ $-25°C \leq T_A \leq 85°C$	— — —	— — —	90 3 4	— — —	— — —	120 4 6	pA nA nA
4	I_{OS}	Average Input	Offset Current	—	5	20	—	10	40	pA
5	en	Input Voltage Noise	0.1 to 1.0 Hz, $R_S \leq 100\ \Omega$	—	0.6	—	—	0.6	—	μV_{P-P}
6	en	Input Voltage Noise	0.1 to 10 Hz, $R_S \leq 100\ \Omega$	—	11	—	—	11	—	μV_{P-P}
7	CMRR	Common-Mode Rejection Ratio	$V_S^- \leq V_{CM} \leq V_S^+ - 2.2$ V	110	116	—	100	110	—	dB
8	CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+ -2.0	V_S^-	—	V_S^+ -2.0	V
9	A_{OL}	Open-Loop Voltage Gain	$R_L = 10\ k\Omega$, $V_O = \pm4$ V	115	120	—	110	120	—	dB
10	V_{OUT}	Output Voltage Swing	$R_L = 10\ k\Omega$	V_S^- + .3 V	—	V_S^+ -.9 V	V_S^- + .3 V	—	V_S^+ -.9 V	V
11	BW	Closed Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
12	SR	Slew Rate	$R_L = 10\ k\Omega$, $C_L = 50$ pf	—	2.5	—	—	2.5	—	V/μs
13	PSRR	Power Supply Rejection	$\pm3.3 \leq V_S \leq \pm\ 5.5$ V	110	—	—	100	—	—	dB
14	V_S	Operating Supply Voltage Range (Note 3)		±3 V	—	±8 V	±3 V	—	±8 V	V
15	I_S	Quiescent Supply Current (Both Amplifiers)	$V_S = \pm5$ V	—	0.65	0.85	—	—	1.1	mA

Notes:

1. Static Sensitive Device. Unused devices should be stored in conductive material.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.
3. Single Supply Operation: V_S^+ = +4.5 V to +16 V.
4. Advance product information.

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TELEDYNE
SEMICONDUCTOR

TSC914

Quad Auto-Zeroed Operational Amplifier

- 15 μV Offset Voltage
- 1.5 mA Supply Current
- No External Capacitors Required

Advance
Product
Information

General Description

The TSC914 is the world's first complete monolithic quad auto-zeroed operational amplifier. The TSC914 sets a new standard for low power precision quad operational amplifiers. Chopper-stabilized or auto-zeroed amplifiers offer low offset voltage errors by periodically sampling offset error and storing correction voltages on capacitors. Previous single amplifier designs required two user supplied external 0.1 μF error storage correction capacitors — much too large for on-chip integration. The unique TSC914 architecture requires smaller capacitors making on-chip integration possible. Microvolt offset levels are achieved and **External Capacitors Are Not Required.**

The TSC914 system benefits are apparent when contrasted with a 7650 chopper amplifier circuit implementation. A single TSC914 replaces four 7650s and eight capacitors. Eleven components and assembly steps are eliminated.

The TSC914 pinout matches many popular quad operational amplifiers. The OP11, TLC274, LTC1014, LM348, and ICL7642/41 are typical examples. In many applications operating from dual five volt power supplies or single supplies, the TSC914 offers superior electrical performance and can be a functional, drop-in replacement. Printed circuit board rework is not necessary. The TSC914 low offset voltage error eliminates offset voltage trim potentiometers often needed with bipolar and low accuracy CMOS operational amplifiers.

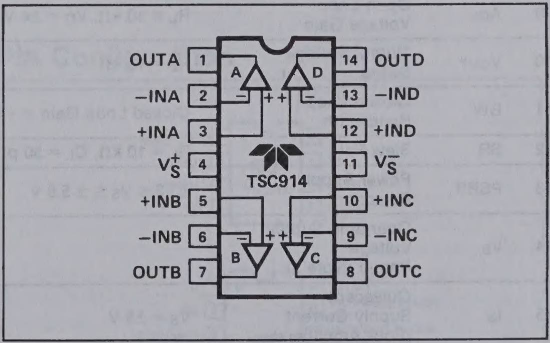
The TSC914 takes full advantage of Teledyne's proprietary CMOS technology. The TSC914 1.5 mA supply current (250 μA per amplifier) makes the TSC914 the lowest power, precision quad operational amplifier available. The 250 microampere amplifier supply current does not compromise AC performance. Unity gain bandwidth is 1.5 MHz and slew rate is 2.5 V/μs.

For single and dual operational amplifiers see the TSC911 and TSC913 data sheets.

Features

- First Monolithic Quad Auto-Zeroed Operational Amplifier
- Chopper Amplifier Performance Without External Capacitors
  - — 15 μV Vos
  - — 0.15 μV/°C Vos Drift
  - — Saves Cost/Assembly of Eight "Chopper" Capacitors
- High DC Gain .... 110 dB
- Low Supply Current .... 1.5 mA
- Wide Common-Mode Voltage Range .... V_S^- to V_S^+ -2 V
- High Common-Mode Rejection .... 110 dB
- Dual or Single Supply Operation .... ±3 V to ±8 V
+4.5 V to +16 V
- Excellent AC Operating Characteristics
  - — 2.5 V/μs Slew Rate
  - — 1.5 MHz Unity Gain Bandwidth
- Pin Compatible to LM348, TLC274, LM324, OP11, ICL7641/42

Pin Configuration



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TSC914

Quad Auto-Zeroed Operational Amplifier

• 15 μV Offset Voltage
• 1.5 mA Supply Current
• No External Capacitors Required

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-)	18 Volts
Input Voltage	(V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range	-55 °C to 150 °C
Lead Temperature (Soldering, 10 sec)	300 °C
Current into Any Pin	10 mA
Operating Temp. Range	
I Device	-25 °C to +85 °C
C Device	0 °C to +70 °C
Package Power Dissipation (T_A = 25 °C)	
CerDIP Package	500 mW
Plastic Package	375 mW

Electrical Characteristics: V_S = ±5, T_A = 25°C unless otherwise indicated.

				TSC914A			TSC914B			
NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
1	V_{OS}	Input Offset Voltage	T_A = 25°C	—	5	15	—	15	30	μV
2	V_{OS}/T	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— —	0.05 0.05	0.15 0.15	— —	— —	0.25 0.25	μV/°C μV/°C
3	I_B	Average Input Bias Current	T_A = 25°C 0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— — —	— — —	90 3 4	— — —	— — —	120 4 6	pA nA nA
4	I_{OS}	Average Input	Offset Current	—	5	20	—	10	40	pA
5	e_n	Input Voltage Noise	0.1 to 1.0 Hz, R_S ≤ 100 Ω	—	0.6	—	—	0.6	—	μV_{P-P}
6	e_n	Input Voltage Noise	0.1 to 10 Hz, R_S ≤ 100 Ω	—	11	—	—	11	—	μV_{P-P}
7	CMRR	Common-Mode Rejection Ratio	V_S^- ≤ V_{CM} ≤ V_S^+ - 2.2 V	110	116	—	100	110	—	dB
8	CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+ -2.0	V_S^-	—	V_S^+ -2.0	V
9	A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_O = ±4 V	115	120	—	110	120	—	dB
10	V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^- + .3 V	—	V_S^+ -.9 V	V_S^- + .3 V	—	V_S^+ -.9 V	V
11	BW	Closed Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
12	SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pf	—	2.5	—	—	2.5	—	V/μs
13	PSRR	Power Supply Rejection	±3.3 ≤ V_S ≤ ± 5.5 V	110	—	—	100	—	—	dB
14	V_S	Operating Supply Voltage Range (Note 3)		±3 V	—	±8 V	±3 V	—	±8 V	V
15	I_S	Quiescent Supply Current (Four Amplifiers)	V_S = ±5 V	—	—	1.6	—	—	2.2	mA

Notes:

1. Static Sensitive Device. Unused devices should be stored in conductive material.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.
3. Single Supply Operation: V_S^+ = +4.5 V to +16 V.
4. Advance product information.

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TELEDYNE SEMICONDUCTOR

TSC918
Low Cost Operational Amplifier
• 50 μV Max. V_{OS}
• 800 μA Max. Supply Current

General Description

The TSC918 is a general purpose, low cost CMOS operaional amplifier. By sampling input offset voltage periodically and storing compensating voltages on external capacitors ow offset voltage errors are possible. The correction circuits compensate offset voltage drift with temperature and time. Offset voltage temperature coefficient is 0.8μV/°C maximum. Maximum V_{OS} is 50 μV.

The TSC918 performance advantages are achieved without he manufacturing complexity and cost incurred with laser or "zener zap" V_{OS} trim techniques. The TSC918 offers a 0.2 V/μs slew rate and a 700 kHz unity gain bandwidth. Open loop voltage gain is 100 dB.

Operating from ±5 V supplies the CMOS TSC918 power dissipation is under 10 mW. In +5 V only systems the TSC7660 DC-to-DC converter can supply the TSC918 negative supply potential. The TSC918 will also operate from a single +5 supply.

For lower power dissipation and offset voltage errors, see the TSC900 and TSC7650/7650A specifications.

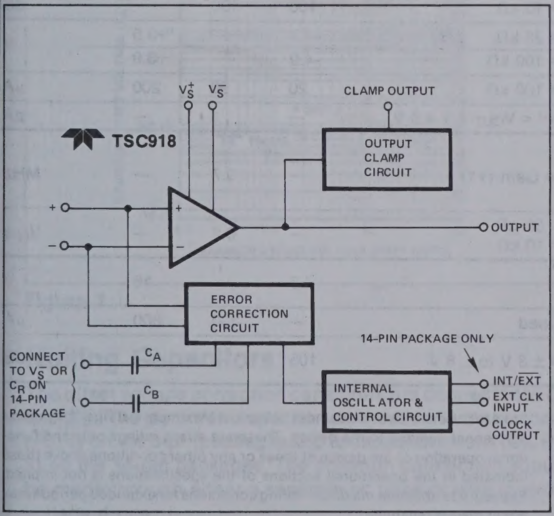
Features

- Low Power Supply Current .... 800 μA Max.
- Low Input Offset Voltage .... 50 μV Max.
- Low Input Offset Voltage Drift .... 0.8 μV/°C Max.
- High Impedance Differential CMOS Inputs ..... 10^{12} Ω
- High Open Loop Voltage Gain .... 100 dB Min.
- Low Input Noise Voltage .... 0.3 μVp-p
- Compensated Internally for Stable Unity Gain Operation
- High Common Mode Rejection .... 98 dB Min.

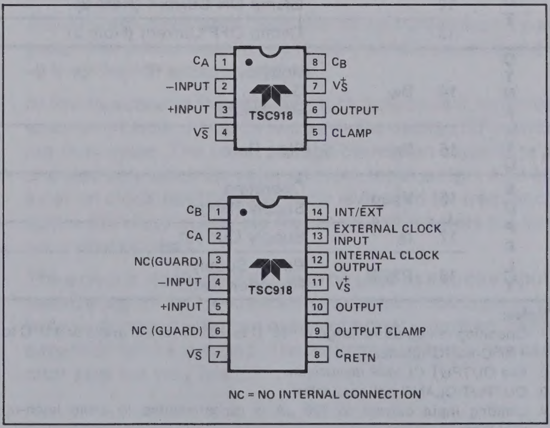
Ordering Information

Part No.	Package	Temp. Range	Max. V_{OS}
TSC918CPA	8-Pin Plastic Dip	COM	50 μV
TSC918IJA	8-Pin CerDIP	IND	50 μV
TSC918CPD	14-Pin Plastic Dip	COM	50 μV
TSC918IJD	14-Pin CerDIP	IND	50 μV

Functional Diagram


TSC918
V+S
V−S
CLAMP OUTPUT
OUTPUT CLAMP CIRCUIT
+
−
+
−
OUTPUT
ERROR CORRECTION CIRCUIT
14-PIN PACKAGE ONLY
CONNECT TO V−S OR CR ON 14-PIN PACKAGE
CA
CB
INTERNAL OSCILLATOR & CONTROL CIRCUIT
INT/EXT
EXT CLK INPUT
CLOCK OUTPUT

Pin Configuration


CA 1
−INPUT 2
+INPUT 3
V−S 4
8 CB
7 V+S
6 OUTPUT
5 CLAMP
TSC918
CB 1
CA 2
NC(GUARD) 3
−INPUT 4
+INPUT 5
NC (GUARD) 6
V−S 7
14 INT/EXT
13 EXTERNAL CLOCK INPUT
12 INTERNAL CLOCK OUTPUT
11 V+S
10 OUTPUT
9 OUTPUT CLAMP
8 CRETN
TSC918
NC = NO INTERNAL CONNECTION

13

Low Cost Operational Amplifier

- **50 µV Max. V_{OS}**
- **800 µA Max. Supply Current**

TSC918

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-)	18 Volts
Input Voltage	(V_S^+ + 0.3) to (V_S^- – 0.3) Volts
Storage Temp. Range	-55° C to 150° C
Lead Temperature (Soldering, 10 sec)	300° C
Voltage on Oscillator Control Pins	V_S^+ to V_S^-
Output Short Circuit Duration	Indefinite
Current into Any Pin	10 mA
While Operating (Note 4)	100 µA
Operating Temp. Range	
I Device	-25° C to +85° C
C Device	0° C to +70° C
Package Power Dissipation (T_A = 25° C)	
CerDIP Package	500 mW
Plastic Package	500 mW

Electrical Characteristics: V_S^+ = +5 V, V_S^- = -5 V, C_A = C_B = 0.1 µF. T_A = 25° C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC918 MIN	TSC918 TYP	TSC918 MAX	UNIT
INPUT	1	V_{OS}	Input Offset Voltage	T_A = +25° C	—	—	50	µV
	2	$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Average Temp. Coefficient	Operating Temp Range (Note 1)	—	0.4	0.8	µV/° C
	3	I_{BIAS}	Average Input Bias Current (Note 7)	T_A = + 25° C	—	—	100	pA
	4	I_{OS}	Input Offset Current	T_A = + 25° C	—	0.5	—	pA
	5	$e_{np\text{-}p}$	Input Noise Voltage	R_S = 100 Ω 0 to 10 Hz	—	4	—	$\mu V_{p\text{-}p}$
	6	$e_{np\text{-}p}$	Input Noise Voltage	R_S = 100 Ω 0 to 1 Hz	—	0.3	—	$\mu V_{p\text{-}p}$
	7	R_{IN}	Input Resistance		—	10^{12}	—	Ω
	8	CMVR	Common-Mode Voltage Range		-5.0		+2.0 V	V
	9	CMRR	Common-Mode Rejection Ratio	CMVR = -5 V to +2.0 V	98	115	—	dB
OUTPUT	10	A_V	Large-Signal Voltage Gain	R_L = 10 kΩ	100	130	—	dB
	11	V_{OUT}	Output Voltage Swing (Note 3)	R_L = 25 kΩ	-4.7	—	+3.5	V
				R_L = 100 kΩ	-4.9	—	+3.9	
	12		Clamp ON Current (Note 2)	R_L = 100 kΩ	20	90	200	µA
	13		Clamp OFF Current (Note 2)	-4.0 V < V_{OUT} < + 4.0 V	—	1	—	pA
DYNAMIC	14	B_W	Unity Gain Bandwidth	Unity Gain (+1)	—	0.7	—	MHz
	15	S_R	Slew Rate	C_L = 50 pF, R_L = 10 kΩ	—	0.2	—	V/µs
SUPPLY	16	V_S^+ to V_S^-	Operating Supply Range		4.5	—	16	V
	17	I_S	Supply Current	No Load	—	300	800	µA
	18	PSRR	Power Supply Rejection Ratio	V_S = ± 3 V to ± 8 V	105	—	—	dB

Notes:

1. Operating temperature range is -25° C to +85° C for "I" grade and 0° C to +70° C for "C" grade.
2. See OUTPUT CLAMP discussion.
3. OUTPUT CLAMP not connected.
4. Limiting input current to 100 µA is recommended to avoid latch-up problems.
5. Static Sensitive Device. Unused devices must be stored in conductive material to protect devices from possible static damage.
6. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
7. Average current caused by switch charge transfer at input.

OP Amp Performance Comparison

The TSC918 is a low cost, low power, precision amplifier. A comparison between the TSC918 and other amplifiers is shown in Figure 1 below.

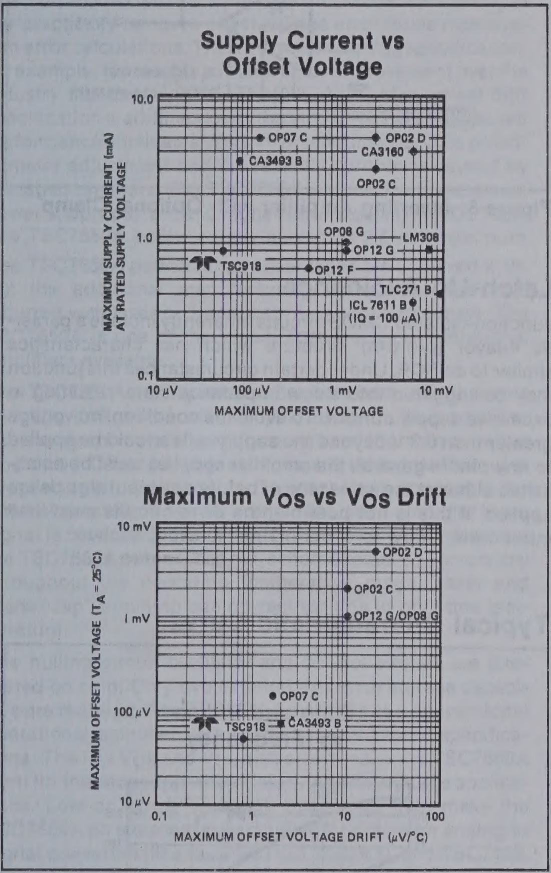


Figure 1

Nulling Capacitors

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (Pin 4) on the 8-pin packages and to capacitor return (C_R, Pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops.

Internally V_S^- is connected to C_R.

C_A and C_B should be 0.1 µF film capacitors. Mylar capacitors are suitable.

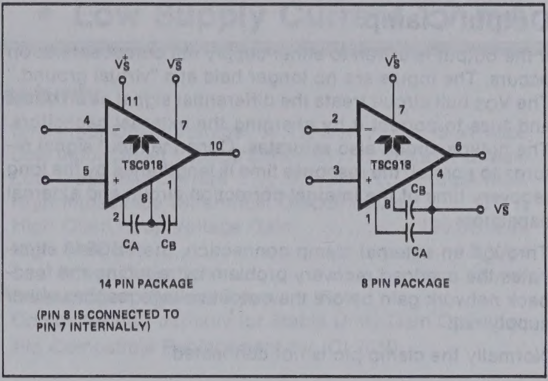


Figure 2: Nulling Capacitor Connection

Clock Operation

The internal oscillator is set for a 150 Hz nominal frequency on both the 8 and 14-pin dual in line packages. With the 14-pin DIP TSC918, the 150 Hz internal frequency is available at the internal clock output (Pin 12). A 300 Hz nominal signal will be present at the external clock input pin (Pin 13) with $\overline{\text{EXT}}$/INT high or open. This is the internal clock signal before a divide by two operation.

The 14-pin DIP device can be driven by an external clock. The INT/$\overline{\text{EXT}}$ input (Pin 14) has an internal pull-up and maybe left open for internal clock operation. If an external clock is used INT/$\overline{\text{EXT}}$ must be tied to V_S^- (Pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (Pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6 V and between V_S^+ and V_S^+ -6 V for higher supply voltages.

At low frequencies the external clock duty cycle is not critical since an internal divide by two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50-80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitor pins are very low.

Output Clamp

If the output is driven to either supply rail output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the internal correction circuit and external capacitors.

Through an external clamp connection, the TSC918 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

Normally the clamp pin is not connected.

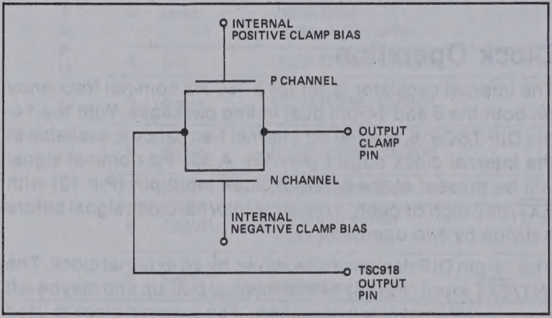

INTERNAL
POSITIVE CLAMP BIAS
P CHANNEL
OUTPUT
CLAMP
PIN
N CHANNEL
INTERNAL
NEGATIVE CLAMP BIAS
TSC918
OUTPUT
PIN

Figure 3: Internal Clamp Circuit

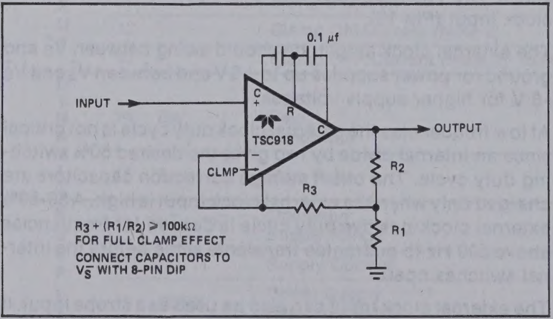

0.1 μf
INPUT
C
+
R
TSC918
C
−
CLMP
OUTPUT
R2
R3
R1
R3 + (R1/R2) ⩾ 100kΩ
FOR FULL CLAMP EFFECT
CONNECT CAPACITORS TO
V$_S^-$ WITH 8-PIN DIP

Figure 4: Non-Inverting Amplifier with Optional Clamp

Input Bias Current

The TSC918 inputs are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. The sampling causes, however, charge transfer at the inputs. The charge transfer represents a peak impulse current of 200 to 290 nA at the inputs when the internal clock makes a transition.

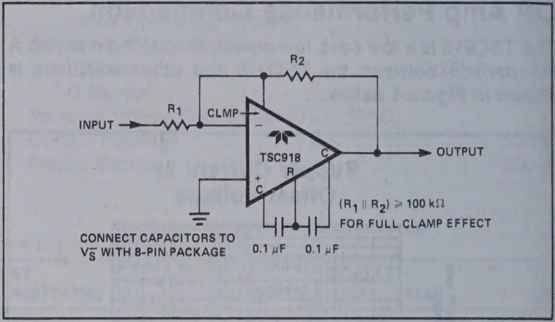
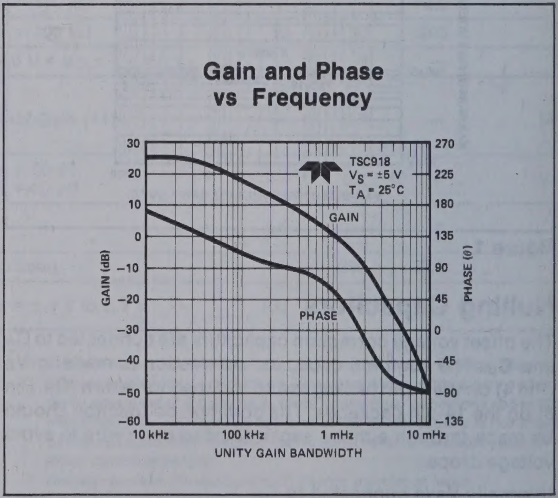

R2
R1
CLMP
INPUT
−
TSC918
R
C
+
C
OUTPUT
(R1 ∥ R2) ⩾ 100 kΩ
FOR FULL CLAMP EFFECT
CONNECT CAPACITORS TO
V$_S^-$ WITH 8-PIN PACKAGE
0.1 μF
0.1 μF

Figure 5: Inverting Amplifier with Optional Clamp

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low impedance state, resulting in excessive supply current. To avoid the condition, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latchup.

Typical Characteristic Curve


Gain and Phase vs Frequency

TELEDYNE SEMICONDUCTOR

TSC7650A
Chopper-Stabilized Operational Amplifier

- **Low Offset Voltage 5 μV Max.**
- **Low Supply Current 1.7 mA**

General Description

The TSC7650A CMOS chopper-stabilized operational ampliier practically removes offset voltage error terms from sysem error calculations. The 5 μV maximum V_{OS} specification, or example, represents a fifteen times improvement over the ndustry standard OP07E. The 0.2 μV/°C Max. offset drift specification is six times lower than the OP07E. The increased performance eliminates V_{OS} trim procedures, periodic potentiometer adjustment and the reliability problems caused by damaged trimmers. The TSC7650A features lower maximum power supply current and higher slew rate than the ICL 7650. The TSC7650A power supply current is 2.5 mA maximum.

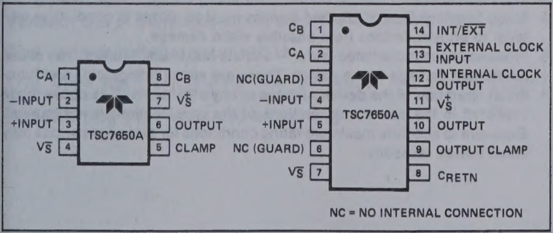
The TSC7650A performance advantages are achieved without the additional manufacturing complexity and cost incurred with laser or "zener zap" V_{OS} trim techniques. The TSC7650A is one of the lowest cost precision operational amplifiers available.

The TSC7650A nulling scheme corrects both dc V_{OS} errors and V_{OS} drift errors with temperature. A nulling amplifier alternately corrects its own V_{OS} errors and the main amplifier V_{OS} error. Offset nulling voltages are stored on two user supplied external capacitors. The capacitors connect to the internal amplifier V_{OS} null points. The main amplifier input signal is never switched. Switching spikes are not present at the TSC7650A output. The null scheme keeps V_{OS} errors low throughout the operating temperature range. Laser and "zener zap" trimming can correct for V_{OS} at only one temperature.

The nulling circuit oscillator and control circuits are integrated on chip. Only two external V_{OS} error storage capacitors are required. The TSC7650A operates as a conventional operational amplifier with vastly improved input specifications. The low V_{OS} and V_{OS} drift errors make the TSC7650A ideal for thermocouple, thermistor, and strain gauge applications. Low dc errors and high open loop gain make the TSC7650A an excellent preamplifier for precision analog to digital converters like the TSC7135, TSC800, and TSC7109.

The 14-pin dual in line package (DIP) has an external oscillator input to drive the nulling circuitry for optimum noise performance. Both the 8 and 14-pin DIP have an output voltage clamp circuit to minimize overload recovery time.

Pin Configuration


CA 1
−INPUT 2
+INPUT 3
V$_S^-$ 4
8 CB
7 V$_S^+$
6 OUTPUT
5 CLAMP
TSC7650A
CB 1
CA 2
NC(GUARD) 3
−INPUT 4
+INPUT 5
NC (GUARD) 6
V$_S^-$ 7
14 INT/$\overline{EXT}$
13 EXTERNAL CLOCK INPUT
12 INTERNAL CLOCK OUTPUT
11 V$_S^+$
10 OUTPUT
9 OUTPUT CLAMP
8 CRETN
TSC7650A

NC = NO INTERNAL CONNECTION

Features

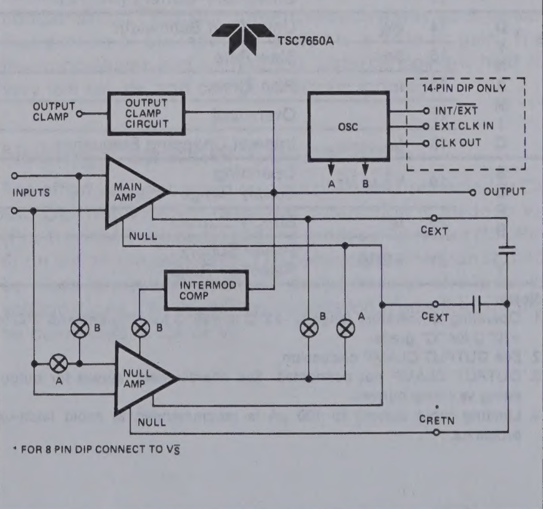
- Low Input Offset Voltage .... 5 μV Max.
- Low Input Offset Voltage Drift .... 0.2 μV/°C Max.
- Low Input Bias Current .... 15 pA Max.
- High Impedance Differential CMOS Inputs ..... 10^{12} Ω
- High Open Loop Voltage Gain .... 120 dB Min.
- High Slew Rate .... 4.0 V/μs
- Low Power Operation .... 17 mW
- Output Clamp Speeds Recovery Time
- Compensated Internally for Stable Unity Gain Operation
- Pin Compatible Replacement for ICL7650

Ordering Information

Part No.	Package	Temp. Range	Max. V_{OS}
*TSC7650ACPA	8-Pin Plastic Dip	0°C to + 70°C	5 μV
*TSC7650AIJA	8-Pin CerDIP	-25°C to + 85°C	5 μV
*TSC7650ACPD	14-Pin Plastic Dip	0°C to + 70°C	5 μV
*TSC7650AIJD	14-Pin CerDIP	-25°C to + 85°C	5 μV

*Available with 160 hour, +125°C burn-in. Add /BI to part number suffix.

Functional Diagram


TSC7650A
OUTPUT CLAMP
OUTPUT CLAMP CIRCUIT
OSC
14-PIN DIP ONLY
INT/$\overline{EXT}$
EXT CLK IN
CLK OUT
A
B
INPUTS
MAIN AMP
OUTPUT
NULL
CEXT
INTERMOD COMP
CEXT
B
B
B
A
A
NULL AMP
NULL
CRETN

* FOR 8 PIN DIP CONNECT TO V$_S^-$

Chopper-Stabilized Operational Amplifier

- **Low Offset Voltage 5 µV Max.**
- **Low Supply Current 1.7 mA**

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-)	18 Volts
Input Voltage	(V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range	-55° C to 150° C
Lead Temperature (Soldering, 10 sec)	300° C
Voltage on Oscillator Control Pins	V_S^+ to V_S^-
Output Short Circuit Duration	Indefinite
Current Into Any Pin	10 mA
While Operating (Note 4)	100 µA
Operating Temp. Range	
I Device	-25° C to +85° C
C Device	0° C to +70° C
Package Power Dissipation (T_A = 25° C)	
CerDIP Package	500 mV
Plastic Package	375 mW

Electrical Characteristics: V_S^+ = +5 V, V_S^- = -5 V, C_A = C_B = 0.1 µF. T_A = 25° C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7650A MIN	TSC7650A TYP	TSC7650A MAX	UNIT
INPUT	1	V_{OS}	Input Offset Voltage	T_A = +25° C	—	± 0.7	± 5.0	µV
	2	$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Average Temp. Coefficient	Operating Temp Range (Note 1)	—	0.08	0.2	µV/° C
	3	I_{BIAS}	Input Bias Current	T_A = + 25° C	—	1.5	15	pA
				0° C ≤ T_A ≤ + 70° C	—	35	150	
				-25° C ≤ T_A ≤ + 85° C	—	100	400	
	4	I_{OS}	Input Offset Current	T_A = 25° C	—	0.5	—	pA
	5	e_{np-p}	Input Noise Voltage	R_S = 100 Ω 0.1 to 10 Hz	—	4.0	—	μV_{p-p}
	6	i_n	Input Noise Current	f = 10 Hz	—	0.01		pA/√Hz
	7	R_{IN}	Input Resistance		—	10^{12}		Ω
	8	CMVR	Common-Mode Voltage Range		-5.0	-5.2 to +2.0	+1.5 V	V
	9	CMRR	Common-Mode Rejection Ratio	CMVR = -5 V to +1. 5 V	120	130	—	dB
OUTPUT	10	A_V	Large-Signal Voltage Gain	R_L = 10 kΩ	120	130	—	dB
	11	V_{OUT}	Output Voltage Swing (Note 3)	R_L = 10 kΩ	± 4.7	± 4.85	—	V
				R_L = 100 kΩ	—	± 4.95	—	
	12		Clamp ON Current (Note 2)	R_L = 100 kΩ	25	70	200	µA
	13		Clamp OFF Current (Note 2)	-4.0 V < V_{OUT} < + 4.0 V	—	1	—	pA
DYNAMIC	14	B_W	Unity Gain Bandwidth	Unity Gain (+1)	—	1.0	—	MHz
	15	S_R	Slew Rate	C_L = 50 pF, R_L = 10 kΩ	—	4.0	—	V/µs
	16	t_r	Rise Time		—	0.2	—	µs
	17		Overshoot		—	30	—	%
	18	f_{ch}	Internal Chopping Frequency	Pins 12-14 Open (DIP)	120	300	420	Hz
SUPPLY	19	V_S^+ to V_S^-	Operating Supply Range		4.5	—	16	V
	20	I_S	Supply Current	No Load	—	1.7	2.5	mA
	21	PSRR	Power Supply Rejection Ratio	V_S = ± 3 V to ± 8 V	120	130	—	dB

Notes:

1. Operating temperature range is -25° C to +85° C for "I" grade and 0° C to +70° C for "C" grade.
2. See OUTPUT CLAMP discussion.
3. OUTPUT CLAMP not connected. See characteristic curves for output swing vs clamp current.
4. Limiting input current to 100 µA is recommended to avoid latch-up problems.
5. Static Sensitive Device. Unused devices must be stored in conductive material to protect devices from possible static damage.
6. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Chopper-Stabilized Operational Amplifier

- **Low Offset Voltage 5 μV Max.**
- **Low Supply Current 1.7 mA**

TSC7650A

Theory of Operation

Figure 1 shows the major elements of the TSC7650A. There are two amplifiers, the main amplifier and the nulling amplifier; both have offset-null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. Two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

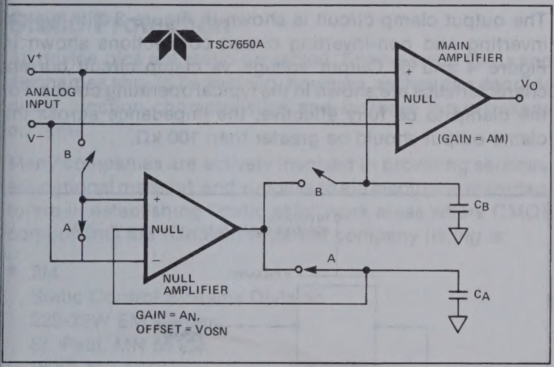


Figure 1: TSC7650A Contains a Nulling and Main Amplifier. Offset Correction Voltages are Stored on Two External Capacitors.

Careful balancing of the input switches minimizes chopper frequency charge injection at the input terminals, and the feed forward-type injection into the compensation capacitor that can cause output spikes in this type of circuit.

The circuits offset voltage compensation is easily shown. With the nulling inputs shorted a voltage almost identical to the nulling amplifier offset voltage is stored on C_A. The effective offset voltage at the null amplifier input is:

$$(1)\quad V_{OSE} = \frac{1}{A_N + 1} V_{OSN}$$

After the nulling amplifier is zeroed the main amplifier is zeroed; the A switches open and B switches close.

The output voltage equation is:

$$(2)\quad V_O = A_M\left[V_{OSM} + (V^+ - V^-) + A_N(V^+ - V^-) + A_N V_{OSE}\right]$$

Substituting (1) → (2) and assuming $A_N >> 1$.

$$(3)\quad V_O = A_M A_N\left[(V^+ - V^-) + \frac{V_{OSM} + V_{OSN}}{A_N}\right]$$

As desired the device offset voltages are reduced by the high open-loop gain of the nulling amplifier.

Output Stage/Load Driving

The output circuit is a high-impedance stage (approximately 18 kΩ). With loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the amplifier is used strictly for dc the lower gain is of little consequence since the dc gain is typically greater than 120 dB even with a 1 kΩ load. In wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or higher. This will result in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier. The clock frequency sets the transition region.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite ac gain of the amplifier results in a small ac signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the TSC7650A by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to a finite ac gain. The intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Nulling Capacitor Connection

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to $V_{\overline{S}}$ (Pin 4) on the 8-pin packages and to capacitor return (C_R, Pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops. The capacitors outside foil, if possible, should be connected to C_R or $V_{\overline{S}}$.

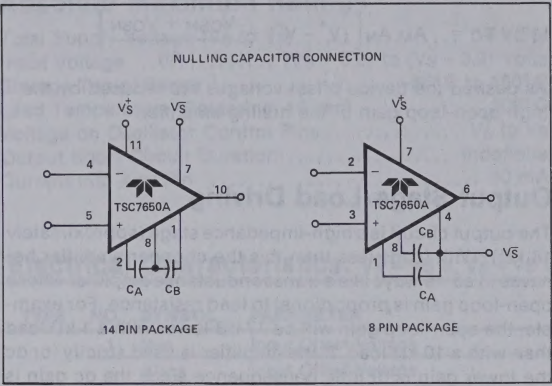

NULLING CAPACITOR CONNECTION
V_S^+
V_S^-
11
4
7
10
TSC7650A
5
1
8
2
C_A
C_B
14 PIN PACKAGE
V_S^+
2
7
6
TSC7650A
3
4
8
1
C_B
V_S^-
C_A
8 PIN PACKAGE

Figure 2: Nulling Capacitor Connection

Clock Operation

The internal oscillator is set for a 300 Hz nominal chopping frequency on both the 8 and 14-pin dual in line packages. With the 14-pin DIP TSC7650A, the 300 Hz internal chopping frequency is available at the internal clock output (Pin 12). A 600 Hz nominal signal will be present at the external clock input pin (Pin 13) with EXT/INT high or open. This is the internal clock signal before a divide by two operation.

The 14-pin DIP device can be driven by an external clock. The INT/EXT input (Pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used INT/EXT must be tied to V_S^- (Pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (Pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ± 6 V and between V^+ and V^+ -6 V for higher supply voltages.

At low frequencies the external clock duty cycle is not critical since an internal divide by two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50-80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitor pins are very low. At 25° C a typical TSC7650A will drift less than 10 µV/sec.

Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TSC7650A eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3 with typical inverting and non-inverting circuit connections shown in Figure 4 and 5. Output voltage vs clamp circuit current characteristics are shown in the typical operating curves. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 kΩ.

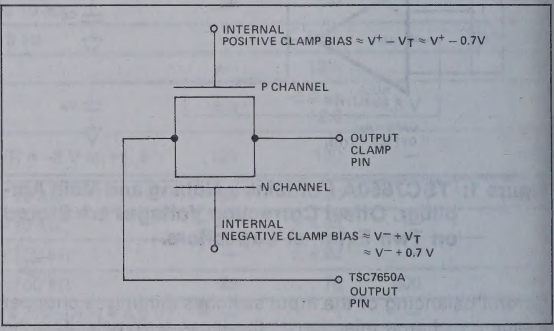

INTERNAL
POSITIVE CLAMP BIAS ≈ $V^+ - V_T \approx V^+ - 0.7V$
P CHANNEL
OUTPUT
CLAMP
PIN
N CHANNEL
INTERNAL
NEGATIVE CLAMP BIAS ≈ $V^- + V_T$
$\approx V^- + 0.7\ V$
TSC7650A
OUTPUT
PIN

Figure 3: Internal Clamp Circuit

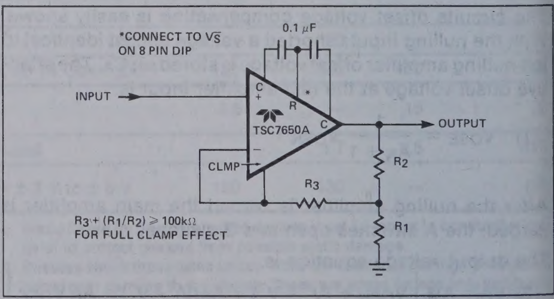

*CONNECT TO V_S^-
ON 8 PIN DIP
0.1 µF
INPUT
C
+
R
*
TSC7650A
C
OUTPUT
−
CLMP
R_2
R_3
R_1
$R_3 + (R_1/R_2) \geq 100k\Omega$
FOR FULL CLAMP EFFECT

Figure 4: Non-Inverting Amplifier with Optional Clamp

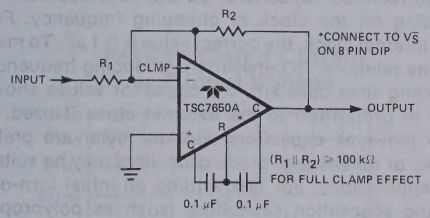


Figure 5: Inverting Amplifier with Optional Clamp

Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational material, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520
- American Convertors
  1919 South Butlerfield Road
  Mundelein, IL 60060
  (312) 362-9000
- ACL
  1960 East Devon Avenue
  Elk Grove Village, IL 60007
  (312) 981-9212

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low impedance state, resulting in excessive supply current. To avoid the condition, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latchup.

Thermo-Electric Potentials

Precision dc measurements are ultimately limited by thermoelectric potentials developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1 μV/° C, but up to tens of μV/° C for some materials, will be generated. In order to realize the benefits extremely low offset voltages provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially those caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and separation from surrounding heat-dissipating elements is advised.

Pin Compatibility

On the 8-pin mini-dip TSC7650A the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or are used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, the replacement of the offset null pot between pins 1 and 8 by two capacitors from the pins to $V_{\overline{S}}$ will convert the OP05/07 pin configuration for TSC7650A operation. For LM108 devices the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pin outs are modified similarly by also removing any circuit connections to pin 5. On the TSC7650A pin 5 is the output clamp connection. Other operational amplifiers may use this pin as an offset or compensation point.

The minor modifications needed to retrofit a TSC7650A into existing sockets operating at reduced power supply voltages make prototyping and circuit verification straight forward.

Input Guarding

High impedance, low leakage CMOS inputs allow the TSC7650A to make measurements of high impedance sources. Stray leakage paths can increase input currents and decrease input resistance unless inputs are guarded. A guard is a conductive pc trace surrounding the input terminals. The ring connects to a low impedance point as the same potential as the inputs. Stray leakages are absorbed by the low impedance ring. The equal potential between ring and inputs prevents input leakage currents. Typical guard connections are shown in Figure 6.

The 14-pin DIP configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are unused.

In applications requiring low leakage currents, boards should be cleaned thoroughly and blown dry after soldering. Protective coatings will prevent future board contamination.

Component Selection

The two required capacitors, C_A C_B, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock if used. High-quality film-type capacitors such as mylar are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 μV.

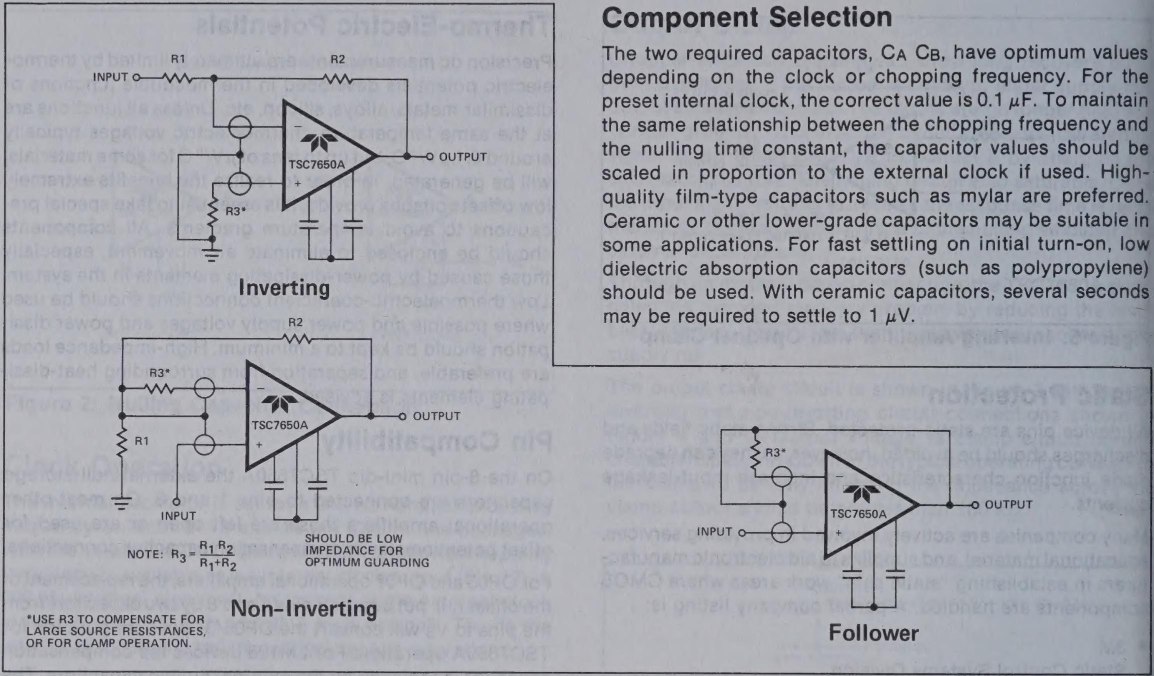
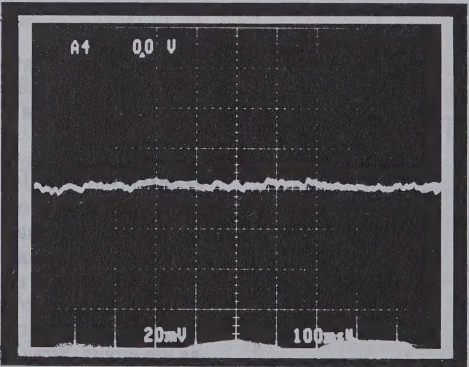

R1
R2
INPUT
TSC7650A
OUTPUT
R3*
Inverting
R2
R3*
TSC7650A
OUTPUT
R1
INPUT
NOTE: $R_3 = \frac{R_1 R_2}{R_1+R_2}$
SHOULD BE LOW IMPEDANCE FOR OPTIMUM GUARDING
Non-Inverting
*USE R3 TO COMPENSATE FOR LARGE SOURCE RESISTANCES, OR FOR CLAMP OPERATION.
R3*
INPUT
TSC7650A
OUTPUT
Follower

Figure 6: Input Guard Connection

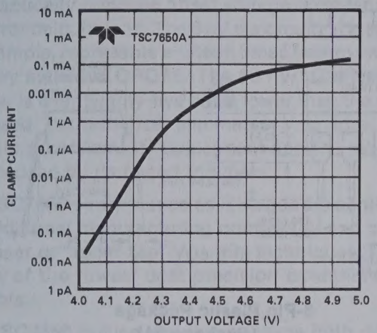


Gain = 1000, 1 Div = 20 μV_{p-p}

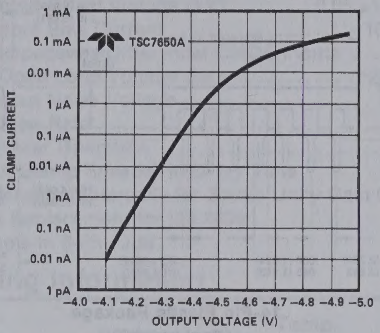
Figure 7: TSC7650A Peak to Peak Noise (0.1 to 10Hz)

Typical Characteristic Curves

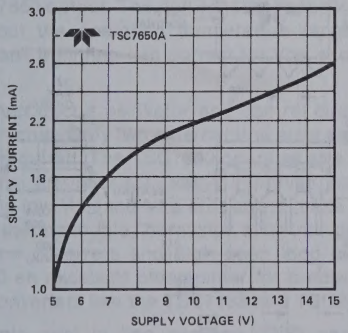
Positive Clamp Current vs Output Voltage



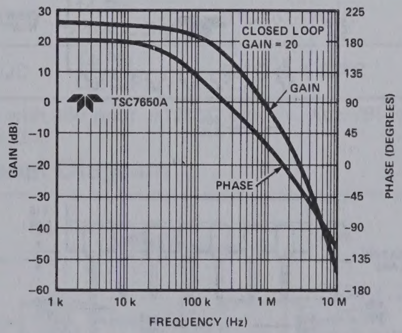
Negative Clamp Current vs Output Voltage



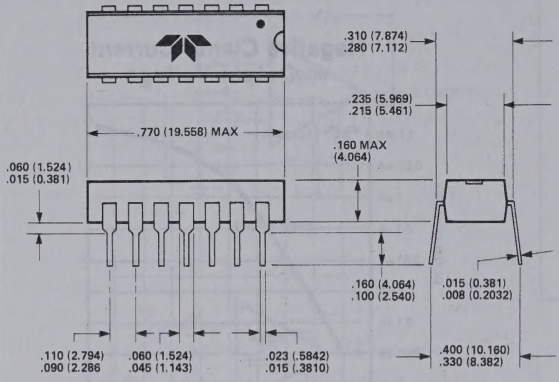
Supply Current vs Supply Voltage



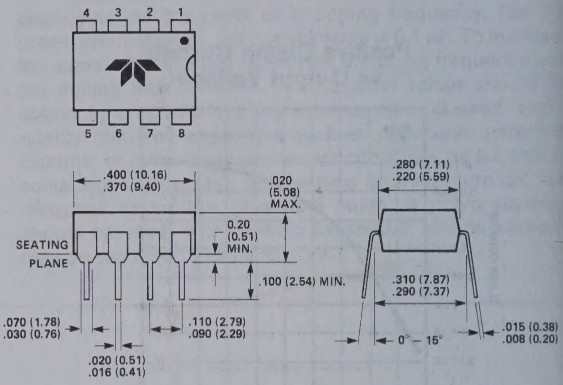
Gain/Phase vs Frequency



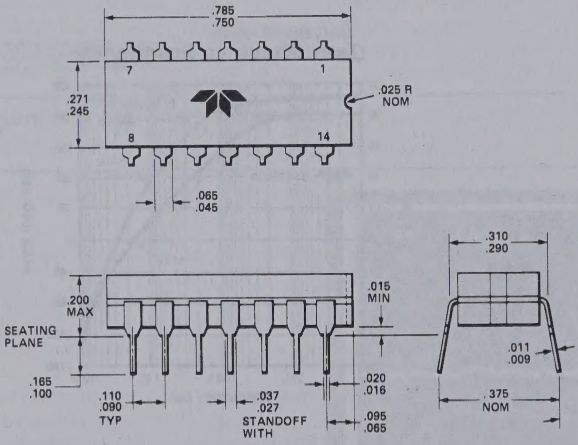
Package Outline


.310 (7.874)
.280 (7.112)
.235 (5.969)
.215 (5.461)
.770 (19.558) MAX
.160 MAX
(4.064)
.060 (1.524)
.015 (0.381)
.160 (4.064)
.100 (2.540)
.015 (0.381)
.008 (0.2032)
.110 (2.794)
.090 (2.286
.060 (1.524)
.045 (1.143)
.023 (.5842)
.015 (.3810)
.400 (10.160)
.330 (8.382)

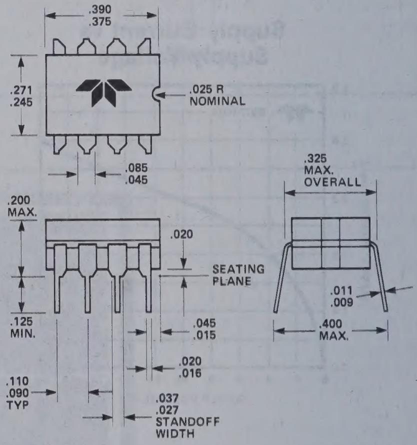
14-Pin Plastic Package
(Package #6)


4 3 2 1
5 6 7 8
.400 (10.16)
.370 (9.40)
.020
(5.08)
MAX.
.280 (7.11)
.220 (5.59)
0.20
(0.51)
MIN.
SEATING
PLANE
.100 (2.54) MIN.
.310 (7.87)
.290 (7.37)
.070 (1.78)
.030 (0.76)
.110 (2.79)
.090 (2.29)
0° – 15°
.015 (0.38)
.008 (0.20)
.020 (0.51)
.016 (0.41)

8-Pin Plastic Package
(Package #4)


.785
.750
7
1
.025 R
NOM
.271
.245
8
14
.065
.045
.310
.290
.015
MIN
.200
MAX
SEATING
PLANE
.011
.009
.165
.100
.110
.090
TYP
.037
.027
STANDOFF
WITH
.020
.016
.095
.065
.375
NOM

14-Pin CerDIP Package
(Package #7)


.390
.375
.271
.245
.025 R
NOMINAL
.085
.045
.325
MAX.
OVERALL
.200
MAX.
.020
SEATING
PLANE
.011
.009
.125
MIN.
.045
.015
.400
MAX.
.020
.016
.110
.090
TYP
.037
.027
STANDOFF
WIDTH

8-Pin CerDIP Package
(Package #5)

TELEDYNE SEMICONDUCTOR

TSC7650

Precision Chopper-Stabilized Operational Amplifier

- **0.7 μV Offset Voltage**
- **50 nV/°C Offset Voltage Drift**

General Description

The TSC7650 CMOS chopper-stabilized operational amplifier practically removes offset voltage error terms from system error calculations. The 5 μV maximum V_{OS} specification, for example, represents a fifteen times improvement over the industry standard OPO7E. The 50 nV/°C offset drift specification is over twenty-five times lower than the OPO7E. The increased performance eliminates V_{OS} trim procedures, periodic potentiometer adjustment and the reliability problems caused by damaged trimmers.

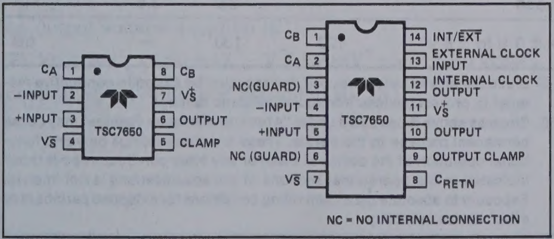
The TSC7650 performance advantages are achieved without the additional manufacturing complexity and cost incurred with laser or "zener zap" V_{OS} trim techniques. The TSC7650 is one of the lowest cost precision operational amplifiers available.

The TSC7650 nulling scheme corrects both dc V_{OS} errors and V_{OS} drift errors with temperature. A nulling amplifier alternately corrects its own V_{OS} errors and the main amplifier V_{OS} error. Offset nulling voltages are stored on two user supplied external capacitors. The capacitors connect to the internal amplifier V_{OS} null points. The main amplifier input signal is never switched. Switching spikes are not present at the TSC7650 output. The null scheme keeps V_{OS} errors low throughout the operating temperature range. Laser and "zener zap" trimming can correct for V_{OS} at only one temperature.

The nulling circuit oscillator and control circuits are integrated on chip. Only two external V_{OS} error storage capacitors are required. The TSC7650 operates as a conventional operational amplifier with vastly improved input specifications. The low V_{OS} and V_{OS} drift errors make the TSC7650 ideal for thermocouple, thermistor, and strain gauge applications. Low dc errors and high open loop gain make the TSC7650 an excellent preamplifier for precision analog to digital converters like the TSC7135 and TSC800.

The 14-pin dual in line package (DIP) has an external oscillator input to drive the nulling circuitry for optimum noise performance. Both the 8 and 14-pin DIP have an output voltage clamp circuit to minimize overload recovery time.

Pin Configuration



C_A 1
−INPUT 2
+INPUT 3
V_S^- 4
TSC7650
8 C_B
7 V_S^+
6 OUTPUT
5 CLAMP
C_B 1
C_A 2
NC(GUARD) 3
−INPUT 4
+INPUT 5
NC (GUARD) 6
V_S^- 7
TSC7650
14 INT/$\overline{EXT}$
13 EXTERNAL CLOCK INPUT
12 INTERNAL CLOCK OUTPUT
11 V_S^+
10 OUTPUT
9 OUTPUT CLAMP
8 C_{RETN}
NC = NO INTERNAL CONNECTION

Features

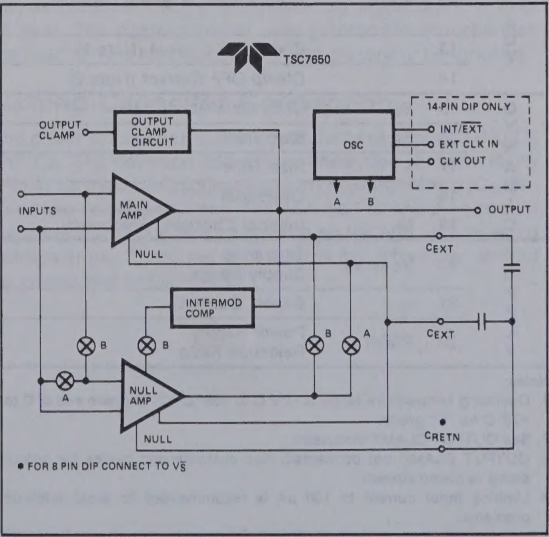
● Low Input Offset Voltage	0.7 μV
● Low Input Offset Voltage Drift	0.05 μV/°C Max.
● Low Input Bias Current	10 pA Max.
● High Impedance Differential CMOS Inputs	10^{12} Ω
● High Open Loop Voltage Gain	120 dB Min.
● Low Input Noise Voltage	2.0 μVp-p
● High Slew Rate	2.5 V/μs
● Low Power Operation	20 mW
● Output Clamp Speeds Recovery Time	
● Compensated Internally for Stable Unity Gain Operation	
● Direct Replacement for ICL7650	
● Available in 8-Pin Dip	

Ordering Information

Part No.	Package	Temp. Range	Max. Offset Voltage
*TSC7650CPA	8-Pin Plastic Dip	0°C to + 70°C	5 μV
*TSC7650IJA	8-Pin CerDIP	-25°C to + 85°C	5 μV
*TSC7650CPD	14-Pin Plastic Dip	0°C to + 70°C	5 μV
*TSC7650IJD	14-Pin CerDIP	-25°C to + 85°C	5 μV

*Available with 160 hour, +125°C burn-in. Add /BI to part number suffix.

Functional Diagram



TSC7650
14-PIN DIP ONLY
OUTPUT CLAMP
OUTPUT CLAMP CIRCUIT
OSC
INT/$\overline{EXT}$
EXT CLK IN
CLK OUT
A
B
INPUTS
MAIN AMP
OUTPUT
NULL
C_{EXT}
INTERMOD COMP
C_{EXT}
B
B
B
A
A
NULL AMP
NULL
C_{RETN}
● FOR 8 PIN DIP CONNECT TO V_S^-

© 1983

TSC7650

Precision Chopper-Stabilized Operational Amplifier

- **0.7 μV Offset Voltage**
- **50 nV/°C Offset Voltage Drift**

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-)	18 Volts
Input Voltage	(V_S^+ + 0.3) to (V_S^- − 0.3) Volts
Storage Temp. Range	-55°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C
Voltage on Oscillator Control Pins	V_S^+ to V_S^-
Output Short Circuit Duration	Indefinite
Current into Any Pin	10 mA
While Operating (Note 4)	100 μA
Operating Temp. Range	
M Device	-55°C to +125°C
I Device	-25°C to +85°C
C Device	0°C to +70°C
Package Power Dissipation (T_A = 25°C)	
CerDIP Package	500 mV
Plastic Package	375 mW

Electrical Characteristics: $V_S^+ = +5$ V, $V_S^- = -5$ V, $C_A = C_B = 0.1$ μF. $T_A = 25°$C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS		TSC7650		UNIT
					MIN	TYP	MAX	
INPUT	1	V_{OS}	Input Offset Voltage	T_A = +25°C	—	± 0.7	± 5.0	μV
				Over Operating Temp. Range (Note 1)	—	± 1.0	—	
	2	$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Average Temp. Coefficient	Operating Temp Range (Note 1)	—	0.01	0.05	μV/°C
	3		Offset Voltage vs Time		—	100	—	$\frac{nV}{\sqrt{month}}$
	4	I_{BIAS}	Input Bias Current	T_A = + 25°C	—	1.5	10	pA
				0°C ≤ T_A ≤ + 70°C	—	35	150	
				-25°C ≤ T_A ≤ + 85°C	—	100	400	
	5	I_{OS}	Input Offset Current	T_A = 25°C	—	0.5	—	pA
	6	e_{np-p}	Input Noise Voltage	R_S = 100 Ω 0 to 10 Hz	—	2	—	μV_{p-p}
	7	i_n	Input Noise Current	f = 10 Hz	—	0.01	—	pA/√Hz
	8	R_{IN}	Input Resistance		—	10^{12}		Ω
	9	CMVR	Common-Mode Voltage Range		-5.0	-5.2 to +2.0	+1.6 V	V
	10	CMRR	Common-Mode Rejection Ratio	CMVR = -5 V to +1. 5 V	120	130	—	dB
OUTPUT	11	A_V	Large-Signal Voltage Gain	R_L = 10 kΩ	120	130	—	dB
	12	V_{OUT}	Output Voltage Swing (Note 3)	R_L = 10 kΩ	± 4.7	± 4.85	—	V
				R_L = 100 kΩ	—	± 4.95	—	
	13		Clamp ON Current (Note 2)	R_L = 100 kΩ	25	70	200	μA
	14		Clamp OFF Current (Note 2)	-4.0 V < V_{OUT} < + 4.0 V	—	1	—	pA
DYNAMIC	15	B_W	Unity Gain Bandwidth	Unity Gain (+1)	—	2.0	—	MHz
	16	S_R	Slew Rate	C_L = 50 pF, R_L = 10 k	—	2.5	—	V/μs
	17	t_r	Rise Time		—	0.2	—	μs
	18		Overshoot		—	20	—	%
	19	f_{ch}	Internal Chopping Frequency	Pins 12-14 Open (DIP)	120	200	375	Hz
SUPPLY	20	V_S^+ to V_S^-	Operating Supply Range		4.5	—	16	V
	21	I_S	Supply Current	No Load	—	2.0	3.5	mA
	22	PSRR	Power Supply Rejection Ratio	V_S = ± 3 V to ± 8 V	120	130	—	dB

Notes:

1. Operating temperature range is -25°C to +85°C for "I" grade and 0°C to +70°C for "C" grade.
2. See OUTPUT CLAMP discussion.
3. OUTPUT CLAMP not connected. See characteristic curves for output swing vs clamp current.
4. Limiting input current to 100 μA is recommended to avoid latch-up problems.
5. Static Sensitive Device. Unused devices must be stored in conductive material to protect devices from possible static damage.
6. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Theory of Operation

Figure 1 shows the major elements of the TSC7650. There are two amplifiers, the main amplifier and the nulling amplifier; both have offset-null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. Two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

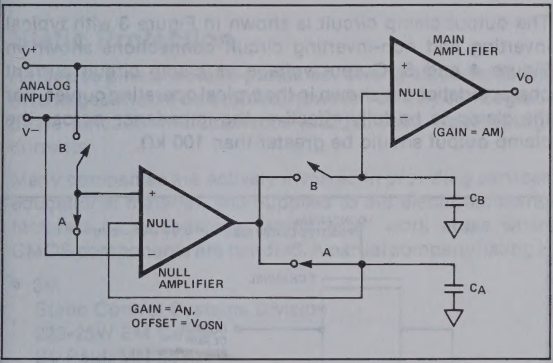


Figure 1: TSC7650 Contains a Nulling and Main Amplifier. Offset Correction Voltages are Stored on Two External Capacitors.

Careful balancing of the input switches minimizes chopper frequency charge injection at the input terminals, and the feed forward-type injection into the compensation capacitor that can cause output spikes in this type of circuit.

The circuits offset voltage compensation is easily shown. With the nulling inputs shorted a voltage almost identical to the nulling amplifier offset voltage is stored on C_A. The effective offset voltage at the null amplifier input is:

$$(1)\quad V_{OSE} = \frac{1}{A_N + 1} V_{OSN}$$

After the nulling amplifier is zeroed the main amplifier is zeroed; the A switches open and B switches close.

The output voltage equation is:

$$(2)\quad V_O = A_M \left[V_{OSM} + (V^+ - V^-) + A_N(V^+ - V^-) + A_N V_{OSE} \right]$$

Substituting (1) → (2) and assuming $A_N >> 1$.

$$(3)\quad V_O = A_M A_N \left[(V^+ - V^-) + \frac{V_{OSM} + V_{OSN}}{A_N} \right]$$

As desired the device offset voltages are reduced by the high open-loop gain of the nulling amplifier.

Output Stage/Load Driving

The output circuit is a high-impedance stage (approximately 18 kΩ). With loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the amplifier is used strictly for dc the lower gain is of little consequence since the dc gain is typically greater than 120 dB even with a 1 kΩ load. In wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or higher. This will result in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier. The clock frequency sets the transition region.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite ac gain of the amplifier results in a small ac signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the TSC7650 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to a finite ac gain. The intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Nulling Capacitor Connection

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (Pin 4) on the 8-pin packages and to capacitor return (C_R, Pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops. The capacitors outside foil, if possible, should be connected to C_R or V_S^-.

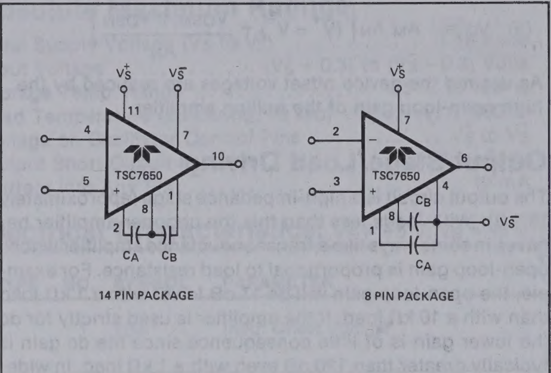


Figure 2: Nulling Capacitor Connection

Clock Operation

The internal oscillator is set for a 200 Hz nominal chopping frequency on both the 8 and 14-pin dual in line packages. With the 14-pin DIP TSC7650, the 200 Hz internal chopping frequency is available at the internal clock output (Pin 12). A 400 Hz nominal signal will be present at the external clock input pin (Pin 13) with $\overline{\text{EXT}}$/INT high or open. This is the internal clock signal before a divide by two operation.

The 14-pin DIP device can be driven by an external clock. Offset voltage and noise characteristics vs chopping frequency are shown in the typical operating characteristic curves. The INT/$\overline{\text{EXT}}$ input (Pin 14) has an internal pull-up and maybe left open for internal clock operation. If an external clock is used INT/$\overline{\text{EXT}}$ must be tied to V_S^- (Pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (Pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ± 6 V and between V^+ and V^+ -6 V for higher supply voltages.

At low frequencies the external clock duty cycle is not critical since an internal divide by two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50-80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitor pins are very low. At 25° C a typical TSC7650 will drift less than 10 μV/sec.

Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TSC7650 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3 with typical inverting and non-inverting circuit connections shown in Figure 4 and 5. Output voltage vs clamp circuit current characteristics are shown in the typical operating curves. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 kΩ.

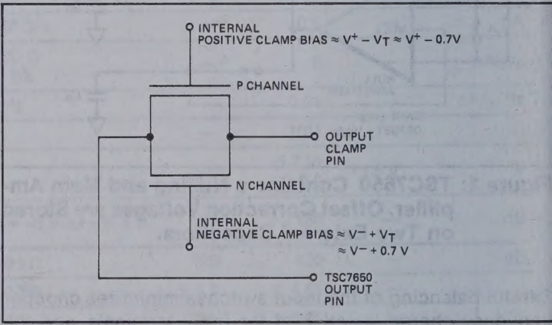

INTERNAL
POSITIVE CLAMP BIAS ≈ $V^+ - V_T \approx V^+ - 0.7V$
P CHANNEL
OUTPUT
CLAMP
PIN
N CHANNEL
INTERNAL
NEGATIVE CLAMP BIAS ≈ $V^- + V_T$
≈ $V^- + 0.7$ V
TSC7650
OUTPUT
PIN

Figure 3: Internal Clamp Circuit

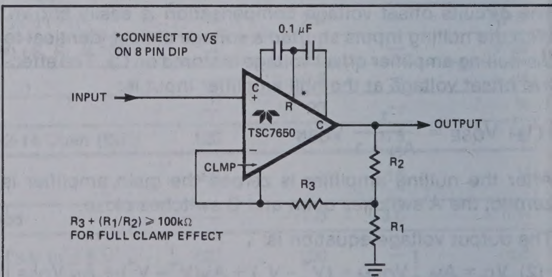


Figure 4: Non-Inverting Amplifier with Optional Clamp

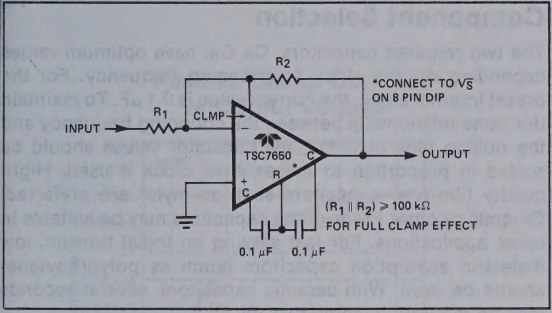


Figure 5: Inverting Amplifier with Optional Clamp

Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational material, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520
- American Convertors
  1919 South Butlerfield Road
  Mundelein, IL 60060
  (312) 362-9000
- ACL
  1960 East Devon Avenue
  Elk Grove Village, IL 60007
  (312) 981-9212

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low impedance state, resulting in excessive supply current. To avoid the condition, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latchup.

Thermo-Electric Potentials

Precision dc measurements are ultimately limited by thermoelectric potentials developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1 μV/° C, but up to tens of μV/° C for some materials, will be generated. In order to realize the benefits extremely low offset voltages provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially those caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and separation from surrounding heat-dissipating elements is advised.

Pin Compatibility

On the 8-pin mini-dip TSC7650 the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or are used for offset potentiometer or compensation capacitor connections.

For OPO5 and OPO7 operational amplifiers, the replacement of the offset null pot between pins 1 and 8 by two capacitors from the pins to $V_{\bar{S}}$ will convert the OPO5/07 pin configuration for TSC7650 operation. For LM108 devices the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pin outs are modified similarly by also removing any circuit connections to pin 5. On the TSC7650 pin 5 is the output clamp connection. Other operational amplifiers may use this pin as an offset or compensation point.

The minor modifications needed to retrofit a TSC7650 into existing sockets operating at reduced power supply voltages make prototyping and circuit verification straight forward.

Input Guarding

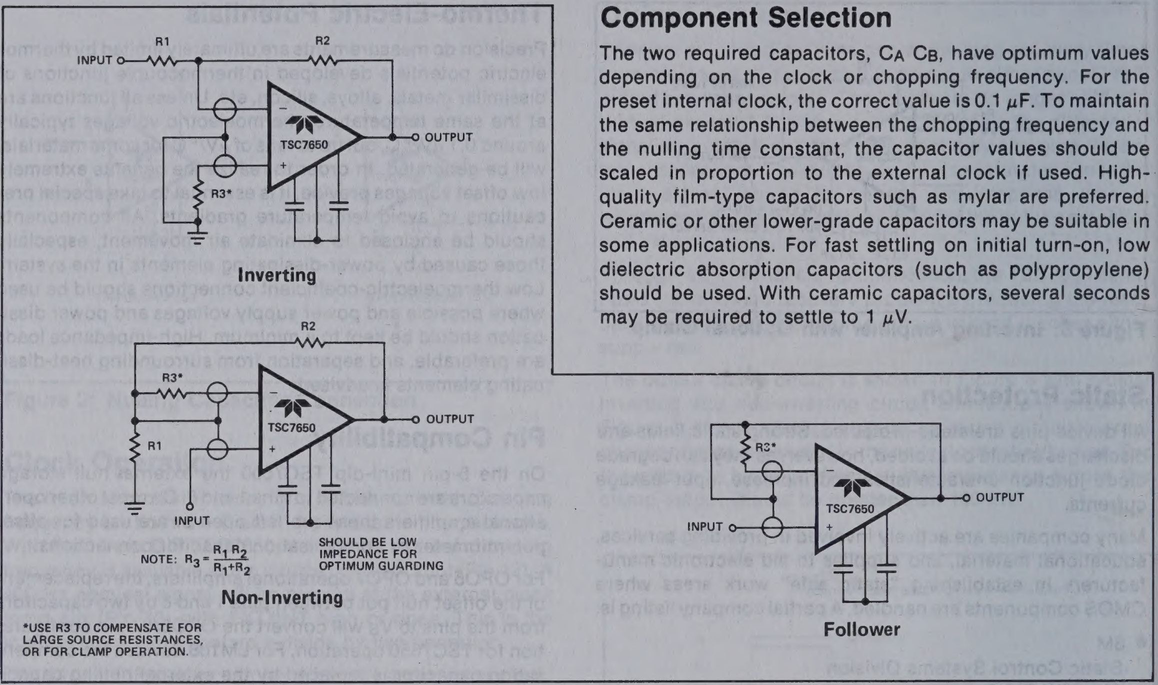
High impedance, low leakage CMOS inputs allow the TSC7650 to make measurements of high impedance sources. Stray leakage paths can increase input currents and decrease input resistance unless inputs are guarded. A guard is a conductive pc trace surrounding the input terminals. The ring connects to a low impedance point as the same potential as the inputs. Stray leakages are absorbed by the low impedance ring. The equal potential between ring and inputs prevents input leakage currents. Typical guard connections are shown in Figure 6.

The 14-pin DIP configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are unused.

In applications requiring low leakage currents, boards should be cleaned thoroughly and blown dry after soldering. Protective coatings will prevent future board contamination.

Component Selection

The two required capacitors, C_A C_B, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock if used. High-quality film-type capacitors such as mylar are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 μV.


INPUT
R1
R2
–
+
TSC7650
OUTPUT
R3*
Inverting
R2
R3*
–
+
TSC7650
OUTPUT
R1
INPUT
Non-Inverting
R3*
–
+
TSC7650
OUTPUT
INPUT
Follower

SHOULD BE LOW IMPEDANCE FOR OPTIMUM GUARDING

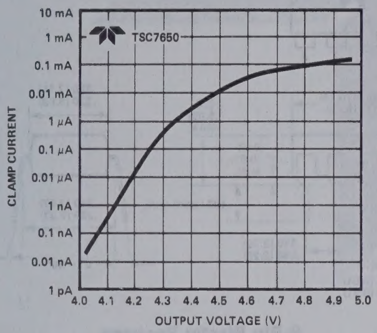
NOTE: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$

*USE R3 TO COMPENSATE FOR LARGE SOURCE RESISTANCES, OR FOR CLAMP OPERATION.

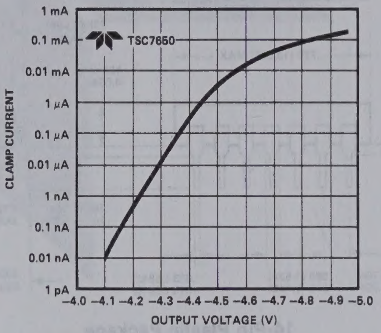
Figure 6: Input Guard Connection

Typical Characteristic Curves

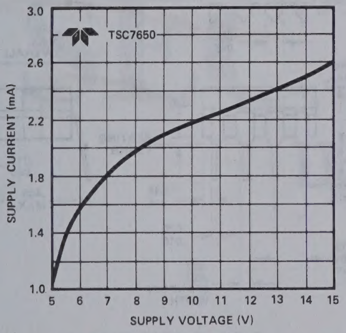
Positive Clamp Current vs Output Voltage



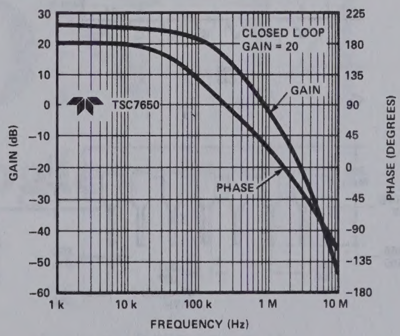
Negative Clamp Current vs Output Voltage



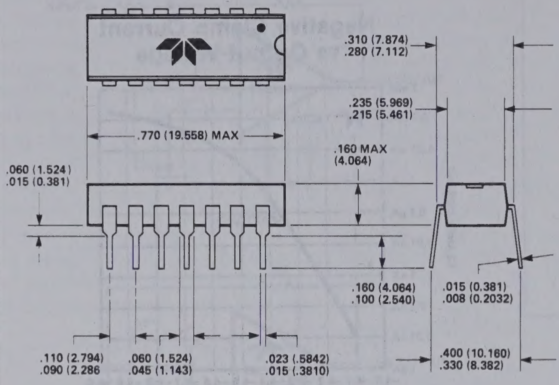
Supply Current vs Supply Voltage



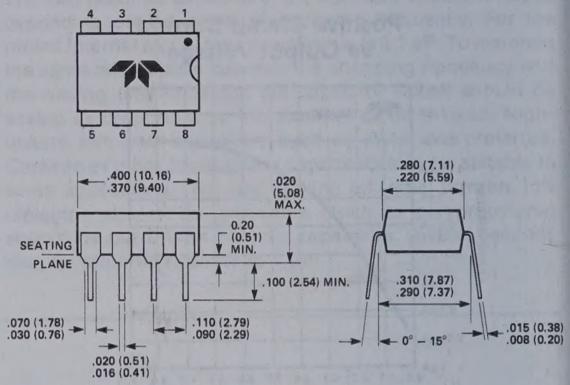
Gain/Phase vs Frequency



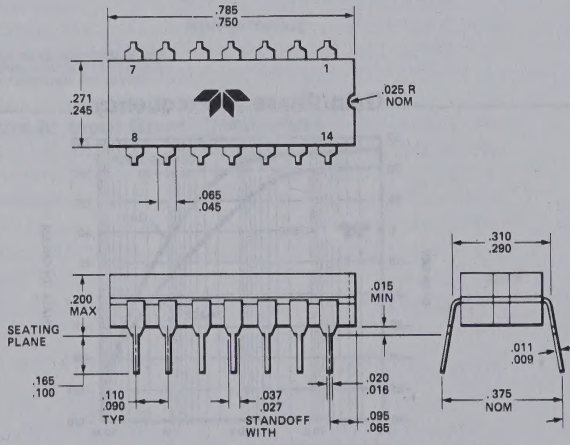
Package Outline


.310 (7.874)
.280 (7.112)
.235 (5.969)
.215 (5.461)
.770 (19.558) MAX
.160 MAX
(4.064)
.060 (1.524)
.015 (0.381)
.160 (4.064)
.100 (2.540)
.015 (0.381)
.008 (0.2032)
.110 (2.794)
.090 (2.286)
.060 (1.524)
.045 (1.143)
.023 (.5842)
.015 (.3810)
.400 (10.160)
.330 (8.382)

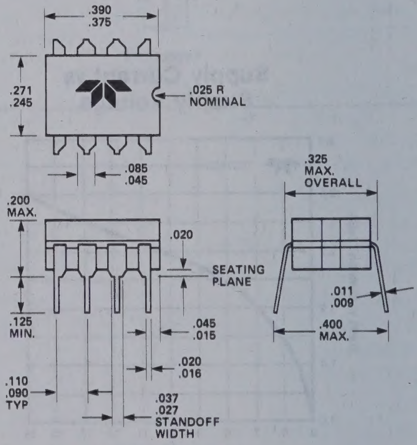
14-Pin Plastic Package
(Package #6)


4
3
2
1
5
6
7
8
.400 (10.16)
.370 (9.40)
.020
(5.08)
MAX.
.280 (7.11)
.220 (5.59)
SEATING
PLANE
0.20
(0.51)
MIN.
.100 (2.54) MIN.
.310 (7.87)
.290 (7.37)
.070 (1.78)
.030 (0.76)
.110 (2.79)
.090 (2.29)
0° – 15°
.015 (0.38)
.008 (0.20)
.020 (0.51)
.016 (0.41)

8-Pin Plastic Package
(Package #4)


.785
.750
7
1
8
14
.271
.245
.025 R
NOM
.065
.045
.310
.290
.200
MAX
.015
MIN
SEATING
PLANE
.011
.009
.165
.100
.110
.090
TYP
.037
.027
STANDOFF
WITH
.020
.016
.095
.065
.375
NOM

14-Pin CerDIP Package
(Package #7)


.390
.375
.271
.245
.025 R
NOMINAL
.085
.045
.325
MAX.
OVERALL
.200
MAX.
.020
SEATING
PLANE
.011
.009
.125
MIN.
.045
.015
.400
MAX.
.020
.016
.110
.090
TYP
.037
.027
STANDOFF
WIDTH

8-Pin CerDIP Package
(Package #5)

SECTION 14

Digital Logic

Section 14

Digital Logic 14-3
Purpose of Bipolar Interface Logic 14-5
Most Popular 300 Series Devices 14-6
Electrical Summary Data 14-8
Digital Logic — 300 Series Ordering Information 14-9
Input Current Requirements 14-10
Output Sink Current vs Output Voltage 14-11
Power Supply Current and Delay Times 14-12
Pin-Out Guide 14-13

The Information in this section is in summary form and is intended for a quick evaluation of the products available and their electrical performance. For more detailed performance characteristics a separate Bipolar Interface Data Book is available. Please contact your local sales office for a copy.

Bipolar Interface Logic

Purpose of Bipolar Interface Logic

PROTECTING CMOS AND μP SYSTEMS

Bipolar Interface Logic - the 300 Series - is a remarkably simple solution to interfacing your CMOS and μp systems (which operate on 12 or 15V power supplies) with the outside world.

OPERATION ON 11V TO 16V

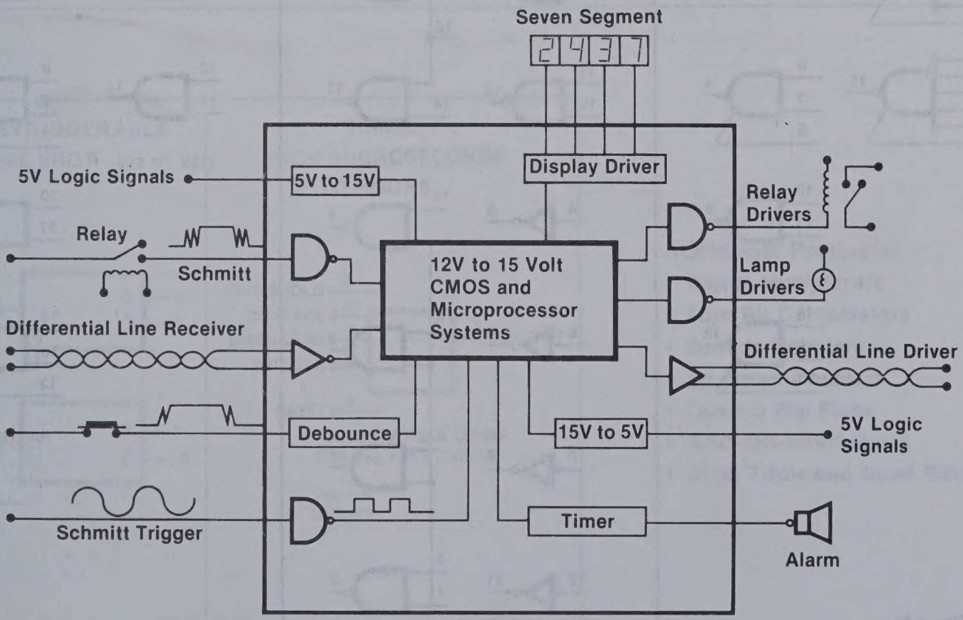
These bipolar circuits have the unique ability to operate on 11V to 16V power supplies with an input threshold of 6V, which allows noise margins from 3.5V up to 6.5V. This eliminates worry about the high-voltage spikes or noise generated by bouncing switches, SCR's, relays, solenoids or large motors. Also, the rugged bipolar construction of the 300 series minimizes catastrophic failures often caused by high voltage spikes or improper maintenance.

LOW OUTPUT IMPEDANCE

With low output impedances, the 300 series can handle high drive currents of up to 250mA, which makes them ideal for driving relays, solenoids, SCR's, displays or long lines.

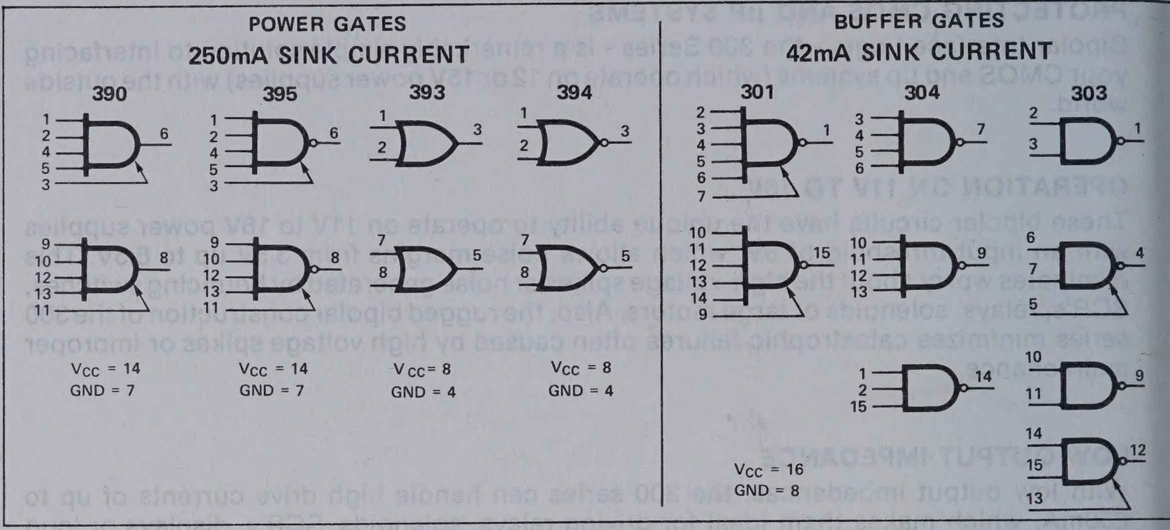
MANY SOLUTIONS OFFERED BY THE 300 SERIES

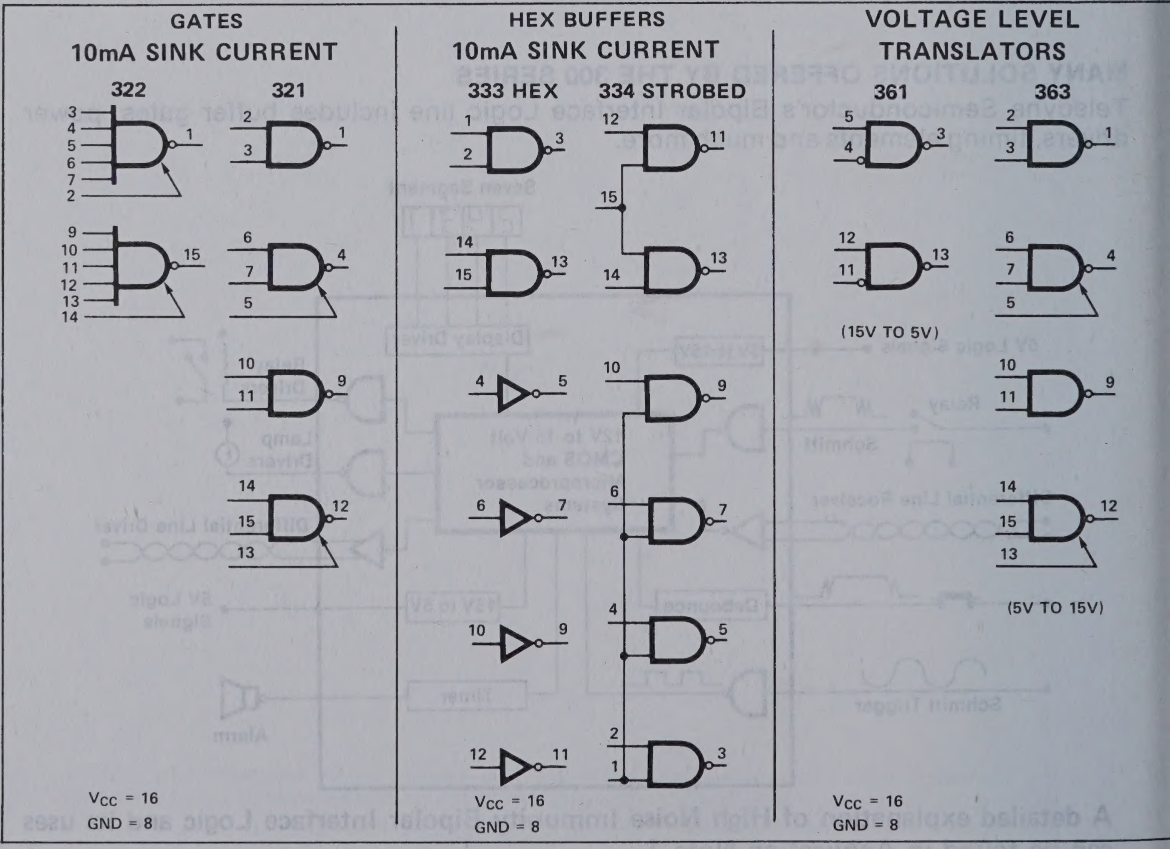
Teledyne Semiconductor's Bipolar Interface Logic line includes buffer gates, power drivers, timing elements and much more.


Seven Segment
2437
Display Driver
5V Logic Signals
5V to 15V
Relay
Schmitt
Differential Line Receiver
Debounce
Schmitt Trigger
12V to 15 Volt CMOS and Microprocessor Systems
Relay Drivers
Lamp Drivers
Differential Line Driver
15V to 5V
5V Logic Signals
Timer
Alarm

A detailed explanation of High Noise Immunity Bipolar Interface Logic and its uses can be found in Application Note 1.

Most Popular 300 Series Devices

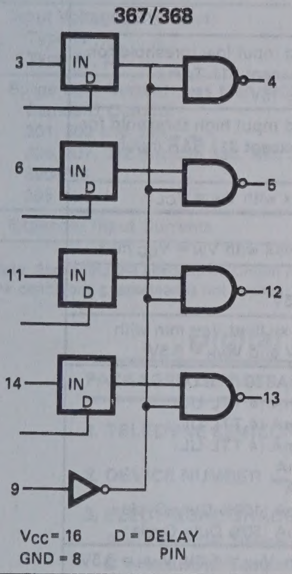

POWER GATES
250mA SINK CURRENT
390
395
393
394
1 2 4 5 3 6
9 10 12 13 11 8
1 2 3
7 8 5
Vcc = 14
GND = 7
Vcc = 14
GND = 7
Vcc = 8
GND = 4
Vcc = 8
GND = 4
BUFFER GATES
42mA SINK CURRENT
301
304
303
2 3 4 5 6 7 1
10 11 12 13 14 9 15
3 4 5 6 7
10 11 12 13 9
1 2 15 14
2 3 1
6 7 5 4
10 11 9
14 15 13 12
Vcc = 16
GND = 8


GATES
10mA SINK CURRENT
322
321
3 4 5 6 7 2 1
9 10 11 12 13 14 15
2 3 1
6 7 5 4
10 11 9
14 15 13 12
Vcc = 16
GND = 8
HEX BUFFERS
10mA SINK CURRENT
333 HEX
334 STROBED
1 2 3
14 15 13
4 5
6 7
10 9
12 11
12 11
15
14 13
10 9
6 7
4 5
2 1 3
Vcc = 16
GND = 8
VOLTAGE LEVEL
TRANSLATORS
361
363
5 4 3
12 11 13
(15V TO 5V)
2 3 1
6 7 5 4
10 11 9
14 15 13 12
(5V TO 15V)
Vcc = 16
GND = 8

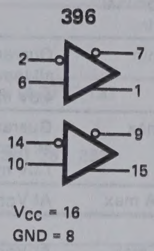
Bipolar Interface Logic

Most Popular 300 Series Devices

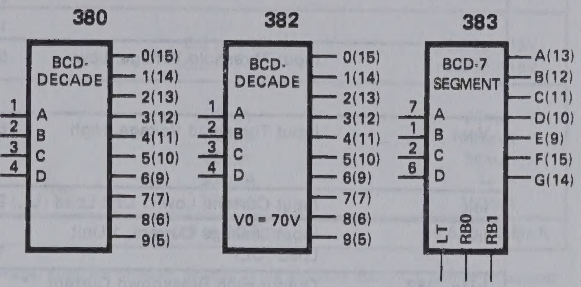
QUAD SCHMITT TRIGGER


367/368
3
IN
D
4
6
IN
D
5
11
IN
D
12
14
IN
D
13
9
VCC = 16
GND = 8
D = DELAY PIN

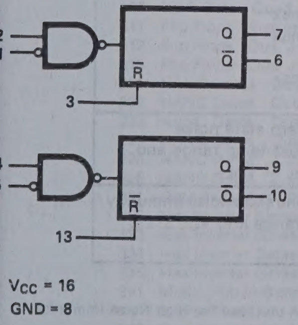
DIFFERENTIAL LINE DRIVER/ RECEIVER


396
2
6
7
1
14
10
9
15
VCC = 16
GND = 8

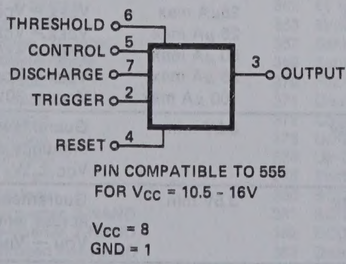
DECODERS/DRIVERS


380
BCD-DECADE
1 A
2 B
3 C
4 D
0(15)
1(14)
2(13)
3(12)
4(11)
5(10)
6(9)
7(7)
8(6)
9(5)
382
BCD-DECADE
1 A
2 B
3 C
4 D
V0 = 70V
0(15)
1(14)
2(13)
3(12)
4(11)
5(10)
6(9)
7(7)
8(6)
9(5)
383
BCD-7 SEGMENT
7 A
1 B
2 C
6 D
LT
RB0
RB1
A(13)
B(12)
C(11)
D(10)
E(9)
F(15)
G(14)

DUAL RETRIGGERABLE ONE SHOT


Q
7
Q̄
6
R̄
3
Q
9
Q̄
10
R̄
13
VCC = 16
GND = 8

TIMER FROM MICROSECONDS TO HOURS


THRESHOLD 6
CONTROL 5
DISCHARGE 7
TRIGGER 2
RESET 4
3 OUTPUT
PIN COMPATIBLE TO 555 FOR VCC = 10.5 - 16V
VCC = 8
GND = 1

Additional Products:

- Digital Multiplexers
- Four Bit Comparators
- Decade Counters
- Up/Down Counters
- Quad D Flip Flops
- AND-OR-Invert Gates
- Dual, Triple and Quad Gates

Bipolar Interface Logic Electrical Summary Data

Parameter		Definition	Type C* (V_{CC} = +12V ±1V) -30° C ≤ T_A ≤ +85° C	Test Conditions
V_{CC}		Supply Voltage	13V max 12V nominal 11V min	(Voltage for other tests — see below)
V_{INL}		Input Threshold Voltage, Low	5.0V min	Guaranteed input low threshold for all inputs except 311 T_2 = 4.8V min @ 15V
V_{INH}		Input Threshold Voltage, High	6.5V max	Guaranteed input high threshold for all inputs except 311 $\overline{S}$&$\overline{R}$ inputs = 7.0V max
I_{INL}		Input Current, Low; 1 Unit Load (UL)	2.1 mA max	At V_{CC} max with V_{IN} = V_{OL}
I_{INH}		Input Leakage Current; 1 Unit Load (UL)	10 μA max	At V_{CC} = max with V_{IN} = V_{CC} max
I_{MAX}	382	Output High Breakdown Current (Open Collector Devices)	2 mA max	V_{CEX} = +65V
V_{OL}		Output Low Voltage (see Loading Table on Data Sheet)	1.5V max	I_{OL} = F.O. x UL at V_{CC} min with V_{INL} = 5.0V and V_{INH} = 6.5V
V_{OL}	302	Output Low Voltage (Open Collector Devices)	.4V max	I_{OL} = 16 mA (10 TTL UL)
	323		.4V max	I_{OL} = 6.4 mA (4 TTL UL)
	332		.4V max	I_{OL} = 6.4 mA (4 TTL UL)
	334		.4V max	I_{OL} = 6.4 mA (4 TTL UL)
	380		1.2V max	I_{OL} = 30 mA
	382		2.5V max	I_{OL} = 7 mA
	383		.7V max	I_{OL} = 20 mA (100% Duty Cycle)
	383		1.2V max	I_{OL} = 40 mA (50% Duty Cycle)
V_{OH}		Output High Voltage of all Devices Without Open Collector Except 362 and 396	10.0V min	At V_{CC} min, V_{INL} = 5.0V, V_{INH} = 6.5V; I_{OH} = F.O. x UL
V_{MAX}	302,323	Output High Breakdown Voltage (Open Collector Devices)	13.0V min	I_{MAX} = 4 mA
	332,334		20.0V min	I_{MAX} = 4 mA
	380		24.0V min	I_{MAX} = 0.5 mA
	381		15.0V min	I_{MAX} = 0.5 mA
	390-395		30.0V min	
V_{OHL}		Output High Voltage, Loaded, of Active Pullup Devices Except 362 and 306	7.0V min	At V_{CC} nominal, V_{INL} = 5.0V, V_{INH} = 6.5V; I_{OH} = -5 mA (except -15 mA for 301 and -12 mA for 350,351
I_{CEX}	302,323,307	Output High Leakage Current (Open Collector Devices)	25 μA max	V_{CEX} = V_{CC} max
	332,334		25μA max	V_{CEX} = V_{CC} max
	380,381		25 μA max	V_{CEX} = V_{CC} max
	382		50 μA max	V_{CEX} = +55V
	383		25 μA max	V_{CEX} = V_{CC} max
	390-395		100 μA max	V_{CEX} = 30V
"0" N.I.		Zero State Noise Immunity	3.5V min	Guaranteed zero state noise immunity across temp range and V_{CC} ± 1V. V_{INL} — V_{OL}
"I" N.I.		One State Noise Immunity	3.5V min	Guaranteed one state noise immunity across temp range and V_{CC} ± 1V. V_{OH} — V_{INH}

Notes: F.O. is fanout in unit loads (UL). Unit loadings are given in the pin tables on the individual data sheets. A unit load for High Noise Immunity Logic is defined by the above input specifications.

See individual data sheets for additional specifications.

*Military spec Type B (V_{CC} = 12V) and Type M (V_{CC} = 15V) are available to meet -55° C to +125° C temperature requirements. Available in ceramic package only. See ordering data.

Electrical Summary Data (Continued)

Absolute Maximum Ratings

	L Package, Ceramic	J Package, Plastic
Storage Temperature	-65° C to +150° C	-55° C to +100° C
Lead Temperature (1/16 inch from case, 10 sec max)	300° C	300° C
Continuous Supply Voltage		
Type C*, B*	+15.0V	+15.0V
Type A*, M*	+16.5V	+16.5V
Pulsed Supply Voltage (less than 100 msec)	+18.0V	+18.0V
Input Voltage (any input)		
Type C*, B*	-0.5 to +15V	-0.5 to +15V
Type A*, M*	-0.5 to +18V	-0.5 to +18V
Surge Sink Current (less than 100 msec at 25° C T_A)		
Standard Outputs	20mA	20mA
301, 302 and 303	100mA	100mA
306, 307, 332 through 335, 350, 351, 380, 381, 383	35mA	35mA
390-395	300mA	—
355	150mA	150mA
Expander Input Currents	-0.5 to +0.5mA	-0.5 to +0.5mA

Note: Exceeding the absolute maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Digital Logic — 300 Series Ordering Information

PACKAGED DEVICES TSC XXX X X

1. TELEDYNE SEMICONDUCTOR DEVICE

2. DEVICE NUMBER

3. ELECTRICAL GRADE AND TEMPERATURE RANGE

A — Industrial Temperature Range, 15 V, (−30 to +70°C)
C — Industrial Temperature Range, 12 V, (−30 to +85°C)

4. PACKAGE TYPE

L — Ceramic Package (CerDIP)

EXAMPLE: 303AL Operates Over an Industrial Temperature Range at 15 V and is a CerDIP Package

Product List — Digital Logic

301	Power NAND Gates Dual 5-Input
302	Power NAND Gates Quad 2-Input
303	Power NAND Gates Quad 2-Input
304	Power NAND Gates Triple 4, 3, 4-Input
306	NOR Gate Quad 2, 2, 3, 3-Input
307	NOR Gate Quad 2, 2, 3, 3-Input
311	Flip Flops Master/Slave RST
312	Flip Flops Dual J-K Edge Triggered
313	Flip Flops Dual J-K Master/Slave
321	NAND Gates Quad 2-Input
322	NAND Gates Dual 5-Input
323	NAND Gates Quad 2-Input
324	NAND Gates Quad 2-Input
325	NAND Gates 2, 2, 3, 3-Input
326	NAND Gates 2, 2, 3, 3-Input
331	Gate Expander Dual 5-Input
332	Hex Inverter Gates 4-Inverter, 2-NAND
333	Hex Inverter Gates 4-Inverter, 2-NAND
334	Hex Inverter Gates Strobed Hex NAND
335	Hex Inverter Gates Strobed Hex NAND
341	Multifunction Gates Dual 2-Wide, 2-Input and/or Invert
342	Dual Monostable Multivibrator
343	Digital Comparator 4-Bit
344	Multifunction Gates Dual Expandable AND-NOR
347	Dual Retriggerable Monostable Multivibrator
350	Multiplexers 8-Bit
351	Multiplexers Dual 4-Bit
355	Timer
361	Dual 11-16V to 5V Interface Voltage Translator
362	5V to 11-16V Interface Dual Translator
363	5V to 11-16V Interface Quad 2-Input NAND
367	Schmitt Trigger Quad(Active Pullup)
368	Schmitt Trigger Quad(Open Collector)
370	Flip Flop Quad D
371	Counters Decade
372	Counters Hexadecimal
373	Up-Down Counters Decade
374	Up-Down Counters Hexadecimal
375	Shift Register 4-Bit
380	BCD-to-Decade Decoder/Drivers Lamp Driver
381	BCD-to-Decade Decoder/Drivers Logic Driver
382	BCD-to-Decade Decoder/Drivers Gas Tube Driver
383	Decoder/Driver BCD-to-7 Segment
390	Dual Interface Buffers 4-Input Expandable AND
391	Dual Interface Buffers 2-Input AND
392	Dual Interface Buffers 2-Input NAND
393	Dual Interface Buffers 2-Input OR
394	Dual Interface Buffers 2-Input NOR
395	Dual Interface Buffers 4-Input Expandable NAND
396	Line Driver/Receiver Dual Differential

14

Bipolar Interface Logic

Input Current Requirements

Device Number	I_{INL} @ V_{CC} = 12V and V_{IL} = 1.5V (mA)	I_{INL} @ V_{CC} = 15V and V_{IL} = 1.5V (mA)	I_{INH} @ V_{CC} = 12 or 15V, V_{INH} = V_{CC} (mA)
301	2.1	2.6	10
302	2.1	2.6	10
303	2.1	2.6	10
304	2.1	2.6	10
306	1.3	1.6	10
307	1.3	1.6	10
311	2.1-4.2	2.6-5.2	10-20
312	2.1-4.2	2.6-5.2	10-20
313	2.1-4.2	2.6-5.2	10-20
321	2.1	2.6	10
322	2.1	2.6	10
323	2.1	2.6	10
324	2.1	2.6	10
325	2.1	2.6	10
326	2.1	2.6	10
332	2.1	2.6	10
333	2.1	2.6	10
334	2.1	2.6	10
335	2.1	2.6	10
341	2.1	2.6	10
342	2.1	2.6	10
343	2.1-4.2	2.6-5.2	10-20
347	2.1-4.2	2.6-5.2	10-20
349	2.1	2.6	10
350	2.1	2.6	10
351	2.1	2.6	10
355	0.01	0.01	10
361	2.1	2.6	10
362	0.47	0.47	10
363	1.6	1.6	10
367	2.1	2.6	40
368	2.1	2.6	40
370	2.1-4.2	2.6-5.2	10-20
371	2.1-4.2	2.6-5.2	10-20
372	2.1-4.2	2.6-5.2	10-20
373	2.1	2.6	10
374	2.1	2.6	10
375	2.1	2.6	10
380	2.1	2.6	10
381	2.1	2.6	10
382	2.1	2.6	10
383	2.1-6.3	2.6-7.8	10-30
390	0.7	1.0	10
391	0.7	1.0	10
392	0.7	1.0	10
393	0.7	1.0	10
394	0.7	1.0	10
395	0.7	1.0	10
396	0.4	1.0	10

Notes:

1. If there are several types of inputs on a device, then the currents listed above are the range of values for the various inputs. Check the individual data sheets to determine what the input current requirements are for each input.
2. A unit load is defined as I_{INL} @ 12V = 2.1mA max, I_{INL} @ 15V = 2.6mA max and I_{INH} = 10μA max at 12 or 15V.
3. CMOS operated at 12 or 15V can be used to drive these devices even if the V_{OL} rating of the CMOS device does not appear to give enough sink current. This is possible since the 300 series of devices has input low rated at ≤5V instead of 0.8V as i common with TTL parts. The result is the CMOS output will be operated at a V_{OL} larger than is typical for CMOS or TTL systems.

Output Sink Current vs. Output Voltage

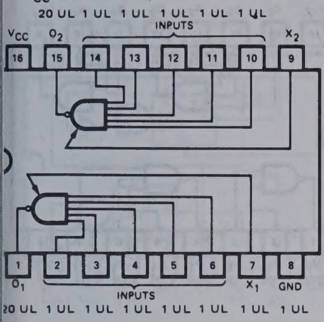
Device Number	V_{OL} (V)	I_{OL} (mA)	Device Number	V_{OL} (V)	I_{OL} (mA)
301	1.5	42	350	1.5	16
302	.4	42	351	1.5	16
303	.4	42	355	2.0	75
304	.4	42	361	.4	10
306	1.5	18	362	.4	10
307	.4	10	363	.4	30
311	1.5	12	367	1.5	10
312	1.5	10	368	.4	10
313	1.5	10	370	.4	10
321	1.5	10	371	.4	10
322	1.5	10	372	.4	10
323	.4	10	373	1.5	10
324	.4	10	374	1.5	10
325	1.5	10	375	1.5	6
326	.4	10	380	.4	20
332	.4	10	381	.4	10
333	.4	10	382	2.5	7
334	.4	10	383	.7	20
335	.4	10	390	.7	250
341	1.5	10	391	.7	250
342	1.5	10	392	.7	250
343	1.5	10	393	.7	250
			394	.7	250
347	1.5	10	395	.7	250
349	1.5	10	396	1.5	12

Bipolar Interface Logic

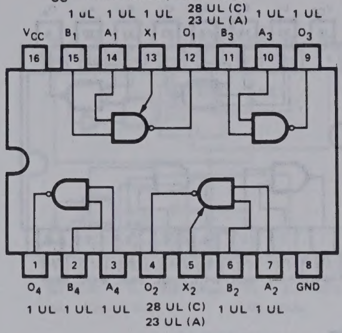
Power Supply Current and Delay Times

			Delay Time 50% to 50% Points (Worst Case)	
Device Number	ICC 13V	(mA) 16V	Low to High (ns)	High to Low (ns)
301	48	68	340	400
302	40	60	600	240
303	49	70	600	240
304	49	70	600	240
306	34	40	600	100
307	34	40	600	100
311	18	25	820	610
312	30	40	300	230
313	30	40	300	230
321	15	20	300	200
322	8	11	550	190
323	5.5	8	400	160
324	28	40	600	200
325	15	20	300	200
326	28	40	600	200
332	28	42	350	140
333	42	60	350	140
334	28	42	350	140
335	42	60	350	140
341	11	15	410	150
342	17	23	260	160
343	42	56	1000	1000
344	11	15	600	200
347	40	50	650	750
350	33	40	400	250
351	33	40	400	250
361	8	11	325	230
362	10	13	400	160
363	51	64	600	240
367	36	54	400	300
368	33	50	600	340
370	38	48	750	750
371	41	53	800	300
372	41	53	800	300
373	50	55	1 mHz	Toggle
374	50	55	1 mHz	Toggle
375	48	64	600	550
380	24	31	500	400
381	30	38	500	400
382	24	31	—	—
383	24	31	—	—
390	38	40	500	200
391	38	40	500	200
392	38	40	500	200
393	38	40	500	200
394	38	40	500	200
395	38	40	500	200
396	23	25	650	80

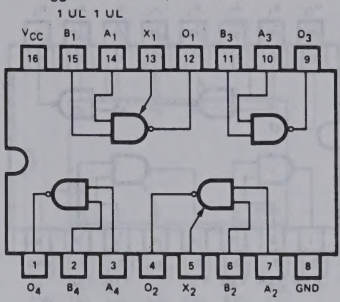
1 DUAL FIVE INPUT POWER NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 48 mA (301C), 68 mA (301A)


20 UL 1 UL 1 UL 1 UL 1 UL 1 UL
INPUTS
VCC O2 X2
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O1 INPUTS X1 GND
20 UL 1 UL 1 UL 1 UL 1 UL 1 UL 1 UL 1 UL

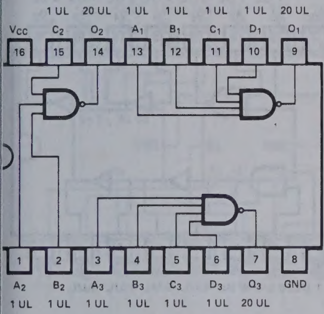
302 QUAD TWO INPUT POWER GATE
(OPEN COLLECTOR)
I_{CC} = 40 mA (302C), 60 mA (302A)


1 UL 1 UL 1 UL 28 UL (C) 23 UL (A) 1 UL 1 UL
VCC B1 A1 X1 O1 B3 A3 O3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O4 B4 A4 O2 X2 B2 A2 GND
1 UL 1 UL 1 UL 28 UL (C) 23 UL (A) 1 UL 1 UL

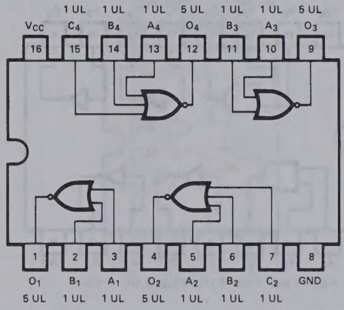
303 QUAD TWO INPUT POWER GATE
(PASSIVE PULL-UP)
I_{CC} = 49 mA (303C), 70 mA (303A)


1 UL 1 UL
VCC B1 A1 X1 O1 B3 A3 O3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O4 B4 A4 O2 X2 B2 A2 GND

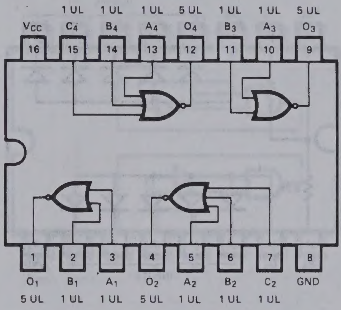
4 TRIPLE 4, 3, 4 INPUT NAND
(PASSIVE PULL-UP)
I_{CC} = 40 mA (304C), 60 mA (304A)


1 UL 20 UL 1 UL 1 UL 1 UL 1 UL 20 UL
VCC C2 O2 A1 B1 C1 D1 O1
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
A2 B2 A3 B3 C3 D3 O3 GND
1 UL 1 UL 1 UL 1 UL 1 UL 1 UL 20 UL

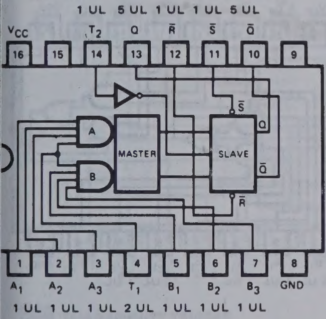
306 2, 2, 3, 3 INPUT NOR GATE
(ACTIVE PULL-UP)
I_{CC} = 34 mA (306C), 40 mA (306A)


1 UL 1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
VCC C4 B4 A4 O4 B3 A3 O3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O1 B1 A1 O2 A2 B2 C2 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL 1 UL

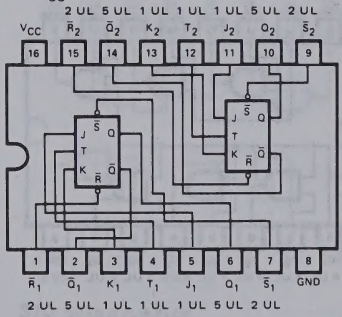
307 2, 2, 3, 3 INPUT NOR GATE
(OPEN COLLECTOR)
I_{CC} = 23 mA (307C), 28 mA (307A)


1 UL 1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
VCC C4 B4 A4 O4 B3 A3 O3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O1 B1 A1 O2 A2 B2 C2 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL 1 UL

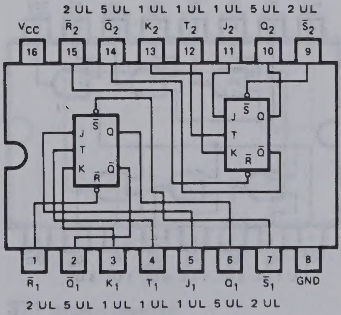
11 MASTER/SLAVE FLIP-FLOP
(ACTIVE PULL-UP)
I_{CC} = 18 mA (311C) 25 mA (311A)


1 UL 5 UL 1 UL 1 UL 5 UL
VCC T2 Q R̄ S̄ Q̄
16 15 14 13 12 11 10 9
A
B
MASTER
SLAVE
S̄
Q
Q̄
R̄
1 2 3 4 5 6 7 8
A1 A2 A3 T1 B1 B2 B3 GND
1 UL 1 UL 1 UL 2 UL 1 UL 1 UL 1 UL

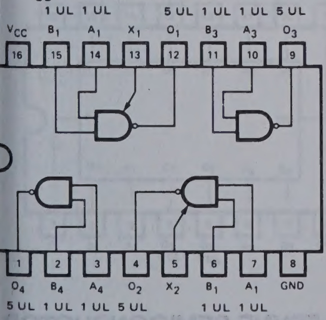
312 DUAL J-K FLIP-FLOP
(ACTIVE PULL-UP)
I_{CC} = 30 mA (312C) 40 mA (312A)


2 UL 5 UL 1 UL 1 UL 1 UL 5 UL 2 UL
VCC R̄2 Q̄2 K2 T2 J2 Q2 S̄2
16 15 14 13 12 11 10 9
J S̄ Q
T
K R̄ Q̄
1 2 3 4 5 6 7 8
R̄1 Q̄1 K1 T1 J1 Q1 S̄1 GND
2 UL 5 UL 1 UL 1 UL 1 UL 5 UL 2 UL

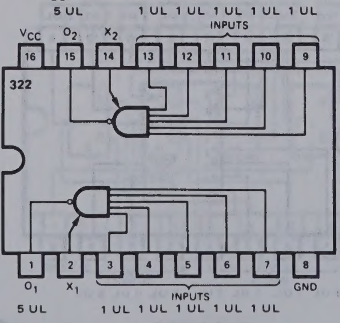
313 DUAL J-K FLIP-FLOP
(ACTIVE PULL-UP)
I_{CC} = 30 mA (312C) 40 mA (312A)


2 UL 5 UL 1 UL 1 UL 1 UL 5 UL 2 UL
VCC R̄2 Q̄2 K2 T2 J2 Q2 S̄2
16 15 14 13 12 11 10 9
J S̄ Q
T
K R̄ Q̄
1 2 3 4 5 6 7 8
R̄1 Q̄1 K1 T1 J1 Q1 S̄1 GND
2 UL 5 UL 1 UL 1 UL 1 UL 5 UL 2 UL

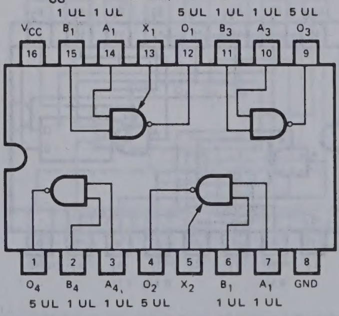
21 QUAD TWO INPUT NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 15 mA (321C), 20 mA (321A)


1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
VCC B1 A1 X1 O1 B3 A3 O3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O4 B4 A4 O2 X2 B1 A1 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL

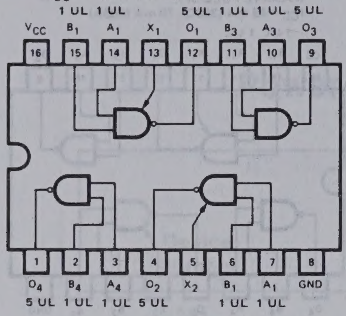
322 DUAL FIVE INPUT NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 8 mA (322C), 11 mA (322A)


5 UL 1 UL 1 UL 1 UL 1 UL 1 UL
INPUTS
VCC O2 X2
16 15 14 13 12 11 10 9
322
1 2 3 4 5 6 7 8
O1 X1 INPUTS GND
5 UL 1 UL 1 UL 1 UL 1 UL 1 UL

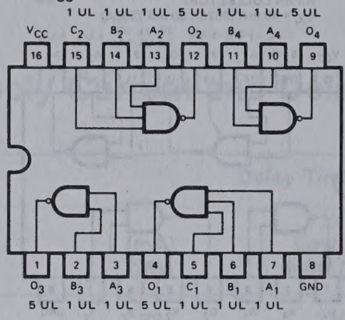
323 QUAD TWO INPUT NAND GATE
(OPEN COLLECTOR)
I_{CC} = 5.5 mA (323C), 8 mA (323A)


1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
VCC B1 A1 X1 O1 B3 A3 O3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O4 B4 A4 O2 X2 B1 A1 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL

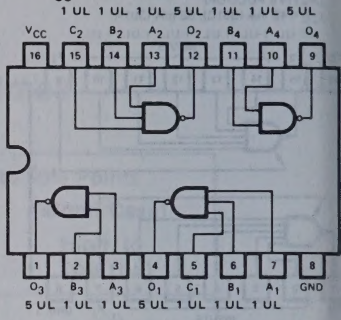
324 QUAD TWO INPUT NAND GATE
(PASSIVE PULL-UP)
I_{CC} = 28 mA (324C), 40 mA (324A)


1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
V_{CC} B_1 A_1 X_1 O_1 B_3 A_3 O_3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_4 B_4 A_4 O_2 X_2 B_1 A_1 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL

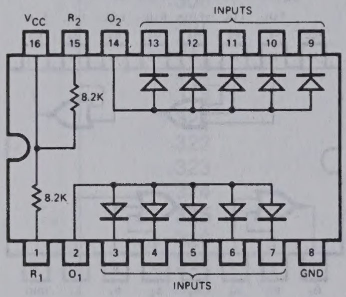
325 2, 2, 3, 3-INPUT NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 15 mA (325C), 20 mA (325A)


1 UL 1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
V_{CC} C_2 B_2 A_2 O_2 B_4 A_4 O_4
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_3 B_3 A_3 O_1 C_1 B_1 A_1 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL 1 UL

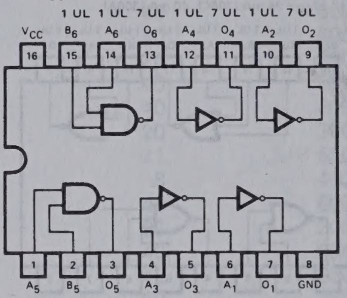
326 2, 2, 3, 3 INPUT NAND GATE
(PASSIVE PULL-UP)
I_{CC} = 28 mA (326C), 40 mA (326A)


1 UL 1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
V_{CC} C_2 B_2 A_2 O_2 B_4 A_4 O_4
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_3 B_3 A_3 O_1 C_1 B_1 A_1 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL 1 UL

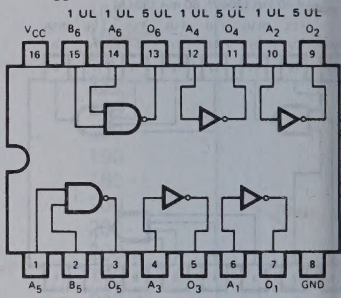
331 DUAL FIVE INPUT GATE EXPANDER
I_{CC} = 4.2 mA (331C), 5.2 mA (331A)


INPUTS
V_{CC} R_2 O_2
16 15 14 13 12 11 10 9
8.2K
8.2K
1 2 3 4 5 6 7 8
R_1 O_1 GND
INPUTS

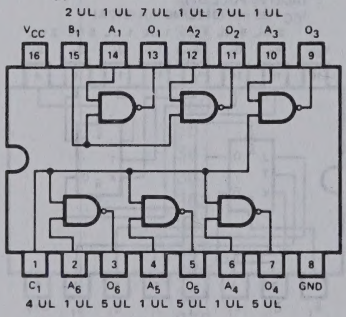
332 HEX INVERTER GATE
(OPEN COLLECTOR)
I_{CC} = 28 mA (332C), 42 mA (332A)


1 UL 1 UL 7 UL 1 UL 7 UL 1 UL 7 UL
V_{CC} B_6 A_6 O_6 A_4 O_4 A_2 O_2
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
A_5 B_5 O_5 A_3 O_3 A_1 O_1 GND
1 UL 1 UL 7 UL 1 UL 7 UL 1 UL 7 UL

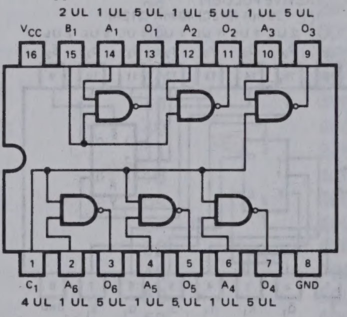
333 HEX INVERTER GATE
(PASSIVE PULL-UP)
I_{CC} = 42 mA (333C), 60 mA (333A)


1 UL 1 UL 5 UL 1 UL 5 UL 1 UL 5 UL
V_{CC} B_6 A_6 O_6 A_4 O_4 A_2 O_2
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
A_5 B_5 O_5 A_3 O_3 A_1 O_1 GND
1 UL 1 UL 5 UL 1 UL 5 UL 1 UL 5 UL

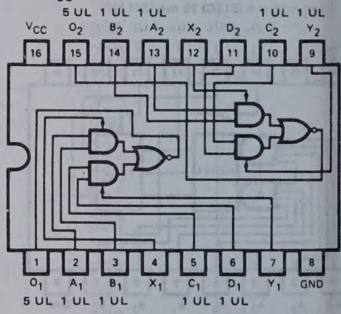
334 STROBED HEX INVERTER GATE
(OPEN-COLLECTOR)
I_{CC} = 28 mA (334C), 42 mA (334A)


2 UL 1 UL 7 UL 1 UL 7 UL 1 UL
V_{CC} B_1 A_1 O_1 A_2 O_2 A_3 O_3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
C_1 A_6 O_6 A_5 O_5 A_4 O_4 GND
4 UL 1 UL 5 UL 1 UL 5 UL 1 UL 5 UL

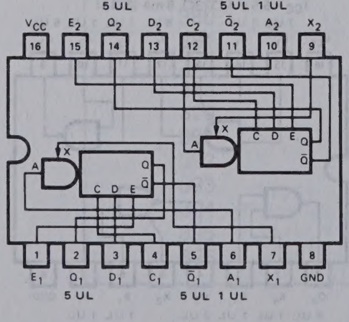
335 STROBED HEX INVERTER GATE
(PASSIVE PULL-UP)
I_{CC} = 42 mA (335C), 60 mA (335A)


2 UL 1 UL 5 UL 1 UL 5 UL 1 UL 5 UL
V_{CC} B_1 A_1 O_1 A_2 O_2 A_3 O_3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
C_1 A_6 O_6 A_5 O_5 A_4 O_4 GND
4 UL 1 UL 5 UL 1 UL 5 UL 1 UL 5 UL

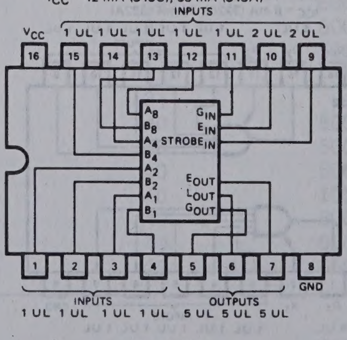
341 DUAL 2-WIDE, 2 INPUT AND-OR-INVERT GAT
(ACTIVE PULL-UP)
I_{CC} = 11 mA (341C), 15 mA (341A)


5 UL 1 UL 1 UL 1 UL 1 UL
V_{CC} O_2 B_2 A_2 X_2 D_2 C_2 Y_2
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_1 A_1 B_1 X_1 C_1 D_1 Y_1 GND
5 UL 1 UL 1 UL 1 UL 1 UL

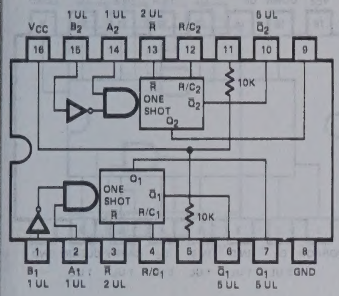
342 DUAL MONOSTABLE MULTIVIBRATOR
(ACTIVE PULL-UP)
I_{CC} = 17 mA (342C), 23 mA (342A)


5 UL 5 UL 1 UL
V_{CC} E_2 Q_2 D_2 C_2 $\bar{Q}_2$ A_2 X_2
16 15 14 13 12 11 10 9
X
A
C D E
Q
$\bar{Q}$
X
A
Q
$\bar{Q}$
C D E
1 2 3 4 5 6 7 8
E_1 Q_1 D_1 C_1 $\bar{Q}_1$ A_1 X_1 GND
5 UL 5 UL 1 UL

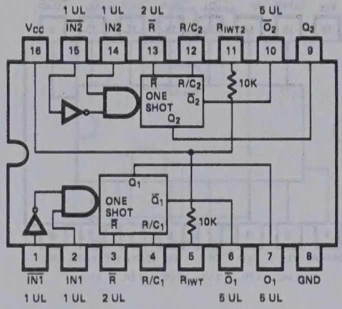
343 FOUR BIT COMPARATOR
(ACTIVE PULL-UP)
I_{CC} = 42 mA (343C), 56 mA (343A)


INPUTS
1 UL 1 UL 1 UL 1 UL 1 UL 2 UL 2 UL
V_{CC}
16 15 14 13 12 11 10 9
A_8
B_8
A_4
B_4
A_2
B_2
A_1
B_1
G_{IN}
E_{IN}
$STROBE_{IN}$
E_{OUT}
L_{OUT}
G_{OUT}
1 2 3 4 5 6 7 8
GND
INPUTS
OUTPUTS
1 UL 1 UL 1 UL 1 UL 5 UL 5 UL 5 UL

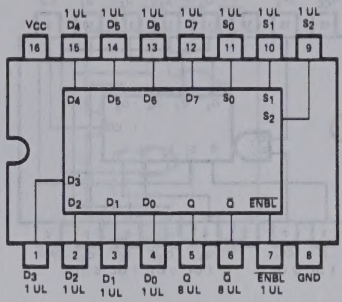
347 DUAL RETRIGGERABLE MONOSTABLE
(ACTIVE PULL-UP)


VCC
1 UL B2
1 UL A2
2 UL R̄
R/C2
5 UL Q̄2
16 15 14 13 12 11 10 9
R̄ R/C2
ONE SHOT
Q̄2
Q2
10K
Q1
ONE SHOT
Q̄1
R̄ R/C1
10K
1 2 3 4 5 6 7 8
B1 1 UL
A1 1 UL
R̄ 2 UL
R/C1
Q̄1 5 UL
Q1 5 UL
GND

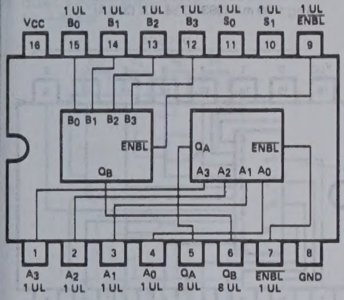
349 DUAL RETRIGGERABLE PULSE STRETCHER
(ACTIVE PULL-UP)
I_{CC} = 40 mA (349C), 50 mA (349A)


VCC
1 UL IN̄2
1 UL IN2
2 UL R̄
R/C2
RIWT2
5 UL Q̄2
Q2
16 15 14 13 12 11 10 9
R̄ R/C2
ONE SHOT
Q̄2
Q2
10K
Q1
ONE SHOT
Q̄1
R̄ R/C1
10K
1 2 3 4 5 6 7 8
IN̄1 1 UL
IN1 1 UL
R̄ 2 UL
R/C1
RIWT
Q̄1 5 UL
Q1 5 UL
GND

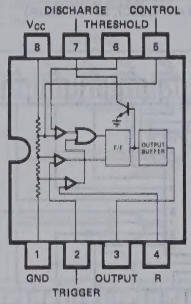
350 EIGHT BIT MULTIPLEXER
(ACTIVE PULL-UP)
I_{CC} = 33 mA (350C), 40 mA (350A)


VCC
1 UL D4
1 UL D5
1 UL D6
1 UL D7
1 UL S0
1 UL S1
1 UL S2
16 15 14 13 12 11 10 9
D4 D5 D6 D7 S0 S1 S2
D3
D2 D1 D0 Q Q̄ EN̄B̄L̄
1 2 3 4 5 6 7 8
D3 1 UL
D2 1 UL
D1 1 UL
D0 1 UL
Q 8 UL
Q̄ 8 UL
EN̄B̄L̄ 1 UL
GND

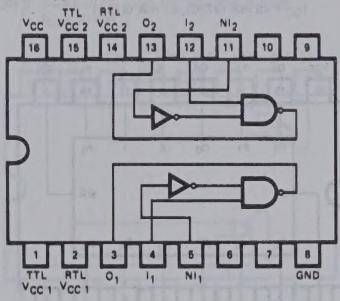
351 DUAL FOUR BIT MULTIPLEXER
(ACTIVE PULL-UP)
I_{CC} = 33 mA (351C), 40 mA (351A)


VCC
1 UL B0
1 UL B1
1 UL B2
1 UL B3
1 UL S0
1 UL S1
1 UL EN̄B̄L̄
16 15 14 13 12 11 10 9
B0 B1 B2 B3
EN̄B̄L̄
QB
QA
EN̄B̄L̄
A3 A2 A1 A0
1 2 3 4 5 6 7 8
A3 1 UL
A2 1 UL
A1 1 UL
A0 1 UL
QA 8 UL
QB 8 UL
EN̄B̄L̄ 1 UL
GND

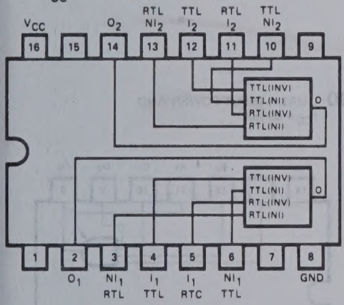
355 TIMER
I_{CC} = 20 mA


DISCHARGE
CONTROL
VCC
THRESHOLD
8 7 6 5
F/F
OUTPUT BUFFER
1 2 3 4
GND
OUTPUT
R
TRIGGER

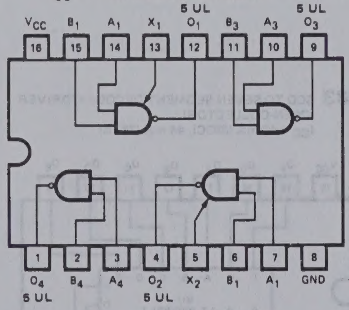
361 DUAL INPUT INTERFACE
(PASSIVE PULL-UP)
I_{CC} = 8 mA (361C), 11 mA (361A)


VCC
TTL VCC 2
RTL VCC 2
O2
I2
NI2
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
TTL VCC 1
RTL VCC 1
O1
I1
NI1
GND

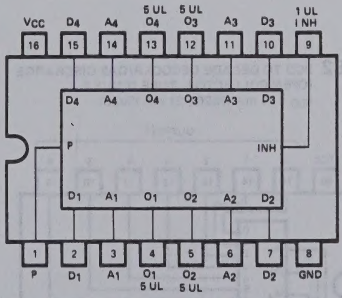
362 DUAL OUTPUT INTERFACE
(ACTIVE PULL-UP)
I_{CC} = 10 mA (362C), 13 mA (362A)


VCC
O2
RTL NI2
TTL I2
RTL I2
TTL NI2
16 15 14 13 12 11 10 9
TTL(INV)
TTL(NI)
RTL(INV)
RTL(NI)
O
TTL(INV)
TTL(NI)
RTL(INV)
RTL(NI)
O
1 2 3 4 5 6 7 8
O1
NI1 RTL
I1 TTL
I1 RTC
NI1 TTL
GND

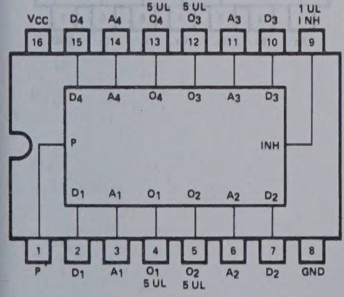
363 QUAD OUTPUT INTERFACE
(PASSIVE PULL-UP)
I_{CC} = 51 mA (363C), 64 mA (363A)


VCC
B1
A1
X1
5 UL O1
B3
A3
5 UL O3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O4 5 UL
B4
A4
O2 5 UL
X2
B1
A1
GND

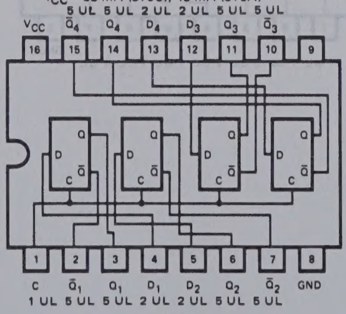
367 QUAD SCHMITT TRIGGER
(ACTIVE PULL-UP)
I_{CC} = 36 mA (367C), 54 mA (367A)


VCC
D4
A4
5 UL O4
5 UL O3
A3
D3
1 UL INH
16 15 14 13 12 11 10 9
D4 A4 O4 O3 A3 D3
P
INH
D1 A1 O1 O2 A2 D2
1 2 3 4 5 6 7 8
P
D1
A1
O1 5 UL
O2 5 UL
A2
D2
GND

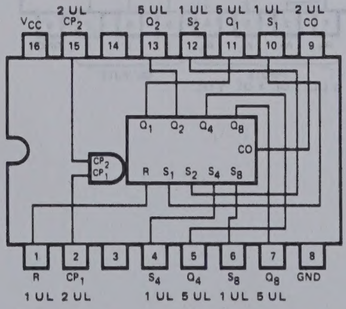
368 QUAD SCHMITT TRIGGER
(OPEN COLLECTOR)
I_{CC} = 33 mA (368C), 50 mA (368A)


VCC
D4
A4
5 UL O4
5 UL O3
A3
D3
1 UL INH
16 15 14 13 12 11 10 9
D4 A4 O4 O3 A3 D3
P
INH
D1 A1 O1 O2 A2 D2
1 2 3 4 5 6 7 8
P
D1
A1
O1 5 UL
O2 5 UL
A2
D2
GND

370 QUAD D FLIP-FLOP
(PASSIVE PULL-UP)
I_{CC} = 38 mA (370C), 48 mA (370A)

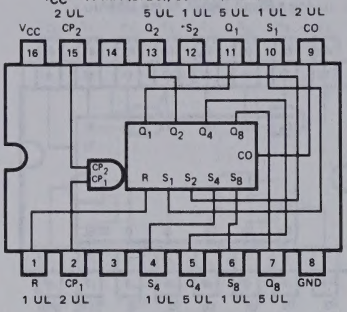

VCC
5 UL Q̄4
5 UL Q4
2 UL D4
2 UL D3
5 UL Q3
5 UL Q̄3
16 15 14 13 12 11 10 9
D Q C Q̄
D Q C Q̄
D Q C Q̄
D Q C Q̄
1 2 3 4 5 6 7 8
C 1 UL
Q̄1 5 UL
Q1 5 UL
D1 2 UL
D2 2 UL
Q2 5 UL
Q̄2 5 UL
GND

371 DECADE COUNTER
(PASSIVE PULL-UP)
I_{CC} = 41 mA (371C), 53 mA (371A)


VCC
2 UL CP2
5 UL Q2
1 UL S2
5 UL Q1
1 UL S1
2 UL CO
16 15 14 13 12 11 10 9
Q1 Q2 Q4 Q8
CO
CP2
CP1
R S1 S2 S4 S8
1 2 3 4 5 6 7 8
R 1 UL
CP1 2 UL
S4 1 UL
Q4 5 UL
S8 1 UL
Q8 5 UL
GND

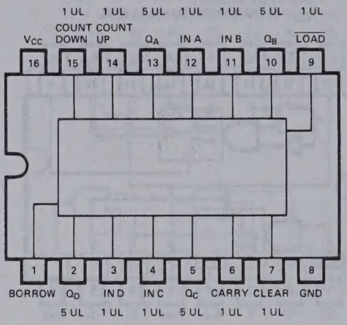
372 HEXADECIMAL COUNTER (PASSIVE PULL-UP)

I_{CC} = 41 mA (372C), 53 mA (372A)


2 UL
5 UL 1 UL 5 UL 1 UL 2 UL
VCC CP2 Q2 S2 Q1 S1 CO
16 15 14 13 12 11 10 9
Q1 Q2 Q4 Q8
CO
CP2 CP1
R S1 S2 S4 S8
1 2 3 4 5 6 7 8
R CP1 S4 Q4 S8 Q8 GND
1 UL 2 UL 1 UL 5 UL 1 UL 5 UL

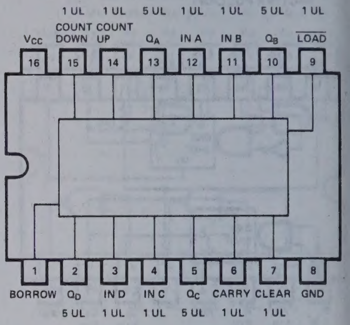
373 DECADE UP-DOWN COUNTER

I_{CC} = 50 mA (373C), 55 mA (373A)


1 UL 1 UL 5 UL 1 UL 1 UL 5 UL 1 UL
VCC COUNT DOWN COUNT UP QA IN A IN B QB LOAD
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
BORROW QD IN D IN C QC CARRY CLEAR GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL

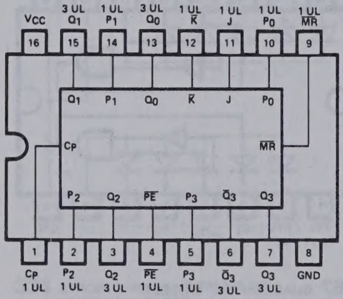
374 HEXADECIMAL UP-DOWN COUNTER

I_{CC} = 50 mA (374C), 55 mA (373A)


1 UL 1 UL 5 UL 1 UL 1 UL 5 UL 1 UL
VCC COUNT DOWN COUNT UP QA IN A IN B QB LOAD
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
BORROW QD IN D IN C QC CARRY CLEAR GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL

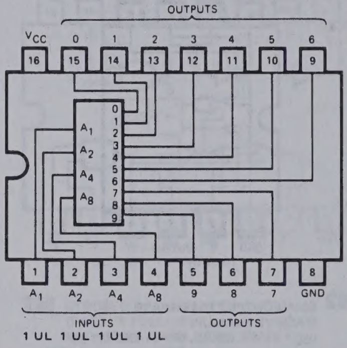
375 FOUR BIT SHIFT REGISTER (ACTIVE PULL-UP)

I_{CC} = 48 mA (375C), 64 mA (375A)


3 UL 1 UL 3 UL 1 UL 1 UL 1 UL 1 UL
VCC Q1 P1 Q0 K J P0 MR
16 15 14 13 12 11 10 9
Q1 P1 Q0 K J P0
CP MR
P2 Q2 PE P3 Q̄3 Q3
1 2 3 4 5 6 7 8
CP P2 Q2 PE P3 Q̄3 Q3 GND
1 UL 1 UL 3 UL 1 UL 1 UL 3 UL 3 UL

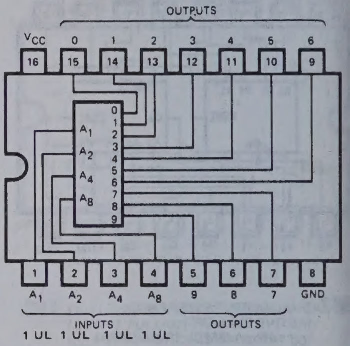
380 BCD TO DECADE DECODER/LAMP DRIVER (OPEN-COLLECTOR)

I_{CC} = 30 mA (380C), 38 mA (380A)


OUTPUTS
VCC 0 1 2 3 4 5 6
16 15 14 13 12 11 10 9
A1 A2 A4 A8
0 1 2 3 4 5 6 7 8 9
1 2 3 4 5 6 7 8
A1 A2 A4 A8 9 8 7 GND
INPUTS
OUTPUTS
1 UL 1 UL 1 UL 1 UL

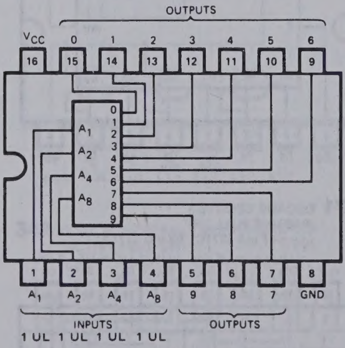
381 BCD TO DECADE DECODER/LOGIC DRIVER (OPEN COLLECTOR)

I_{CC} = 30 mA (383C), 38 mA (383A)


OUTPUTS
VCC 0 1 2 3 4 5 6
16 15 14 13 12 11 10 9
A1 A2 A4 A8
0 1 2 3 4 5 6 7 8 9
1 2 3 4 5 6 7 8
A1 A2 A4 A8 9 8 7 GND
INPUTS
OUTPUTS
1 UL 1 UL 1 UL 1 UL

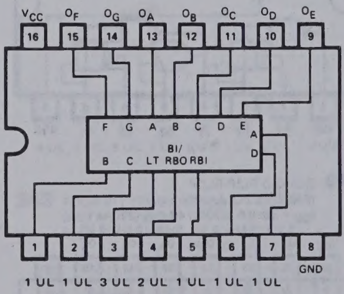
382 BCD TO DECADE DECODER/GAS DISCHARGE (OPEN-COLLECTOR) TUBE DRIVER

I_{CC} = 24 mA (382C), 31 mA (382C)


OUTPUTS
VCC 0 1 2 3 4 5 6
16 15 14 13 12 11 10 9
A1 A2 A4 A8
0 1 2 3 4 5 6 7 8 9
1 2 3 4 5 6 7 8
A1 A2 A4 A8 9 8 7 GND
INPUTS
OUTPUTS
1 UL 1 UL 1 UL 1 UL

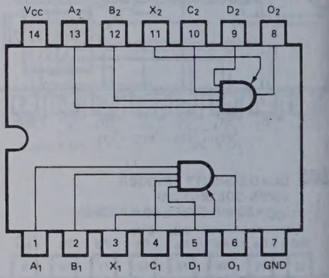
383 BCD TO SEVEN SEGMENT DECODER/DRIVER (OPEN-COLLECTOR)

I_{CC} = 40 mA (383C), 44 mA (383A)


VCC OF OG OA OB OC OD OE
16 15 14 13 12 11 10 9
F G A B C D E
A
BI/
D
B C LT RBO RBI
1 2 3 4 5 6 7 8
GND
1 UL 1 UL 3 UL 2 UL 1 UL 1 UL 1 UL

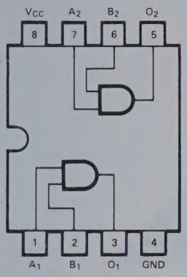
390 DUAL 4 INPUT POWER AND

I_{CC} = 40 mA


VCC A2 B2 X2 C2 D2 O2
14 13 12 11 10 9 8
1 2 3 4 5 6 7
A1 B1 X1 C1 D1 O1 GND

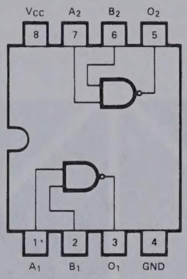
1 DUAL 2 INPUT POWER AND

$I_{CC} = 40$ mA


Vcc
A2
B2
O2
8
7
6
5
1
2
3
4
A1
B1
O1
GND

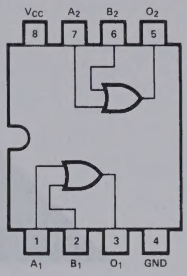
392 DUAL 2 INPUT POWER NAND

$I_{CC} = 40$ mA


Vcc
A2
B2
O2
8
7
6
5
1
2
3
4
A1
B1
O1
GND

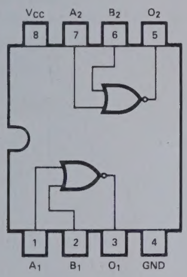
393 DUAL 2 INPUT POWER OR

$I_{CC} = 40$ mA


Vcc
A2
B2
O2
8
7
6
5
1
2
3
4
A1
B1
O1
GND

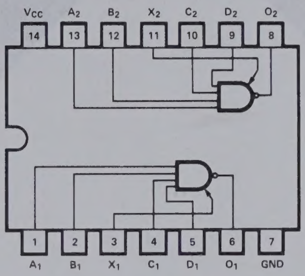
4 DUAL 2 INPUT POWER NOR

$I_{CC} = 40$ mA


Vcc
A2
B2
O2
8
7
6
5
1
2
3
4
A1
B1
O1
GND

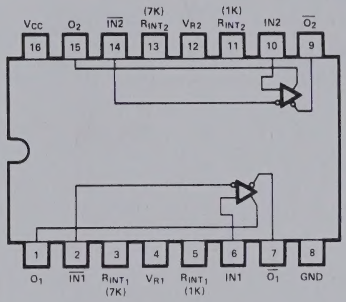
395 DUAL 4 INPUT POWER NAND

$I_{CC} = 40$ mA


Vcc
A2
B2
X2
C2
D2
O2
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
X1
C1
D1
O1
GND

396 DUAL DIFF. LINE DRIVER/RECEIVER

$I_{CC} = 25$ mA


Vcc
O2
IN2
(7K) RINT2
VR2
(1K) RINT2
IN2
O2
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
O1
IN1
RINT1 (7K)
VR1
RINT1 (1K)
IN1
O1
GND

Notes

SECTION 15

Application Notes

Section 15

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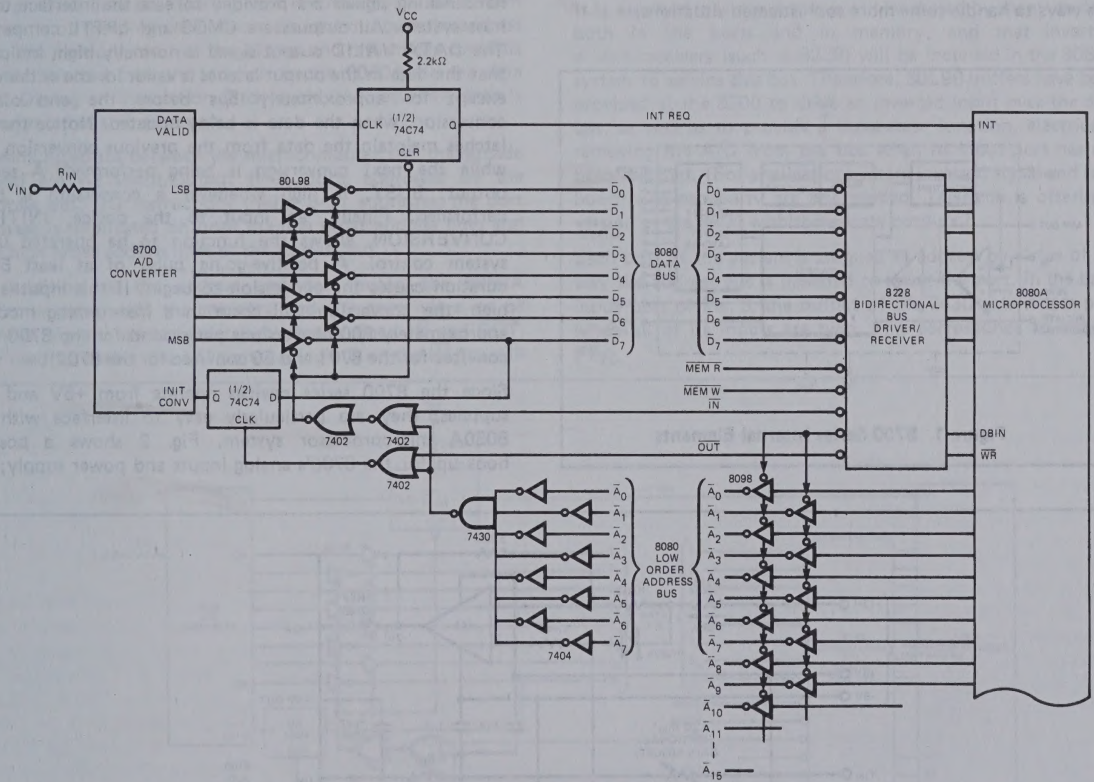
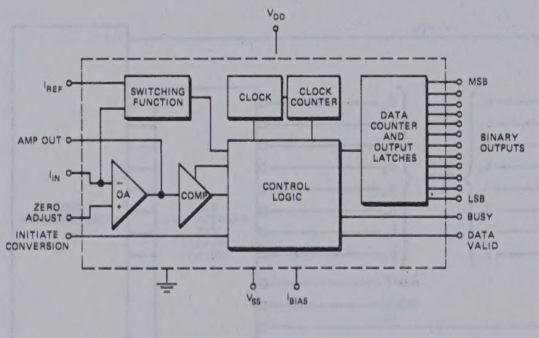
Application Note 8
Interfacing the TSC8700 A/D Converter with the 8080 μP System
By Dave Guzeman


V_CC
2.2kΩ
D
(1/2) 74C74
CLK
Q
CLR
DATA VALID
INT REQ
INT
V_IN
R_IN
LSB
80L98
D̄0
D̄1
D̄2
D̄3
D̄4
D̄5
D̄6
D̄7
8700 A/D CONVERTER
MSB
8080 DATA BUS
8228 BIDIRECTIONAL BUS DRIVER/ RECEIVER
8080A MICROPROCESSOR
MEM R
MEM W
IN
OUT
DBIN
WR
INIT CONV
Q̄
(1/2) 74C74
D
CLK
7402
7402
7402
8098
7430
Ā0
Ā1
Ā2
Ā3
Ā4
Ā5
Ā6
Ā7
8080 LOW ORDER ADDRESS BUS
7404
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A15

INTERFACING THE 8700 A/D CONVERTER WITH THE 8080 μP SYSTEM

The growth of microcomputers has included an expansion into process monitoring and control systems, as well as other applications requiring interaction with "real world" physical variables. At the same time, advances in semiconductor technology have allowed complex data conversion functions (A/D, D/A, V/F, etc.) to be performed by small and inexpensive IC's. By integrating these monolithic converter circuits into his microcomputer system, the designer thus can retain the same low cost and small size advantages which make the microprocessor so attractive.

In particular, the popular Intel 8080A microprocessor and Teledyne Semiconductor's 8700 series analog-to-digital converters are well suited to such a combination. This paper describes the basic techniques for interfacing the two, as well as ways to handle some more sophisticated situations.



V_{DD}
I_{REF}
AMP OUT
I_{IN}
ZERO ADJUST
INITIATE CONVERSION
SWITCHING FUNCTION
CLOCK
CLOCK COUNTER
DATA COUNTER AND OUTPUT LATCHES
OA
COMP
CONTROL LOGIC
MSB
BINARY OUTPUTS
LSB
BUSY
DATA VALID
V_{SS}
I_{BIAS}

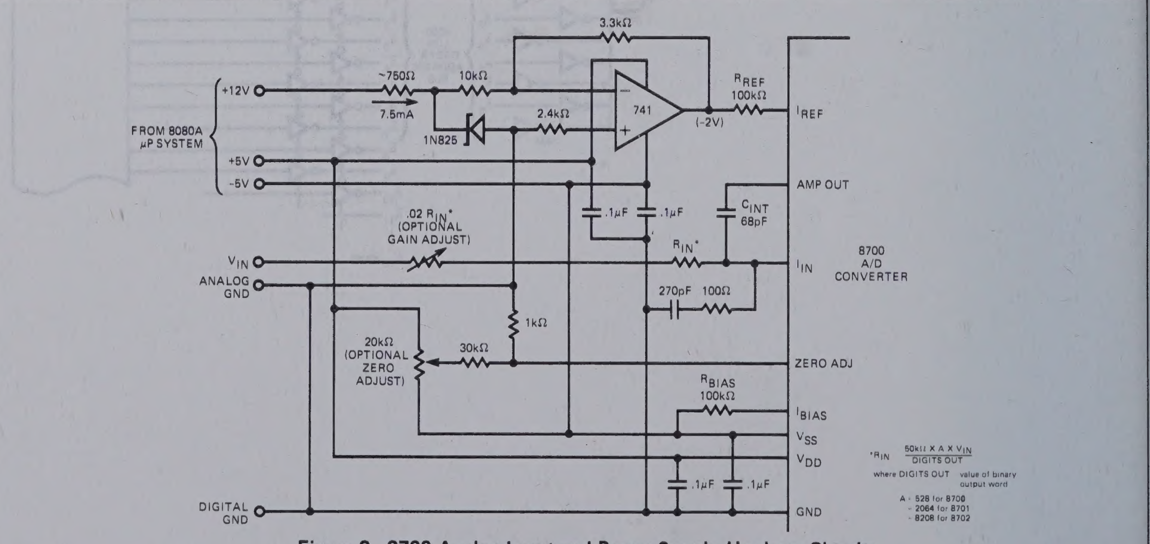
Figure 1. 8700 Series Internal Elements

THE 8700 A/D CONVERTER

Teledyne Semiconductor's 8700 series is a family of monolithic CMOS analog-to-digital converter IC's. All versions — the 8700 8-bit, 8701 10-bit and 8702 12-bit — are integrating converters which can accept an unlimited input voltage range (changed to a current input by external scaling resistor) and provide a latched parallel binary digital output. All are available in 24-pin ceramic DIP, and the 8-bit version is also offered in a low-cost 24-pin plastic package. As may be seen from the block diagram (Fig. 1), each device contains all of the essential elements for a complete A/D converter; only minimal support components are needed.

In addition to the 8, 10 or 12 buffered data output lines, three handshaking signals are provided to ease the interface to the host system. All outputs are CMOS and LPTTL compatible. The DATA VALID output signal is normally high, indicating that the data in the output latches is valid, for the entire cycle except for approximately 5μs before the end of the conversion, when the data is being updated. Notice that the latches maintain the data from the previous conversion even while the next conversion is being performed. A second output, BUSY, is high whenever a conversion is being performed. Finally, an input to the device, INITIATE CONVERSION, allows the function to be operated under system control. A positive-going pulse of at least 500ns duration causes the conversion to begin. If this input is tied high, the conversion will occur in a free-running mode at approximately 800 conversions per second for the 8700 (200 conv/sec for the 8701 and 50 conv/sec for the 8702).

Since the 8700 series devices operate from +5V and -5V supplies, they are particularly easy to interface with the 8080A microprocessor system. Fig. 2 shows a possible hook-up for the 8700's analog inputs and power supply; also



FROM 8080A μP SYSTEM
+12V
+5V
-5V
~750Ω
7.5mA
10kΩ
3.3kΩ
2.4kΩ
1N825
741
(-2V)
R_{REF} 100kΩ
I_{REF}
AMP OUT
.1μF
.1μF
C_{INT} 68pF
.02 R_{IN}* (OPTIONAL GAIN ADJUST)
V_{IN}
ANALOG GND
R_{IN}*
I_{IN}
8700 A/D CONVERTER
270pF
100Ω
1kΩ
20kΩ (OPTIONAL ZERO ADJUST)
30kΩ
ZERO ADJ
R_{BIAS} 100kΩ
I_{BIAS}
V_{SS}
V_{DD}
.1μF
.1μF
DIGITAL GND
GND

*R_{IN} $\frac{50k\Omega \times A \times V_{IN}}{\text{DIGITS OUT}}$

where DIGITS OUT value of binary output word

A = 528 for 8700
= 2064 for 8701
= 8208 for 8702

Figure 2. 8700 Analog Input and Power Supply Hook-up Circuits, Including V_{REF} Derived from 8080A System

incorporated is a circuit to supply the necessary negative reference, using a temperature-compensated zener diode and an inverting op amp. Note that the ±5V supplies needed for the 8700, as well as the additional +12V used in the reference circuit, are all available from the 8080A system.

In order to simplify the hardware and software for illustrative purposes, this paper concentrates on interfacing the 8-bit 8700 converter and the 8-bit 8080A microprocessor system. The same principles apply to inter-connecting the 8080A with the higher-resolution 8701 and 8702 A/D converters.

THE 8080A MICROPROCESSOR

The 8080A, an 8-bit microprocessor, communicates within the microcomputer system over two buses, a 16-bit address bus and an 8-bit data bus. During each machine cycle the current contents of the program counter are sent out over the address bus; the memory receives the address and returns the contents of the selected memory location to the 8080A via the data bus. During an instruction fetch cycle, the returning data is interpreted as an instruction.

Communications between the microcomputer and the outside world are via Input/Output (I/O) ports addressed by the address bus. I/O instructions utilize 8-bit addresses; the port address is duplicated on both the low order address lines and the high order address lines of the address bus.

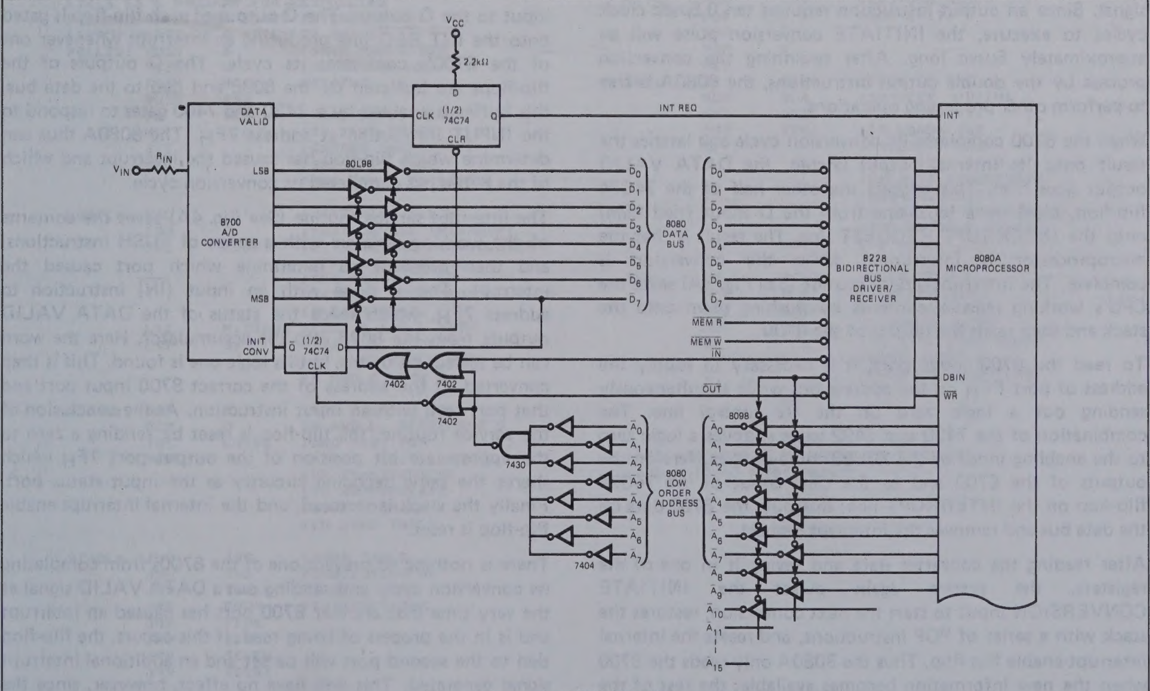
In addition to the address and data buses, the 8080A communicates with the memory and I/O ports via a set of control signals. In particular two control lines, $\overline{\text{IN}}$ and $\overline{\text{OUT}}$, are used to enable the I/O ports. A logic 0 on the $\overline{\text{IN}}$ line will enable the Input port that corresponds to the address on the address bus at that time. The $\overline{\text{OUT}}$ line functions in a similar fashion.

THE BASIC 8700 I/O PORT

A basic approach to interfacing the 8080A and the 8700 8-bit A/D converter is shown in Fig. 3. The conversion is started on command of the 8080A, using the INITIATE CONVERSION input of the 8700. When the conversion is complete, the DATA VALID output of the A/D requests an interrupt; the interrupt service routine transfers the current data from the working registers to the stack memory, and the A/D input port is read. A control signal then is sent to the INITIATE CONVERSION input to restart the conversion, and the main program activity is resumed.

It is assumed that the data bus will be shared by many devices, both in the ports and in memory, and that inverting drivers/receivers (such as 8228) will be included in the 8080A system to service this bus. Therefore, 80L98 buffers have been provided at the 8700 to drive an inverted input over the data bus, as well as to provide a three-state function, electrically removing the A/D from the bus when its input port has not been selected. (For applications where inverted signal and high bus-driving capability are not needed, Teledyne is offering a version of the 8700 with three-state outputs.)

Each port of the system is assigned an address by virtue of the way the address bus is decoded to select the port. In the basic input port of Fig. 3, the output of the 7430 gate is low only when all of its inputs are high. This corresponds to address FF_H.



V_{CC}
2.2kΩ
D
CLK (1/2) 74C74 Q
CLR
DATA VALID
INT REQ
INT
R_{IN}
V_{IN}
LSB
80L98
8700 A/D CONVERTER
MSB
INIT CONV
Q̄ (1/2) 74C74 D
CLK
7402
7402
7402
7430
7404
$\bar{D}_0$ $\bar{D}_1$ $\bar{D}_2$ $\bar{D}_3$ $\bar{D}_4$ $\bar{D}_5$ $\bar{D}_6$ $\bar{D}_7$
8080 DATA BUS
8228 BIDIRECTIONAL BUS DRIVER/ RECEIVER
8080A MICROPROCESSOR
MEM R
MEM W
IN
OUT
DBIN
WR
8098
$\bar{A}_0$ $\bar{A}_1$ $\bar{A}_2$ $\bar{A}_3$ $\bar{A}_4$ $\bar{A}_5$ $\bar{A}_6$ $\bar{A}_7$
8080 LOW ORDER ADDRESS BUS
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8 A_9 A_{10} A_{11} A_{15}

Figure 3. Basic 8700/8080A Interface

```
;INITIATION
        MVI     A,80H   ;THE CONVERSION
        OUT     0FFH    ;IS INITIATED
        MVI     A,0     ;BY SENDING A
        OUT     0FFH    ;BRIEF PULSE
                        ;TO PORT FF
;INTERRUPT
        PUSH    B       ;THE PROCESSOR
        PUSH    D       ;REGISTERS AND
        PUSH    H       ;STATUS ARE SAVED
        PUSH    PSW     ;IN THE STACK, AND THE
        IN      0FFH    ;DATA IS READ AND
        MOV     B,A     ;STORED IN REG B.
        MVI     A,80H   ;THE CONVERSION IS
        OUT     0FFH    ;INITIATED AND
        MVI     A,0     ;THE DATA IS
        OUT     0FFH    ;PROCESSED.
        .
        .
        .
        .
        POP     PSW     ;WHEN COMPLETE,
        POP     H       ;THE REGISTERS
        POP     D       ;ARE RESTORED, THE
        POP     B       ;INTERRUPTS ENABLED
        RET             ;AND PROGRAM
                        ;CONTROL RETURNED
                        ;TO THE MAIN PROGRAM.
```

Figure 3A

To initiate a conversion in the A/D, an output port, also address FF_H, is used. By defining both the input and output ports as address FF_H, the same address decoder, the 7430, may be used for both functions. In this case the output of the 7430 and the $\overline{\text{OUT}}$ signal are gated by 7402 to clock half of a 74C74 flip-flop. The D input of the flip-flop is tied to the D_7 line of the data bus. The flip-flop is, in effect, a one-bit output port. Sending the data word 80_H to port FF_H with an output ($\overline{\text{OUT}}$) instruction will cause the flip-flop to be set, thus supplying an INITIATE CONVERSION signal to the 8700. A second output instruction, sending 00_H to the same port, will reset the flip-flop and remove the INITIATE CONVERSION signal. Since an output instruction requires ten 0.5μsec clock cycles to execute, the INITIATE conversion pulse will be approximately 5μsec long. After beginning the conversion process by the double output instructions, the 8080A is free to perform other processing operations.

When the 8700 completes its conversion cycle and latches the result onto its internal output latches. the DATA VALID output goes high. This triggers the other half of the 74C74 flip-flop, clocking a logic one from the D input (tied high) onto the INTERRUPT REQUEST line. The result is that the microprocessor is interrupted when the conversion is complete. The interrupt service routine (See Fig. 3A) saves the CPU's working register contents by pushing them onto the stack and then reads the output of the 8700.

To read the 8700 input port, it is necessary to supply the address of port FF_H on the address bus while simultaneously sending out a logic zero on the $\overline{\text{IN}}$ control line. The combination of the 7430 and 7402 gates supplies a logic zero to the enabling input of the 80L98 three-state buffers on the outputs of the 8700 and to the clear input of the 74C74 flip-flop on the INTERRUPT line; this puts the 8700 data on the data bus and removes the interrupt request.

After reading the converter data and saving it in one of the registers, the system again pulses the INITIATE CONVERSION input to start the next conversion, restores the stack with a series of POP instructions, and resets the internal interrupt-enable flip-flop. Thus the 8080A only reads the 8700 when the new information becomes available; the rest of the time is spent in processing activities.

HANDLING MULTIPLE A/D CONVERTERS

When multiple analog inputs are involved, conventional system designs have tended to use an analog multiplexer feeding a single high-speed A/D converter. With the increasing availability of low-cost converter IC's, the approach of using a separate A/D for each analog line becomes more attractive. Fig. 4 illustrates a system of eight 8700 converters all supplying data in parallel to an 8080A system.

The system illustrated in Fig. 4 contains many of the same elements as the basic input port of Fig. 3. As before, the data outputs of the 8700s are buffered with 80L98 three-state buffers to drive the bus and to allow them to be disconnected. The decoding circuitry is slightly more complex. The five high-order address lines form the inputs to a 7430 gate which is used to enable a 7442 BCD to decimal decoder. The 7442 performs the final decoding by selecting the appropriate 8700 whenever an INPUT instruction is executed to one of the output ports $F8_H$ to FF_H. Also, the 8700s have their INITIATE CONVERSION inputs tied high so the devices operate in the free-running mode.

The interrupt scheme in this system is far more versatile than that previously illustrated. The user may assign priorities to each of the input ports, so that if one port has already interrupted the system and is being serviced, only a higher priority port can interrupt it. Lower priority interrupts will be delayed until the first port has been serviced.

Each of the eight interrupt input ports is constructed of a 74L74 flip-flop with its D inputs wired high. Each flip-flop is clocked independently by lines from the appropriate 8700 DATA VALID output, transferring the logic one on the D input to the Q output. The $\overline{Q}$ output of each flip-flop is gated onto the $\overline{\text{INT}}$ $\overline{\text{REQ}}$ line producing an interrupt whenever one of the 8700's completes its cycle. The Q outputs of the flip-flops are buffered by the 8098 and tied to the data bus; this buffer is enabled by a 7430 and 7400 gates to respond to the INPUT instruction at address $7F_H$. The 8080A thus can determine which flip-flop has caused the interrupt and which of the 8700s has completed its conversion cycle.

The interrupt service routine (See Fig. 4A) saves the contents of the working registers with a series of PUSH instructions, and then proceeds to determine which port caused the interrupt. This is done with an input ($\overline{\text{IN}}$) instruction to address $7F_H$, which loads the status of the DATA VALID outputs from the 8098 into the accumulator. Here the word can be tested, bit by bit, until a logic one is found. This is then converted to the address of the correct 8700 input port and that port read with an input instruction. At the conclusion of the service routine, the flip-flop is reset by sending a zero to the appropriate bit position of the output port $7F_H$ which shares the same decoding circuitry as the input status port. Finally the stack is restored, and the internal interrupt enable flip-flop is reset.

There is nothing to prevent one of the 8700s from completing its conversion cycle and sending out a DATA VALID signal at the very time that another 8700 port has caused an interrupt and is in the process of being read. If this occurs, the flip-flop tied to the second port will be set and an additional interrupt signal generated. This will have no effect, however, since the

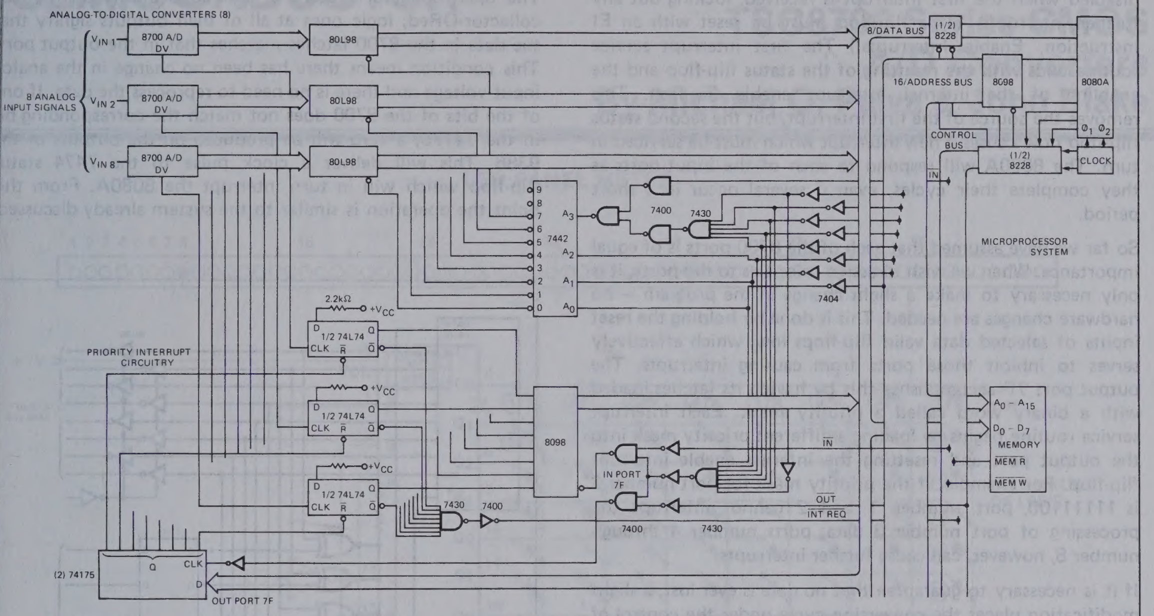

ANALOG-TO-DIGITAL CONVERTERS (8)
8 ANALOG INPUT SIGNALS
$V_{IN\ 1}$
$V_{IN\ 2}$
$V_{IN\ 8}$
8700 A/D DV
8700 A/D DV
8700 A/D DV
80L98
80L98
80L98
8/DATA BUS
(1/2) 8228
16/ADDRESS BUS
8098
8080A
CONTROL BUS
(1/2) 8228
$Ø_1$ $Ø_2$
CLOCK
IN
7442
A_3
A_2
A_1
A_0
7400
7430
7404
MICROPROCESSOR SYSTEM
2.2kΩ
+V_{CC}
1/2 74L74
D
CLK
Q
R
PRIORITY INTERRUPT CIRCUITRY
8098
IN PORT 7F
IN
OUT
INT REQ
A_0 - A_{15}
D_0 - D_7
MEMORY
MEM R
MEM W
(2) 74175
OUT PORT 7F

Figure 4. Eight Port A/D Converter System with Maskable Priority Interrupt

```
;THIS IS A PROGRAM FOR RESPONDING
;TO AND SERVICING EIGHT INTERRUPTING
;INPUT PORTS ON A PRIORITY BASIS.
POLLED: PUSH    B       ;SAVE PROCESSOR
        PUSH    D       ;REGISTERS AND
        PUSH    H       ;STATUS.
        PUSH    PSW
        IN      7FH     ;READ INPUT PORT
        MVI     D,0     ;TO FIND WHICH
        STC             ;CAUSED INTERRUPT.
        CMC             ;SET D TO ZERO
                        ;AND CARRY TO ZERO.

LOOP1:  RAL             ;DETERMINE WHICH
        INR     D       ;PORT CAUSED INTERRUPT
        JNC     LOOP1   ;BY ROTATING ACCUMULATOR
                        ;LEFT AND TESTING
                        ;FOR PRESENCE OF
                        ;CARRY.  INCREMENT
                        ;D EACH TIME.
        LXI     H,STABL ;LOAD H AND L WITH
        LXI     B,3     ;STARTING ADDRESS
                        ;OF JUMP TABLE AND
                        ;B AND C WITH 3.

LOOP2:  DAD     B       ;ADD B AND C TO
        DCR     D       ;H AND L, DECREMENT D
        JNZ     LOOP2   ;AND TEST FOR
        PCHL            ;ZERO.  EXIT LOOP
                        ;BY TRANSFERRING
                        ;TO APPROPRIATE
                        ;JUMP COMMAND
                        ;IN JUMP TABLE.

STABL:  JMP     ONE     ;JUMP TABLE
        JMP     TWO     ;CONSISTING OF
        JMP     THREE   ;3-BYTE JUMP
        JMP     FOUR    ;INSTRUCTIONS.
        JMP     FIVE
        JMP     SIX
        JMP     SEVEN
        JMP     EIGHT
```

```
RSTR:   POP     PSW     ;RESTORE REGISTERS
        POP     H       ;AND EXIT.
        POP     D
        POP     B
        RET
ONE:    IN      0F8H    ;THIS IS THE
        MOV     B,A     ;SERVICE ROUTINE
        MVI     0FEH    ;FOR PORT #1.
        OUT     7FH     ;IT LOADS THE
        EI              ;PRIORITY MASK
        .               ;WITH 1111 1110,
        .               ;ENABLES INTERRUPTS
        .               ;AND PROCESSES
        .               ;DATA.  AT CONCLUSION,
        .               ;THE PROGRAM JUMPS
        JMP     RSTR    ;TO RSTR.

TWO:    IN      0F9H    ;THIS IS THE
        MOV     B,A     ;ROUTINE FOR
        MVI     0FCH    ;PORT #2.  THE
        OUT     7FH     ;PRIORITY MASK
        EI              ;IS 1111 1100 WHICH
        .               ;KEEPS PORT #1
        .               ;FROM INTERRUPTING.
        .
        .
        .
        JMP     RSTR
;THE BALANCE OF THE SERVICE ROUTINES
;ARE OMITTED FOR BREVITY.
```

Figure 4A

8080A's internal-interrupt enable flip-flop is automatically disabled when the first interrupt is received, locking out any further interrupts. (This flip-flop must be reset with an EI instruction, Enable Interrupts.) The first interrupt service routine ends with the resetting of the status flip-flop and the enabling of the internal interrupt enable flip-flop. This removes the source of the first interrupt, but the second status flip-flop now causes a new interrupt which must be serviced in turn. The 8080A will respond to each of the input ports as they complete their cycles, even if several occur in a short period.

So far we have assumed that each of the 8700 ports is of equal importance. When we wish to assign priorities to the ports, it is only necessary to make a slight change in the program — no hardware changes are needed. This is done by holding the reset inputs of selected data valid flip-flops low, which effectively serves to inhibit those ports from causing interrupts. The output port 7F accomplishes this by having its latches loaded with a binary word called a priority mask. Each interrupt service routine begins by loading a different priority mask into the output port and resetting the internal enable interrupt flip-flop. For example, if the priority mask for port number 3 is 11111100, port number 1 and 2 cannot interrupt the processing of port number 3 data; ports number 4 through number 8, however, can cause further interrupts.

If it is necessary to guarantee that no data is ever lost, a slight modification places the conversion cycle under the control of the CPU. This is done by tying the reset inputs of the status flip-flops to the INITIATE CONVERSION inputs of the corresponding 8700's. The process of resetting the status flip-flop after the port has been read will cause the cycle to restart. This has the effect of holding the data on the output latches of the 8700's until it has been read.

INCREASING THE THROUGHPUT

If a great deal of data manipulation is to be done by the 8080A or a large number of 8700 input ports are to be connected to the bus, it is possible to feed data to the system faster than it can be processed. If the analog inputs on some of the ports are changing slowly, additional logic can be added to increase the effective capacity of the system. This involves adding a latching output port with the same address as the 8700 input port corresponding to it. (See Fig. 5) After the input port is read initially, an output instruction to the same address causes the data to be duplicated in the 74175 latches. The open collector feature of the 9386 allows them to be collector-ORed; logic ones at all of their outputs signify that the data in the 8700 latches matches that in the output port. This condition means there has been no change in the analog input voltage and there is no need to reprocess the data. If one of the bits of the 8700 does not match the corresponding bit in the 74175, a zero will be produced on the outputs of the 9386. This will deliver a clock pulse to the 7474 status flip-flop which will in turn interrupt the 8080A. From this point the operation is similar to the system already discussed.

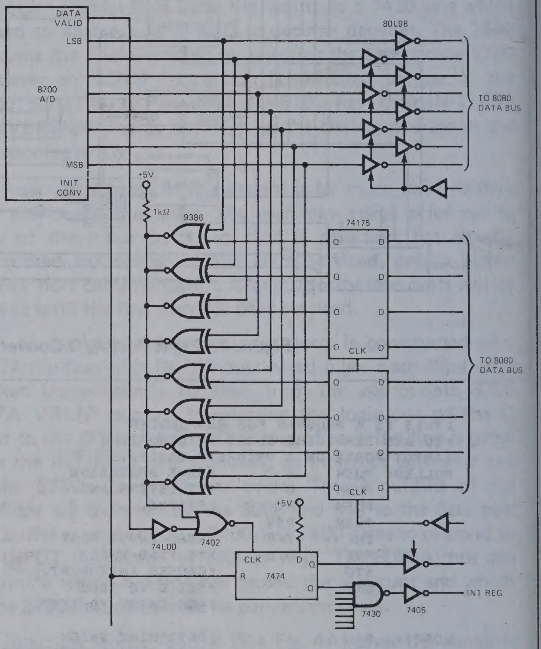
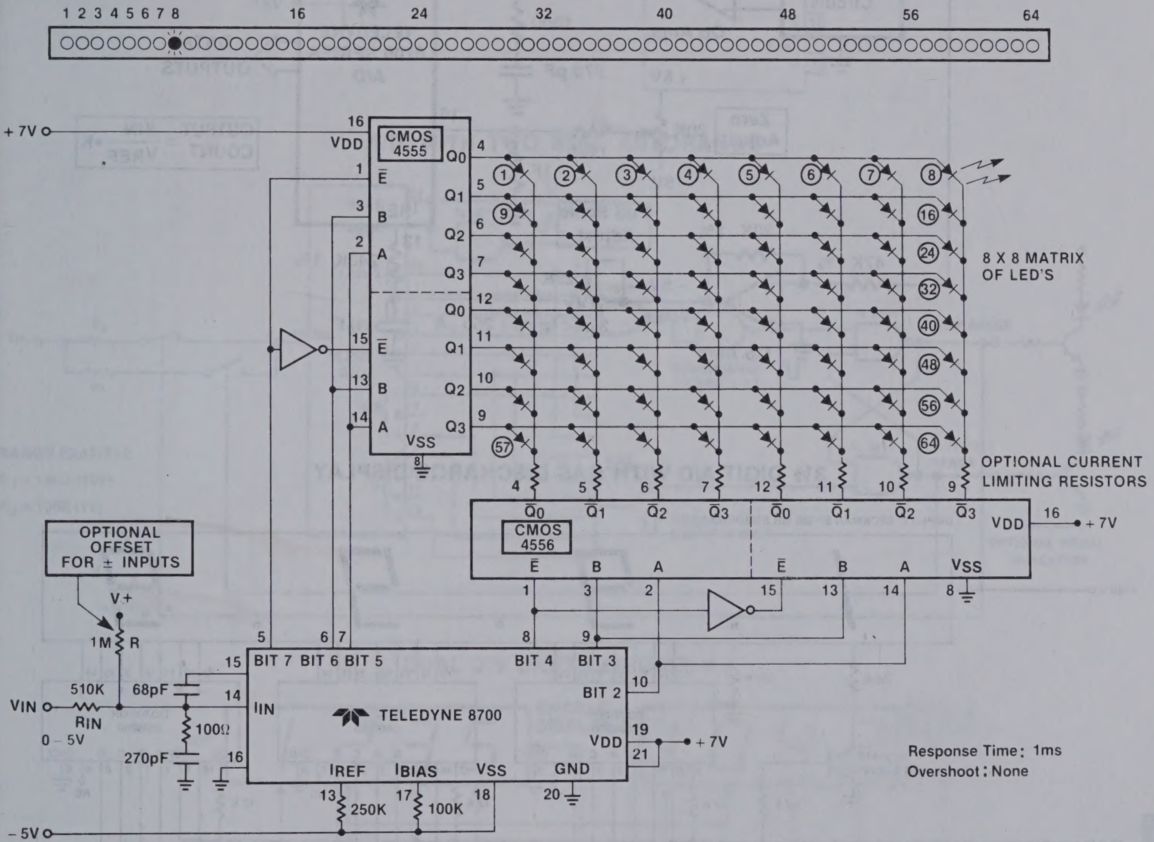


Figure 5. Significant Change Interrupt for 8700 Input Port

TELEDYNE SEMICONDUCTOR

Application Note 9
Applications of the TSC8700 Series CMOS A/D Converters
By Michael O. Paiva & John Blake

LED PANEL METER


1 2 3 4 5 6 7 8
16
24
32
40
48
56
64
+7V
VDD
16
CMOS 4555
1
Ē
3
B
2
A
15
Ē
13
B
14
A
VSS
8
Q0
Q1
Q2
Q3
Q0
Q1
Q2
Q3
4
5
6
7
12
11
10
9
① ② ③ ④ ⑤ ⑥ ⑦ ⑧
⑨ ⑯ ㉔ ㉜ ㊵ ㊽ (56) (57) (64)
8 X 8 MATRIX OF LED'S
OPTIONAL CURRENT LIMITING RESISTORS
4
5
6
7
12
11
10
9
Q̄0
Q̄1
Q̄2
Q̄3
Q̄0
Q̄1
Q̄2
Q̄3
CMOS 4556
Ē
B
A
Ē
B
A
VDD
16
+7V
VSS
1
3
2
15
13
14
8
OPTIONAL OFFSET FOR ± INPUTS
V+
1M
R
510K
RIN
VIN
0 – 5V
68pF
100Ω
270pF
15
14
16
5
6
7
8
9
BIT 7 BIT 6 BIT 5
BIT 4
BIT 3
BIT 2
10
IIN
TELEDYNE 8700
19
VDD
21
+7V
IREF
IBIAS
VSS
GND
13
250K
17
100K
18
20
-5V
Response Time: 1ms
Overshoot: None

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Ratiometric Applications
3½ Digit A/D With Gas Discharge Display
Overrange/Underrange Indicator
Autoranging
Dual 3½ Digit LED Display
Analog Peak Detector
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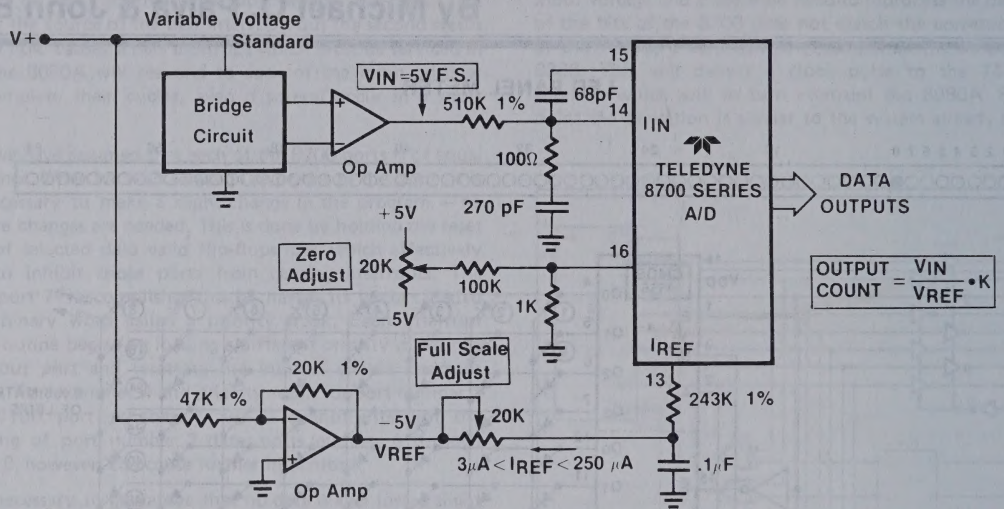
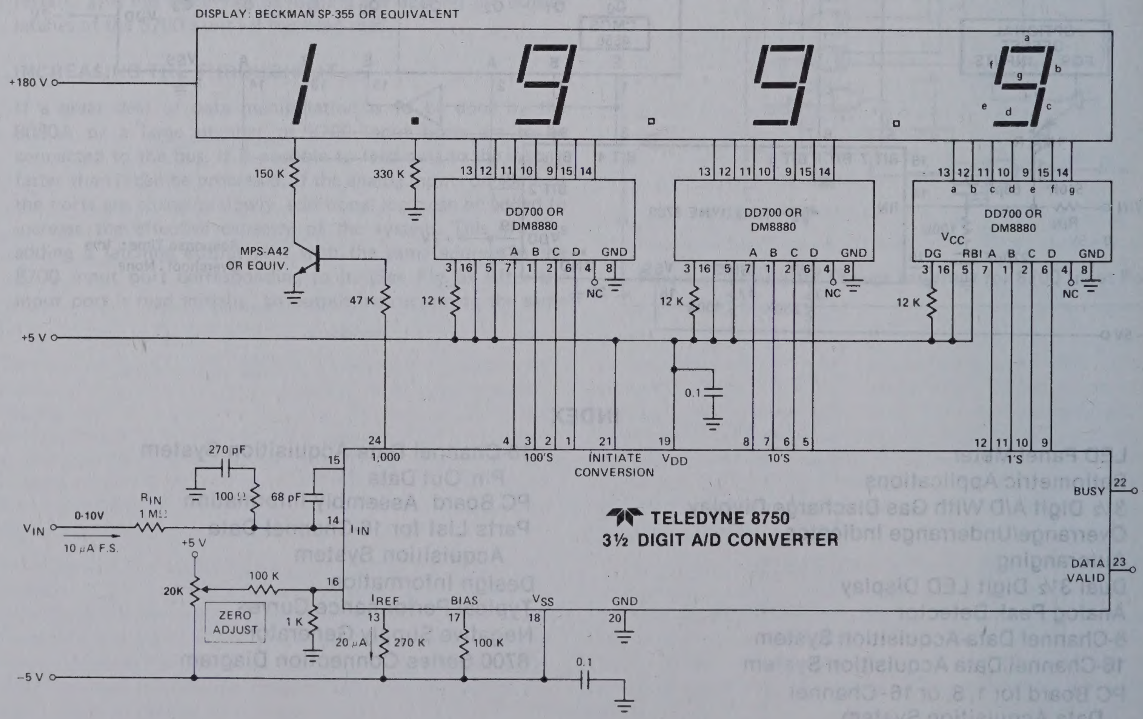
16-Channel Data Acquisition System
PC Board for 1, 8, or 16-Channel Data Acquisition System
16-Channel Data Acquisition System Pin Out Data
PC Board Assembly Information
Parts List for 16-Channel Data Acquisition System
Design Information
Typical Performance Curves
Negative Supply Generator
8700 Series Connection Diagram

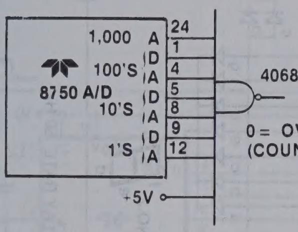
RATIOMETRIC APPLICATIONS


V+
Variable Voltage Standard
Bridge Circuit
Op Amp
VIN =5V F.S.
510K 1%
68pF
100Ω
270 pF
15
14
IIN
TELEDYNE 8700 SERIES A/D
DATA OUTPUTS
OUTPUT COUNT = VIN / VREF •K
+5V
Zero Adjust
20K
100K
−5V
16
1K
IREF
Full Scale Adjust
20K 1%
47K 1%
−5V
VREF
20K
Op Amp
3μA < IREF < 250 μA
13
243K 1%
.1μF

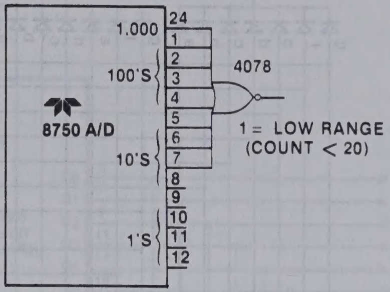
3½ DIGIT A/D WITH GAS DISCHARGE DISPLAY


DISPLAY: BECKMAN SP-355 OR EQUIVALENT
+180 V
150 K
330 K
MPS-A42 OR EQUIV.
47 K
+5 V
DD700 OR DM8880
13 12 11 10 9 15 14
A B C D GND
3 16 5 7 1 2 6 4 8
12 K
NC
VCC
DG RBI A B C D GND
a b c d e f g
0.1
24 1,000
4 3 2 1 100'S
21 INITIATE CONVERSION
19 VDD
8 7 6 5 10'S
12 11 10 9 1'S
BUSY 22
DATA VALID 23
TELEDYNE 8750 3½ DIGIT A/D CONVERTER
270 pF
15
100 Ω
68 pF
RIN 1 MΩ
VIN 0-10V 10 μA F.S.
14 IIN
+5 V
100 K
16
20K
ZERO ADJUST
1 K
IREF 13
20 μA
270 K
BIAS 17
100 K
VSS 18
GND 20
−5 V
0.1

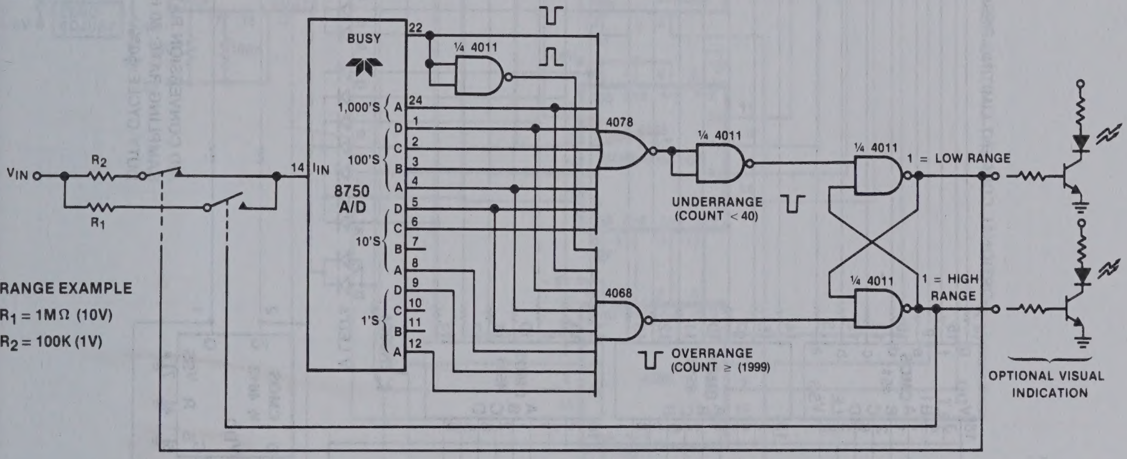
OVERRANGE INDICATOR


1,000
A
D
A
D
A
D
A
100'S
8750 A/D
10'S
1'S
24
1
4
5
8
9
12
4068
0 = OVERRANGE
(COUNT ≥ 1,999)
+5V

UNDERRANGE INDICATOR

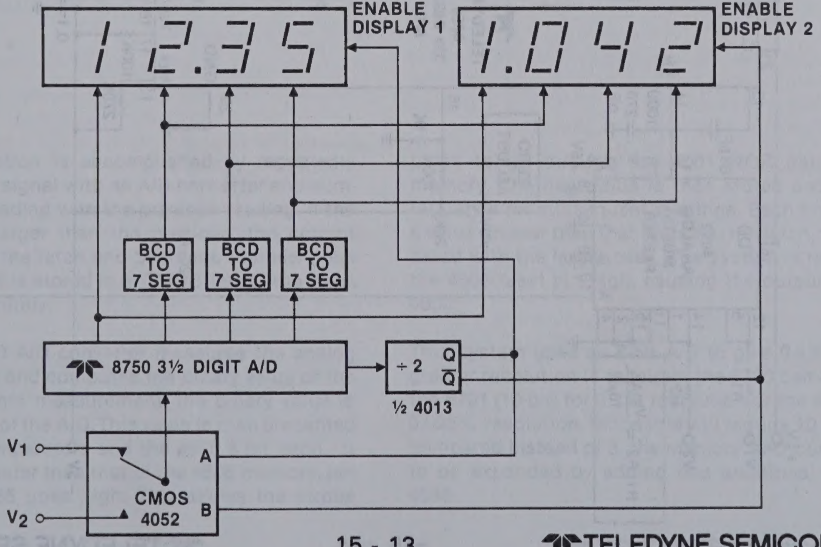

1,000
100'S
8750 A/D
10'S
1'S
24
1
2
3
4
5
6
7
8
9
10
11
12
4078
1 = LOW RANGE
(COUNT < 20)

A/D WITH TWO STEP AUTORANGE

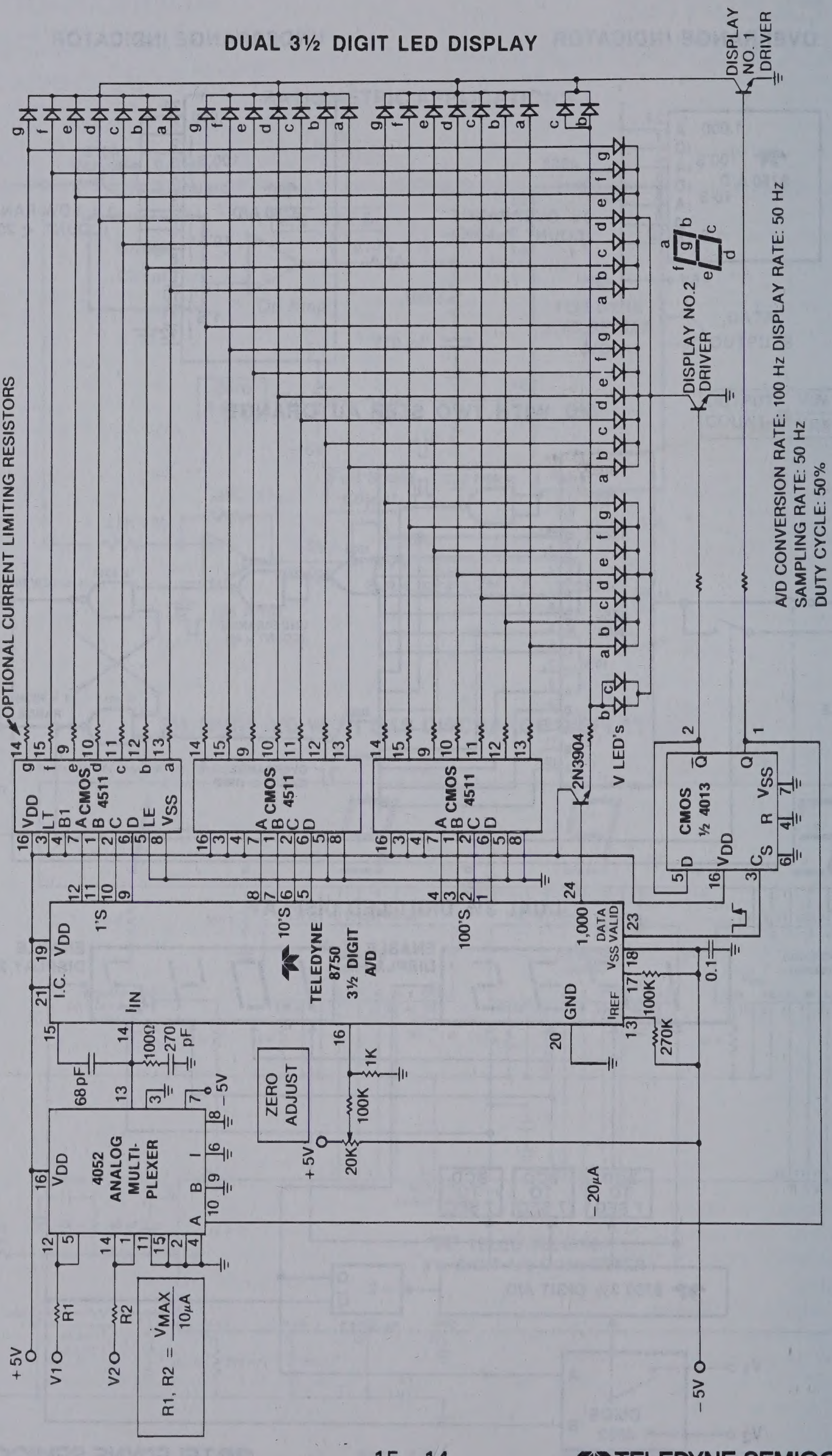

BUSY
22
¼ 4011
1,000'S
100'S
10'S
1'S
A
D
C
B
A
D
C
B
A
D
C
B
A
24
1
2
3
4
5
6
7
8
9
10
11
12
14
IIN
8750 A/D
VIN
R2
R1
4078
¼ 4011
UNDERRANGE
(COUNT < 40)
4068
OVERRANGE
(COUNT ≥ (1999)
¼ 4011
¼ 4011
1 = LOW RANGE
1 = HIGH RANGE
OPTIONAL VISUAL INDICATION

RANGE EXAMPLE
$R_1 = 1M\Omega$ (10V)
$R_2 = 100K$ (1V)

DUAL 3½ DIGIT LED DISPLAY


12.35
ENABLE DISPLAY 1
1.042
ENABLE DISPLAY 2
BCD TO 7 SEG
BCD TO 7 SEG
BCD TO 7 SEG
8750 3½ DIGIT A/D
÷ 2
Q
Q̄
½ 4013
V1
V2
A
B
CMOS 4052

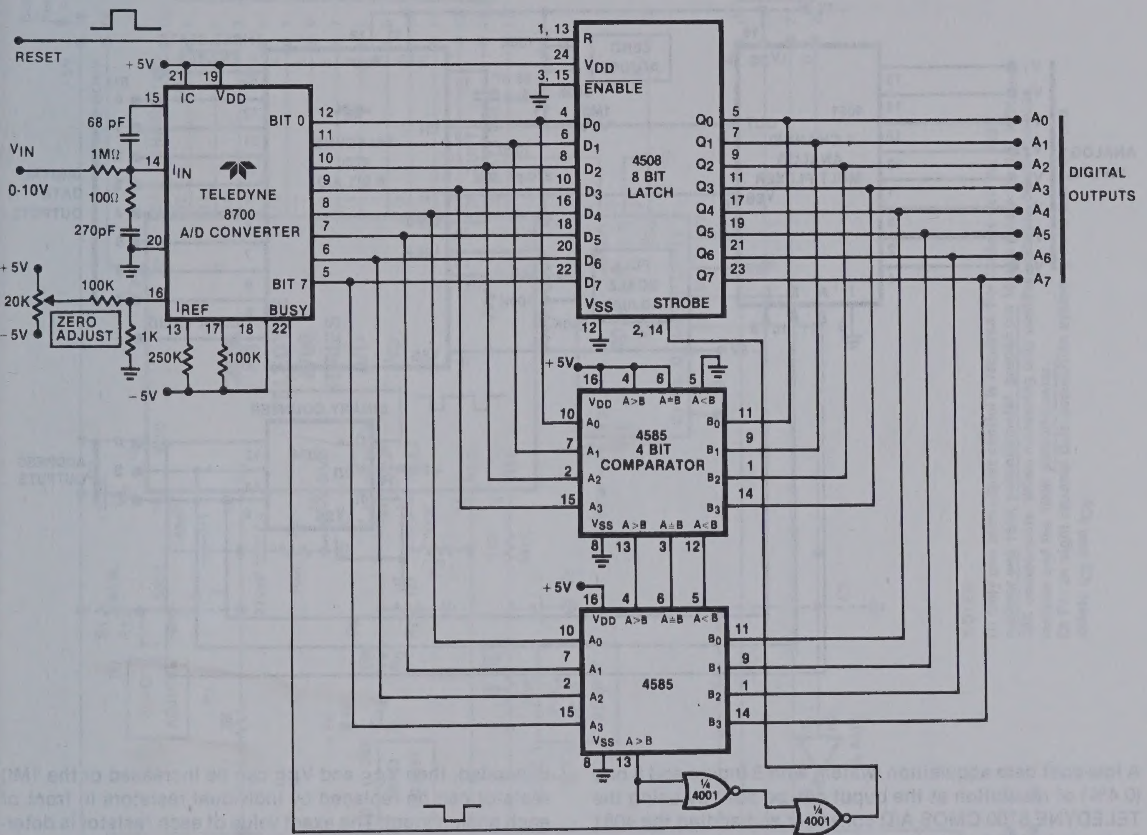
DUAL 3½ DIGIT LED DISPLAY


OPTIONAL CURRENT LIMITING RESISTORS
+5V
V1
V2
R1
R2
4052 ANALOG MULTI-PLEXER
VDD
A
B
I
68pF
100Ω
270 pF
−5V
ZERO ADJUST
+5V
20K
100K
1K
IIN
I.C.
VDD
TELEDYNE 8750 3½ DIGIT A/D
1'S
10'S
100'S
1,000
DATA VALID
VSS
GND
IREF
100K
270K
0.1
−20μA
CMOS 4511
VDD
LT
B1
A
B
C
D
LE
VSS
g
f
e
d
c
b
a
2N3904
V LED's
CMOS ½ 4013
D
VDD
CS
R
VSS
Q
Q̄
DISPLAY NO.2 DRIVER
DISPLAY NO.1 DRIVER
−5V

R1, R2 = $\frac{V_{MAX}}{10\mu A}$

A/D CONVERSION RATE: 100 Hz DISPLAY RATE: 50 Hz
SAMPLING RATE: 50 Hz
DUTY CYCLE: 50%

ANALOG PEAK DETECTOR WITH DIGITAL HOLD

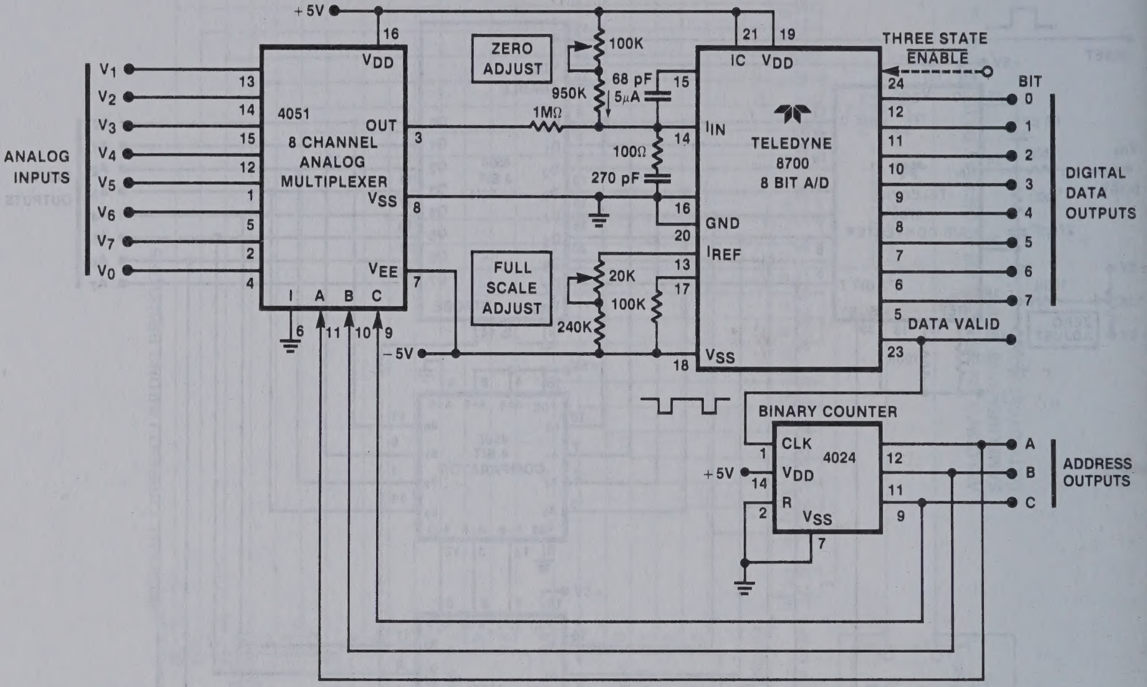

RESET
+5V
21
19
15
IC
VDD
68 pF
VIN
1MΩ
14
IIN
0-10V
100Ω
TELEDYNE
8700
A/D CONVERTER
270pF
20
+5V
20K
100K
16
IREF
-5V
ZERO ADJUST
1K
13
17
18
22
250K
100K
BUSY
-5V
BIT 0
BIT 7
12
11
10
9
8
7
6
5
1, 13
R
24
VDD
3, 15
ENABLE
4
D0
6
D1
8
D2
10
D3
16
D4
18
D5
20
D6
22
D7
VSS
12
4508
8 BIT
LATCH
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
STROBE
2, 14
5
7
9
11
17
19
21
23
A0
A1
A2
A3
A4
A5
A6
A7
DIGITAL OUTPUTS
+5V
16
4
6
5
VDD A>B A=B A<B
A0
A1
A2
A3
B0
B1
B2
B3
4585
4 BIT
COMPARATOR
VSS A>B A=B A<B
8
13
3
12
+5V
16
4
6
5
VDD A>B A=B A<B
A0
A1
A2
A3
B0
B1
B2
B3
4585
VSS A>B
8
13
¼ 4001
¼ 4001

Analog peak detection is accomplished by repeatedly measuring the input signal with an A/D converter and comparing the current reading with the previous reading. If the current reading is larger than the previous, the current reading is stored in the latch and becomes the new peak value. Since the peak is stored in a CMOS latch, the peak can be stored indefinitely.

The TELEDYNE 8700 A/D converter measures the analog input at a 1 KHz rate and computes the binary value of the input. After each 1ms measurement, the binary value is ched in the output of the A/D. This value is then presented to both the 4585 comparators and the 4508 8-bit latch. If the A/D's value is greater than that of the 4508 memory, pin 13 (A>B) of the 4585 goes high. This allows the strobe pulse to go through the 4001 NOR gate to the 4508 memory. The new value is then stored and becomes the reference for subsequent readings. Each time the A/D has a value greater than that stored in the latch, the latch is updated with the larger peak. The system is reset by pulsing the 4508 reset pin high, causing the output to go to 0000 0000.

This system uses an 8-bit A/D to give 0.4% resolution. If greater resolution is required, the 8700 can be replaced by the 8701 (10-bit) for 0.1% resolution or the 8702 (12-bit) for 0.025% resolution. Since this will require 10 or 12 bits to be compared instead of 8, the memory and comparator need to be expanded by adding one additional 4508 and one 4585.

8—CHANNEL DATA ACQUISITION SYSTEM


+5V
16
VDD
4051
8 CHANNEL
ANALOG
MULTIPLEXER
OUT
VSS
VEE
I A B C
V1
V2
V3
V4
V5
V6
V7
V0
ANALOG INPUTS
13
14
15
12
1
5
2
4
3
8
7
6
11
10
9
-5V
ZERO ADJUST
100K
950K
1MΩ
68 pF
5μA
100Ω
270 pF
FULL SCALE ADJUST
20K
100K
240K
21
19
IC VDD
15
IIN
14
16
GND
20
IREF
13
17
VSS
18
TELEDYNE
8700
8 BIT A/D
THREE STATE ENABLE
24
12
11
10
9
8
7
6
5
23
BIT
0
1
2
3
4
5
6
7
DIGITAL DATA OUTPUTS
DATA VALID
BINARY COUNTER
CLK
4024
VDD
R
VSS
1
14
2
7
12
11
9
+5V
A
B
C
ADDRESS OUTPUTS

A low-cost data acquisition system with 8 inputs and 8 bits (0.4%) of resolution at the ouput can be built by using the TELEDYNE 8700 CMOS A/D converter and adding the 4051 8 channel CMOS multiplexer and the 4024 binary counter.

Each input is measured for 1ms, then the digital value is placed in the output latch and remains for 1ms while the next input is being measured. After each 1ms measurement (conversion), the data valid line goes low for 5μs to indicate that the output latch is being updated. (The data must not be read during this period.) The negative edge of the data valid pulse is used to advance the binary counter by one. So after each conversion the 4051, via the 4024, automatically advances to the next input. The sampling sequence is therefore V_1, V_2,...V_7, V_0 and then back to V_1. The 8700 resets itself for 2.5μs after the data valid pulse so the analog switch has a total of 7.5μs to settle down. This is more than adequate to assure that the A/D will ignore any switching transients.

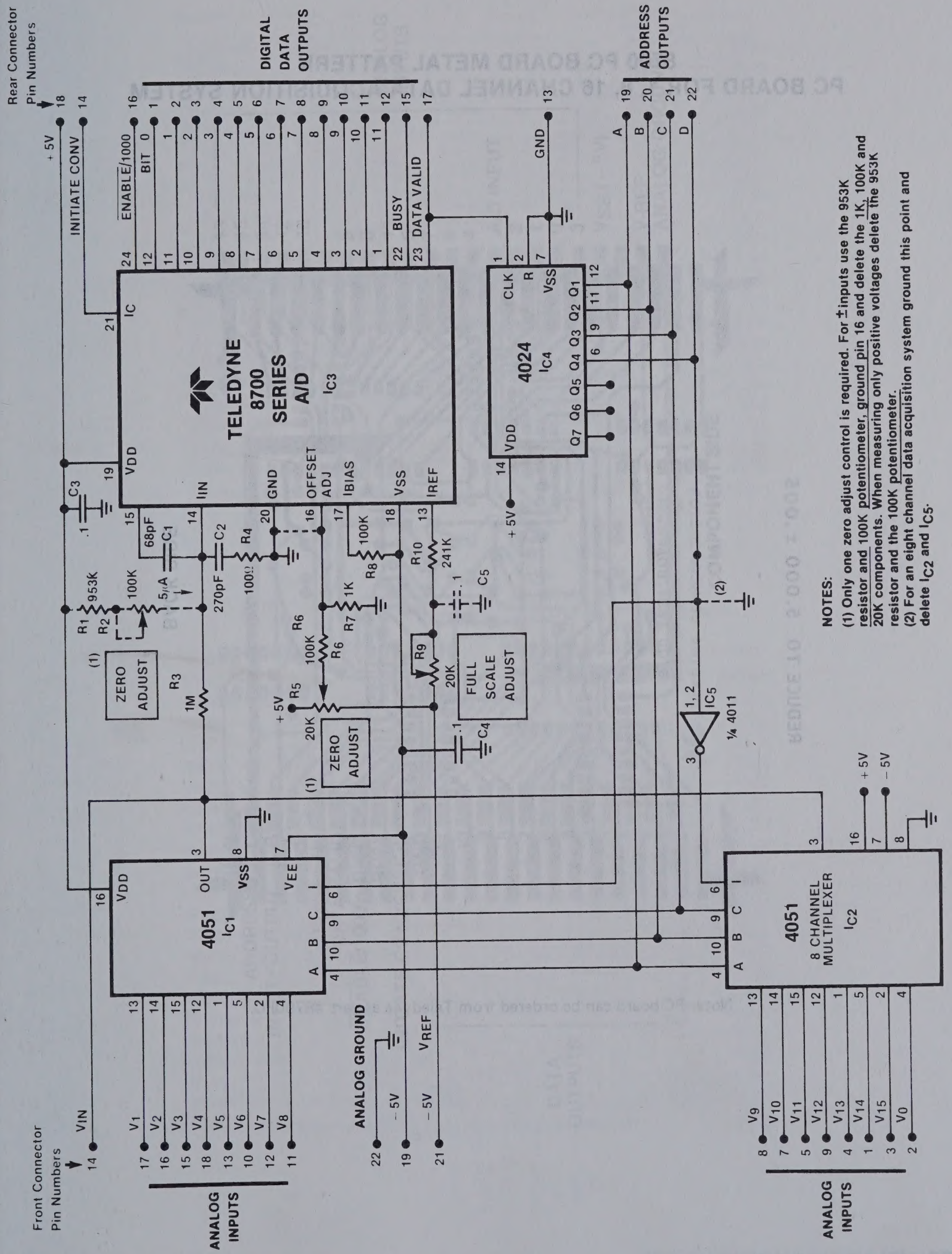
For the circuit shown, the input voltage range is limited by the 4051 to ± 5 volts (V_{DD}, V_{EE}). If more input voltage range is needed, then V_{SS} and V_{EE} can be increased or the 1MΩ resistor can be replaced by individual resistors in front of each analog input. The exact value of each resistor is determined by dividing the maximum input voltage by 5μA. ($R_{IN} = V_{max} \div 5\mu A$).

The 950K and 100K resistor are used to provide an offset current of 5μA, allowing the analog input voltage to be negative as well as positive. If the input voltage does not go negative, then these two resistors can be deleted.

By adding additional 4051's, the number of analog inputs can be increased in multiples of eight. The additional binary outputs of the 4024 are then simply decoded to control the inhibit (I) input of each 4051.

If three-state outputs are needed for interfacing to a data buss, then the 8700 can be replaced by the 8703. The 8703 is identical to the 8700 except that the digital data outputs are three-state outputs controlled by pin 24 ($\overline{\text{ENABLE}}$).

16—CHANNEL DATA ACQUISITION SYSTEM

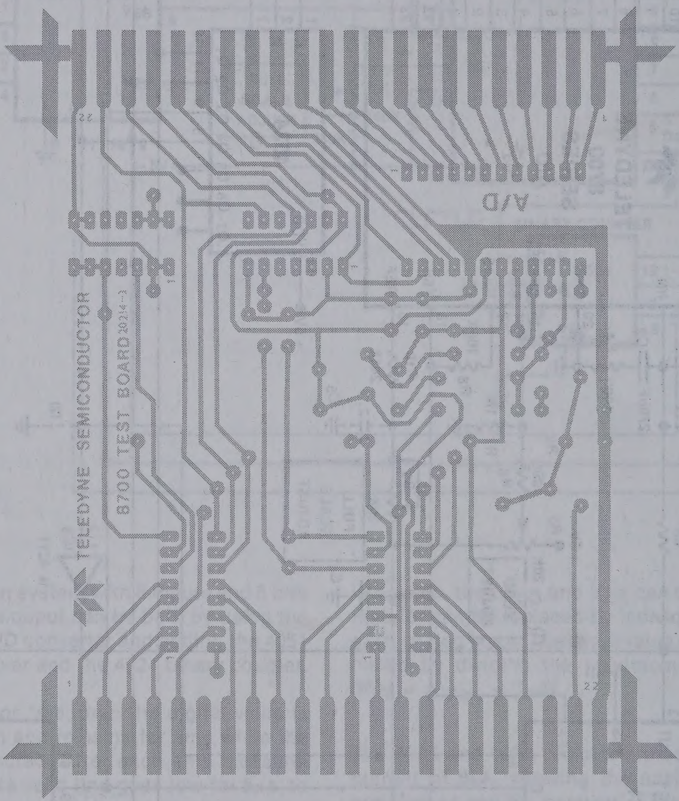

Rear Connector Pin Numbers
Front Connector Pin Numbers
+5V
INITIATE CONV
ENABLE/1000
BIT 0
BUSY
DATA VALID
GND
DIGITAL DATA OUTPUTS
ADDRESS OUTPUTS
A
B
C
D
TELEDYNE 8700 SERIES A/D
IC3
IC
VDD
IIN
GND
OFFSET ADJ
IBIAS
VSS
IREF
4024
IC4
CLK
R
VSS
VDD
Q1
Q2
Q3
Q4
Q5
Q6
Q7
4051
IC1
OUT
VSS
VEE
4051
8 CHANNEL MULTIPLEXER
IC2
IC5
1/4 4011
ZERO ADJUST
FULL SCALE ADJUST
C3 .1
C1 68pF
C2 270pF
C4 .1
C5 .1
R1 953K
R2 100K
R3 1M
R4 100Ω
R5 20K
R6 100K
R7 1K
R8 100K
R9 20K
R10 241K
5μA
VIN
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
V11
V12
V13
V14
V15
V0
ANALOG INPUTS
ANALOG GROUND
−5V
VREF
(1)
(2)

NOTES:

(1) Only one zero adjust control is required. For ± inputs use the 953K resistor and 100K potentiometer, ground pin 16 and delete the 1K, 100K and 20K components. When measuring only positive voltages delete the 953K resistor and the 100K potentiometer.

(2) For an eight channel data acquisition system ground this point and delete I_{C2} and I_{C5}.

8700 PC BOARD METAL PATTERN
PC BOARD FOR 1, 8, 16 CHANNEL DATA ACQUISITION SYSTEM

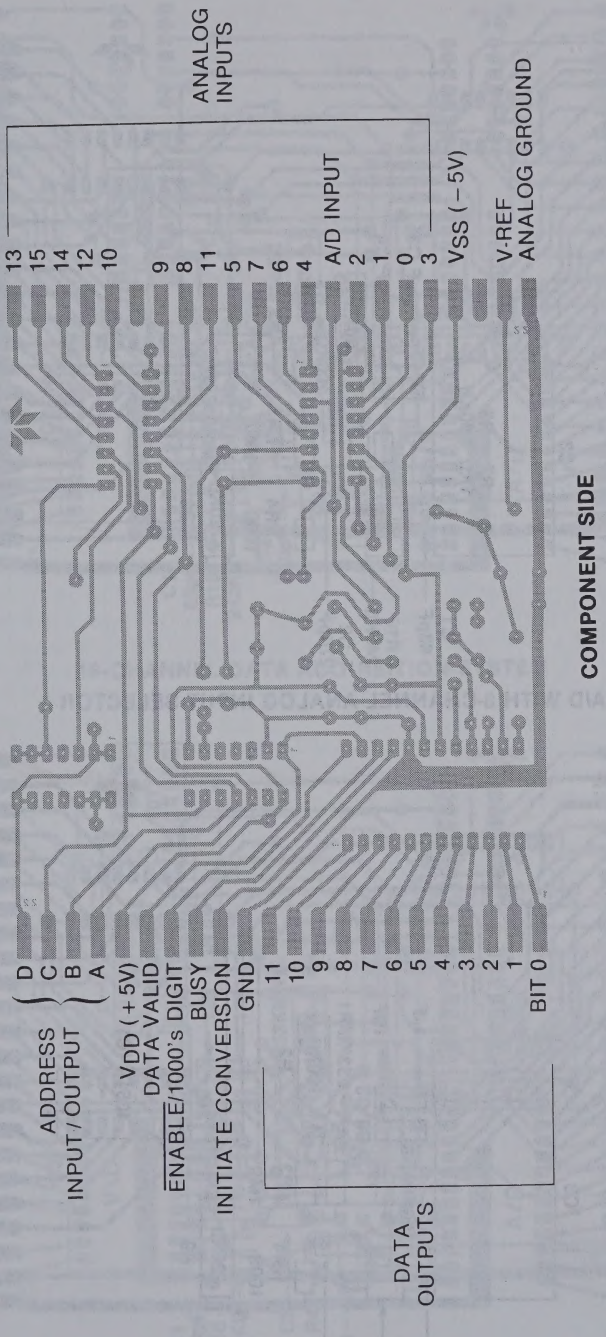

TELEDYNE SEMICONDUCTOR
8700 TEST BOARD 20214-1
A/D
1
22

REDUCE TO 5.000 ±.005

BACK SIDE

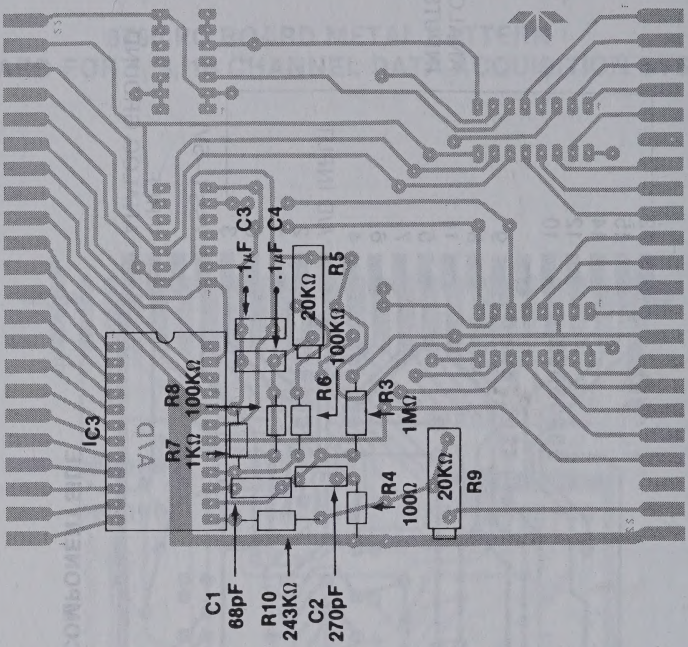
Note: PC board can be ordered from Teledyne as part #8700PC.

PIN-OUT DATA FOR 16 CHANNEL DATA ACQUISITION SYSTEM


ANALOG INPUTS
13
15
14
12
10
9
8
11
5
7
6
4
A/D INPUT
2
1
0
3
V_{SS} (−5V)
V-REF
ANALOG GROUND
ADDRESS INPUT/OUTPUT
D
C
B
A
V_{DD} (+5V)
DATA VALID
$\overline{\text{ENABLE}}$/1000's DIGIT
BUSY
INITIATE CONVERSION
GND
11
10
9
8
7
6
5
4
3
2
1
BIT 0
DATA OUTPUTS
COMPONENT SIDE

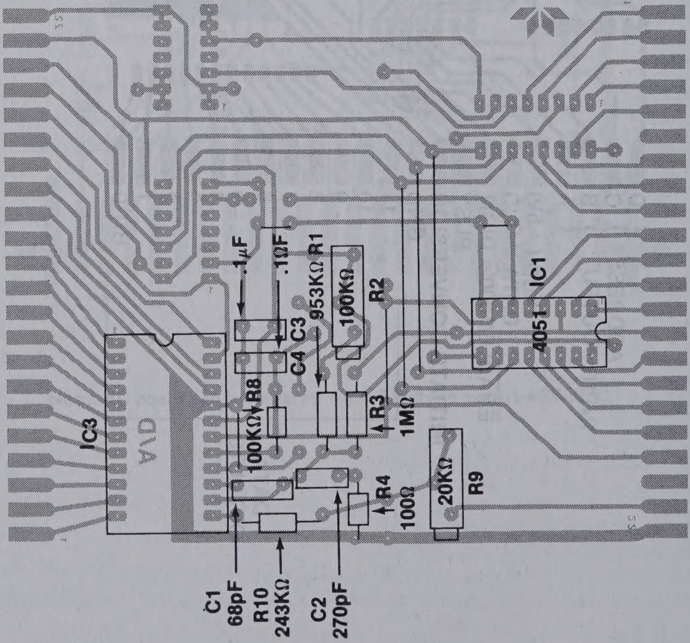
ASSEMBLY INFORMATION

STANDARD TEST CIRCUIT



IC3
A/D
R8
100KΩ
R7
1KΩ
.1μF C3
.1μF C4
20KΩ
R5
100KΩ
R6
R3
1MΩ
R4
100Ω
20KΩ
R9
C1
68pF
R10
243KΩ
C2
270pF

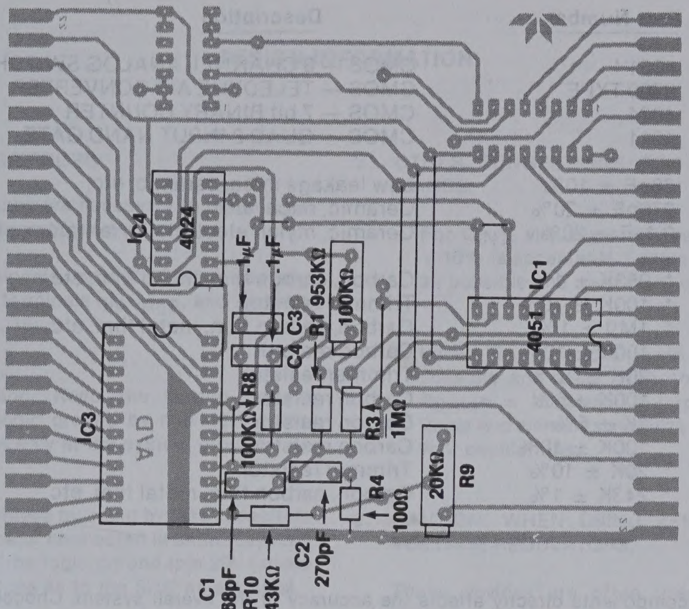
A/D WITH 8-CHANNEL ANALOG INPUT SELECTOR



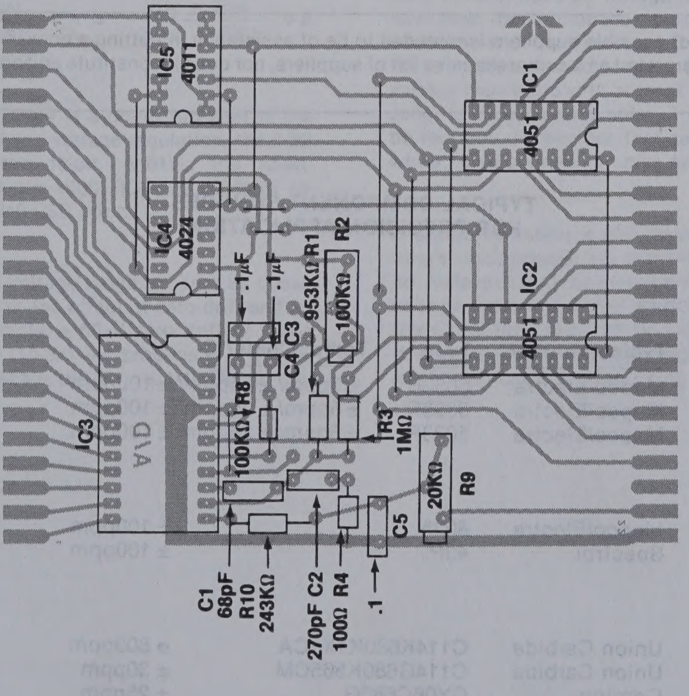
.1μF
.1μF
953KΩ R1
100KΩ
R2
C3
C4
R8
100KΩ
IC1
4051
IC3
A/D
R3
1MΩ
R4
100Ω
20KΩ
R9
C1
68pF
R10
243KΩ
C2
270pF

ASSEMBLY INFORMATION

8-CHANNEL DATA ACQUISITION SYSTEM


IC4
4024
.1µF
.1µF
C3
C4
R1 953KΩ
100KΩ
IC1
4051
R8
100KΩ
IC3
A/D
R3
1MΩ
R4
100Ω
20KΩ
R9
C1
68pF
R10
243KΩ
C2
270pF

16-CHANNEL DATA ACQUISITION SYSTEM


IC5
4011
IC1
4051
IC4
4024
.1µF
.1µF
C3
C4
953KΩ R1
R2
100KΩ
IC2
4051
R8
100KΩ
IC3
A/D
R3
1MΩ
20KΩ
R9
C5
C1
68pF
R10
243KΩ
270pF C2
100Ω R4
.1

PARTS LIST
16 CHANNEL DATA ACQUISITION SYSTEM

Ref #	Part Number	Description
IC1, IC2	4051	CMOS — 8 CHANNEL ANALOG SWITCH
IC3	8700 TYPE	CMOS — TELEDYNE A/D CONVERTER
IC4	4024	CMOS — 7 bit BINARY COUNTER
IC5	4011	CMOS — QUAD 2-INPUT NAND GATE
C1	68pF ± 10%	Low leakage mica, ceramic, etc.
C2	270pF ± 20%	Ceramic, mica, etc.
C3, C4, C5	0.1μF ± 20%	Ceramic, mylar, electrolytic, tantalum, etc.
R1	* 953K ± 1%	Carbon, carbon film, metal film, etc.
R2	* 100K ± 10%	Trimmer resistor
R3	* 1MΩ ± 1%	Carbon, carbon film, metal film, etc.
R4	100Ω ± 10%	Carbon resistor
R5	20K ± 10%	Trimmer resistor
R6	100K ± 5%	Carbon resistor
R7	1K ± 5%	Carbon resistor
R8	100K ± 10%	Carbon resistor
R9	* 20K ± 10%	Trimmer resistor
R10	* 243K ± 1%	Carbon, carbon film, metal film, etc.

★ The stability of these components directly affects the accuracy of the overall system. Choose components whose stability is consistent with the accuracy and temperature range required. For example, if an 8-bit A/D is used at a constant temperature, then 5% carbon resistors may be adequate since an 8-bit A/D's resolution is only 0.4%. However, if a 12-bit A/D (0.025% resolution) is to be used over the −55°C to + 125°C temperature range, then these components will be very critical and should have a stability of 5 to 15 ppm for fixed resistors and 25 to 50 ppm for variable resistors.

The following parts list of possible suppliers is intended to be of assistance in putting a converter design into production. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Teledyne Semiconductor.

TYPICAL COMPONENT SOURCES FOR PRECISION APPLICATION

A. Precision fixed resistors

Value	Tol.	Typical Source	Type	Temp. Coeff./°C
243K	± 1%	Mepco/Electra	5033R	± 5ppm/ ± 25ppm/ ± 100ppm
953K	± 1%	Mepco/Electra	5033R	± 5ppm/ ± 25ppm/ ± 100ppm
1MΩ	± 1%	Mepco/Electra	5033R	± 5ppm/ ± 25ppm/ ± 100ppm

B. Variable resistors

20K/100K	± 10%	Mepco/Electra	8035	± 100ppm
20K/100K	± 10%	Spectrol	43P	± 100ppm

C. Capacitors

68pF	± 10%	Union Carbide	C114K680K1X1CA	± 800ppm
68pF	± 10%	Union Carbide	C114G680K565CM	± 30ppm
68pF	± 5%	Corning	CY06C680G	± 25ppm

DESIGN INFORMATION

AVOID INTRODUCING ERRORS:

Proper design procedures are necessary to obtain best accuracy from 8700 series converters.

a. Do not route logic signals under the 8700 or near any of the three analog terminals I_{IN}, I_{REF}, and Zero Adjust (pins 13, 14, 15, 16).

b. Plan your grounding. Keep the analog ground isolated from the logic ground by making the two electrically common only at the system ground.

c. Filter the supply voltages by using bypass capacitors of value 0.1μF or greater connected in shunt between the supply line and the logic ground (pin 20). Locate the capacitors as close as to the 8700 as practical.

d. Provide a reference as stable as the conversion accuracy you expect. Remember:

$$\text{IGITAL COUNTS} = \frac{I_{IN}}{I_{REF}} \bullet A = \frac{V_{IN} \div R_{IN}}{V_{REF} \div R_{REF}} \bullet A$$

The conversion accuracy is a direct function of the V_{REF}. In terms of V_{REF} voltage regulation, the 8-bit requires ±.04%, the 10-bit, ±.01%, the 12-bit, ±.0025%, and the 3½ digit BCD, ±.005%,to introduce less than 1/10 LSB error.

e. Choose a full scale voltage range as large as possible; this will minimize the effect of zero drift and input noise. For example, a 50μV zero drift or noise voltage on the 8701 (10-bit) will produce a ± ½ LSB error at 500mV full scale, but only ± 1/40 LSB at 10V full scale.

2. OTHER SUGGESTIONS FOR IMPROVING PERFORMANCE:

a. For C_{INT}, virtually any type of non-polarized 68pF ±10% is acceptable. Locate as near to the converter as possible and away from noisy lines.

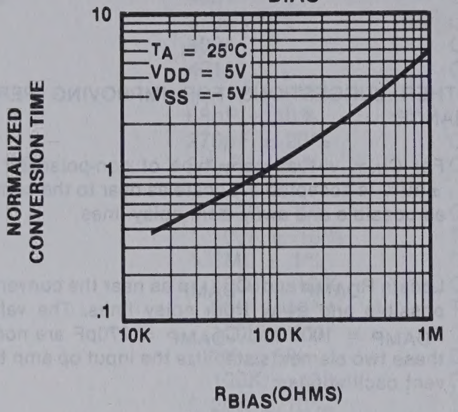
b. Locate R_{DAMP} and C_{DAMP} as near the converter as possible and away from noisy lines. The value of R_{DAMP} = 100Ω and C_{DAMP} = 270pF are nominal; these two elements stabilize the input op amp to prevent oscillations.

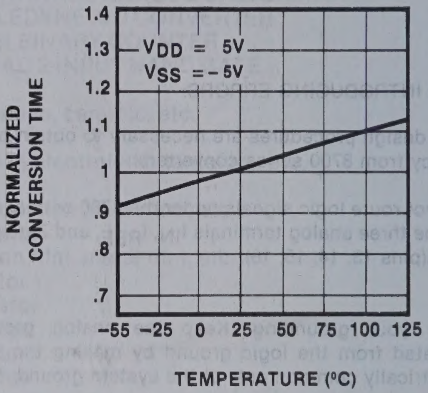
3. CAUTION: WHEN USING ZENERS, OP AMPS AND VOLTAGE REGULATORS:

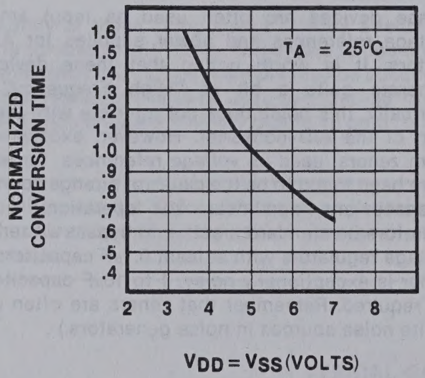
These devices are often used as input amplifiers, voltage references and power supplies for A/D converters. It is worth noting that these devices can generate quite a bit of "High Frequency" noise. Normally, this noise does not interfere with the operation of the A/D converter. However, excessive noise from zeners, used as voltage references for example, have been found to be the cause of strange counting sequences and non-linear A/D operation. It should therefore be standard practice to bypass all zeners and voltage regulators with at least 0.1μF capacitors. (If the zener is exceptionally noisy, 1 to 10μF capacitors may be required. Remember that zeners are often used as white noise sources in noise generators.)

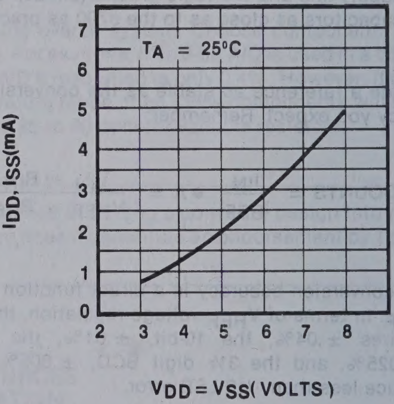
If erratic operation is still observed, then either the op amp's feedback resistor or the output should be bypassed. Note also that the noise level of zeners, op amps and voltage regulators varies from lot to lot and especially from one manufacturer to another. Bypassing these devices during the design stage will prevent the noise level variation from becoming a possible production problem.

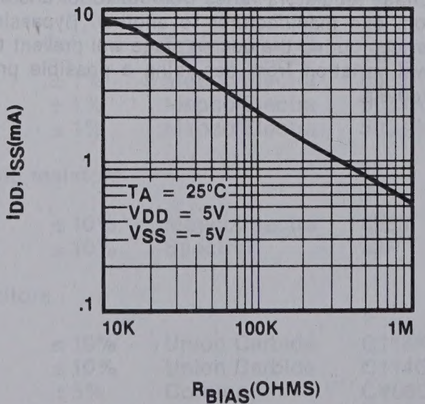
TYPICAL PERFORMANCE CURVES

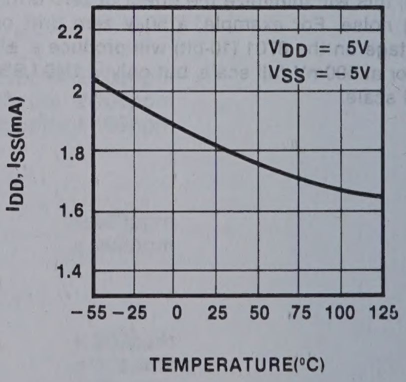

CONVERSION TIME vs R_{BIAS}


CONVERSION TIME vs TEMPERATURE


CONVERSION TIME vs SUPPLY VOLTAGE

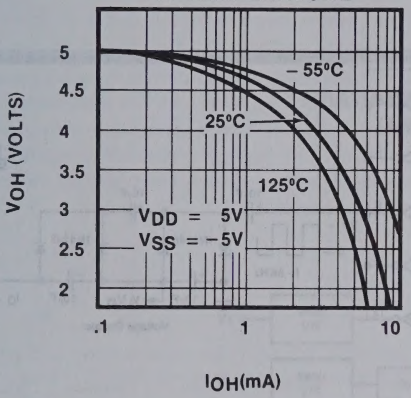

SUPPLY CURRENT vs SUPPLY VOLTAGE


SUPPLY CURRENT vs R_{BIAS}

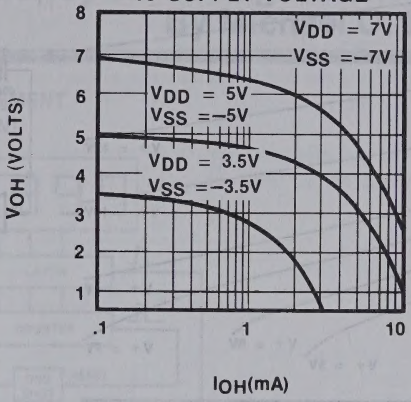

SUPPLY CURRENT vs TEMPERATURE

TYPICAL PERFORMANCE CURVES

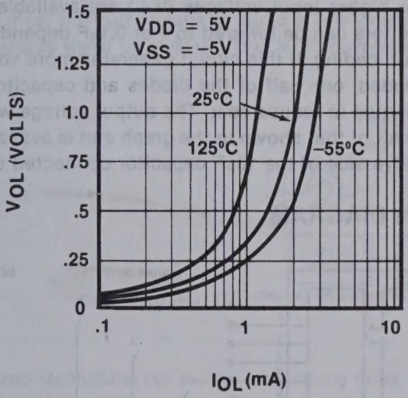
OUTPUT SOURCE CURRENT vs TEMPERATURE



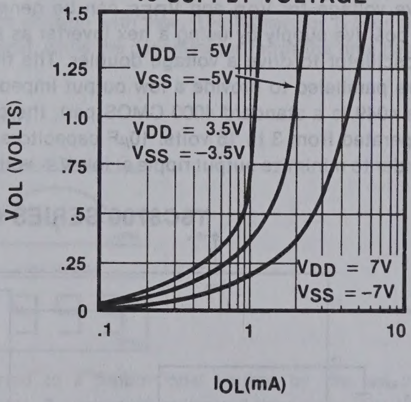
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



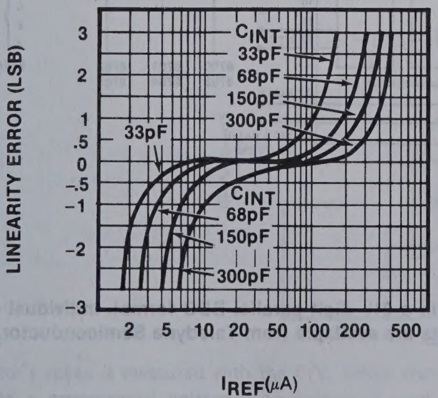
OUTPUT SINK CURRENT vs TEMPERATURE



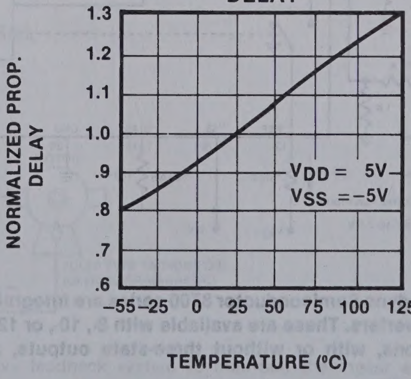
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs IREF

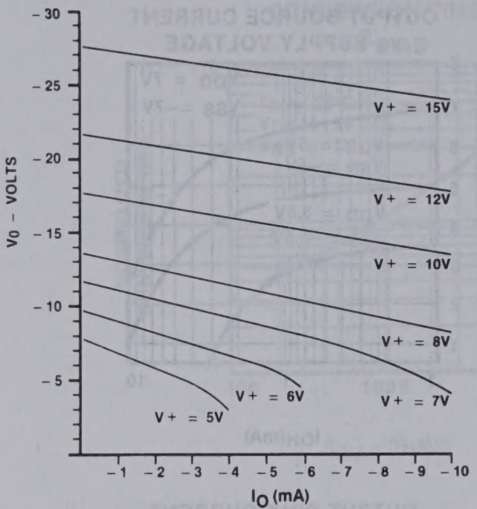


TRI-STATE PROPAGATION DELAY

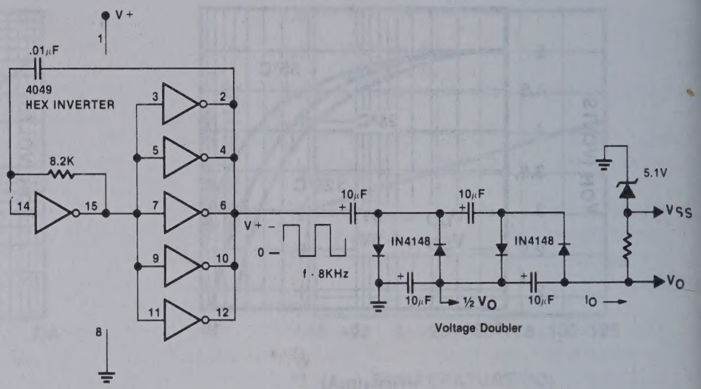


15

NEGATIVE SUPPLY GENERATOR



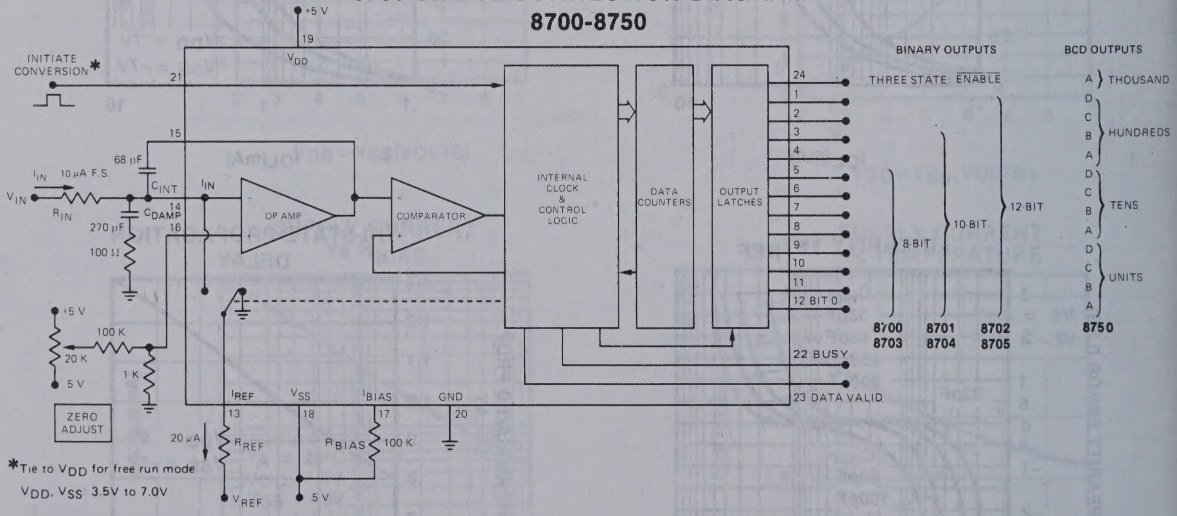
OUTPUT VOLTAGE VS OUTPUT CURRENT


V+
1
.01μF
4049
HEX INVERTER
8.2K
14
15
3
2
5
4
7
6
9
10
11
12
8
V+ –
0 –
f · 8KHz
10μF
10μF
IN4148
IN4148
10μF
½ V_O
10μF
I_O
5.1V
V_{SS}
V_O
Voltage Doubler

A negative voltage for V_{SS} and V_{REF} can be generated from the positive supply by using a hex inverter as a free running oscillator to drive a voltage doubler. The five inverters are paralleled to provide a low output impedance. Since the 4049 is a standard 4000 CMOS part, the circuit can be operated from 3 to 15 volts. 10μF capacitors were used in order to minimize output ripple at low V+ voltages.

When higher input voltages (V+) are available the 10μF capacitors can be lowered to 1 or 0.1μF depending on the output loading. If this circuit generates more voltage than is needed, one half of the diodes and capacitors can be eliminated to reduce cost. The output voltage will then be one half of that shown in the graph and is available on the negative side of the 10μF capacitor connected to ground.

TSC8700 SERIES CONNECTION DIAGRAM
8700-8750


+5 V
19
V_{DD}
INITIATE CONVERSION*
21
15
68 pF
I_{IN} 10 μA F.S.
V_{IN}
R_{IN}
C_{INT}
I_{IN}
14
C_{DAMP}
16
270 pF
100 Ω
OP AMP
COMPARATOR
INTERNAL CLOCK & CONTROL LOGIC
DATA COUNTERS
OUTPUT LATCHES
+5 V
100 K
20 K
5 V
1 K
ZERO ADJUST
I_{REF}
13
20 μA
R_{REF}
V_{REF}
V_{SS}
18
5 V
I_{BIAS}
17
R_{BIAS}
100 K
GND
20
24
1
2
3
4
5
6
7
8
9
10
11
12 BIT 0
22 BUSY
23 DATA VALID
BINARY OUTPUTS
THREE STATE: ENABLE
8-BIT
10-BIT
12-BIT
8700
8703
8701
8704
8702
8705
BCD OUTPUTS
A THOUSAND
D C B A HUNDREDS
D C B A TENS
D C B A UNITS
8750

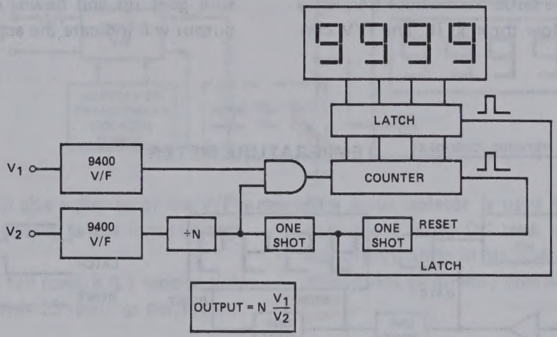
*Tie to V_{DD} for free run mode
V_{DD}, V_{SS}: 3.5V to 7.0V

The Teledyne Semiconductor 8700 series are integrating A/D converters. These are available with 8-, 10-, or 12-bit resolutions, with or without three-state outputs, and also in a 3½ digit parallel BDC format. Individual data sheets are available from Teledyne Semiconductor.

TELEDYNE SEMICONDUCTOR

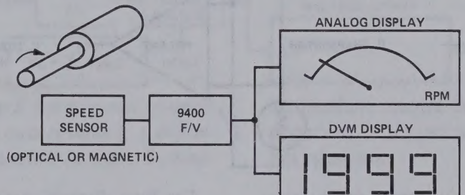
Application Note 10
Applications of the TSC9400 Voltage to Frequency Frequency to Voltage Converter
By Michael O. Paiva

RATIOMETRIC MEASUREMENT (ANALOG DIVISION)


9999
LATCH
V1
9400 V/F
COUNTER
V2
9400 V/F
÷N
ONE SHOT
ONE SHOT
RESET
LATCH
OUTPUT = N $\frac{V_1}{V_2}$

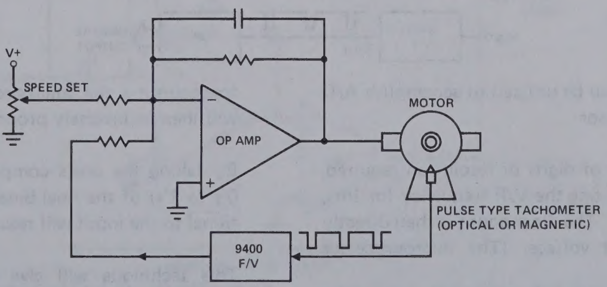
Dne of the most difficult circuits to build is one which will ivide one analog signal by another. Two V/F converters can do such division with ease. The numerator is counted directly as a signal, while the denominator forms the time base.

RPM/SPEED INDICATOR


ANALOG DISPLAY
RPM
SPEED SENSOR
9400 F/V
(OPTICAL OR MAGNETIC)
DVM DISPLAY
1999
RPM

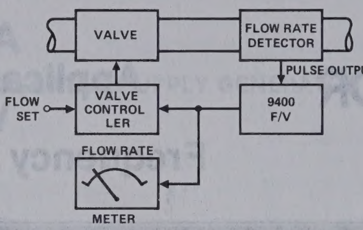
Flow rates and revolutions per second are nothing more than requency signals since they measure the number of events per ime period. Optical and magnetic sensors will convert these lows and revolutions into a digital signal which in turn can be converted to a proportional voltage by the use of an F/V converter. A simple voltmeter will then give a visual indication of the speed.

MOTOR SPEED CONTROL


V+
SPEED SET
OP AMP
−
+
MOTOR
PULSE TYPE TACHOMETER (OPTICAL OR MAGNETIC)
9400 F/V

The motor's speed is measured with the F/V, which converts RPM into a proportional voltage. This voltage is used in a negative feedback system to maintain the motor at the controlled setting.

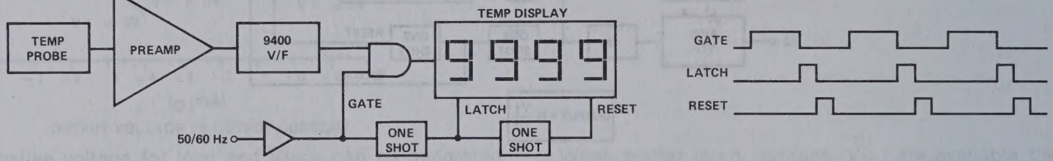
PROPORTIONAL FLOW RATE CONTROLLER

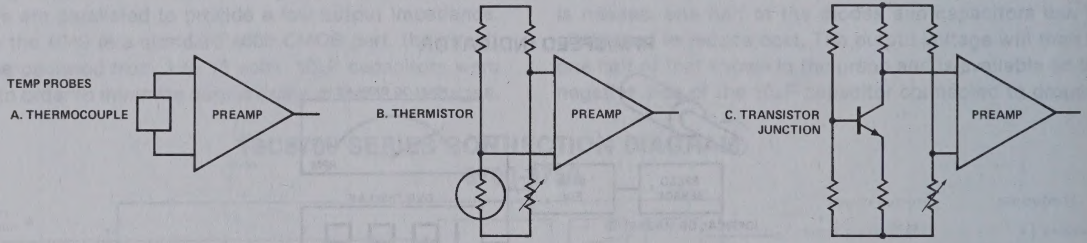

VALVE
FLOW RATE DETECTOR
PULSE OUTPUT
FLOW SET
VALVE CONTROL LER
9400 F/V
FLOW RATE
METER

A 9400 F/V can be used to regulate the amount of liquid or gas flowing through a pipeline.

The flow rate detector generates a pulse train whose frequency is proportional to the rate of flow through it. The F/V converts this frequency to a proportional analog voltage which is used to drive the valve controller. The valve controller regulates the valve so that the flow is steady even though pipeline pressure goes up and down. A voltmeter connected to the F/V output will indicate the actual instantaneous flow rate.

TEMPERATURE METER

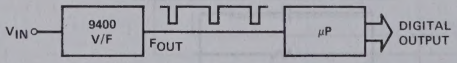

TEMP PROBE
PREAMP
9400 V/F
TEMP DISPLAY
9999
GATE
LATCH
RESET
50/60 Hz
ONE SHOT
ONE SHOT
GATE
LATCH
RESET


TEMP PROBES
A. THERMOCOUPLE
PREAMP
B. THERMISTOR
PREAMP
C. TRANSISTOR JUNCTION
PREAMP

A temperature meter using the voltage output of a probe, such as one of the three shown, can be economically and straightforwardly implemented with the 9400 V/F. The V/F output is simply counted to display the temperature.

For long distance data transmission, the 9400 can be used to modulate an RF transmitter.

A/D CONVERSION WITH A MICROPROCESSOR


V_{IN}
9400 V/F
F_{OUT}
μP
DIGITAL OUTPUT

There are two schemes that can be utilized to accomplish A/D conversion with a microprocessor:

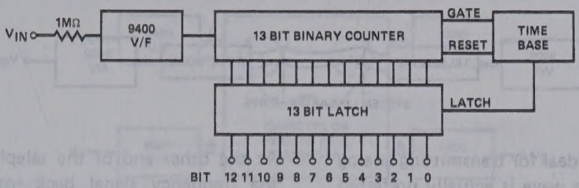
1. Depending on the number of digits of resolution required, V_{OUT} is measured by counting the V/F frequency for 1ms, 10ms, 100ms, or 1 second. The final count is then directly proportional to the input voltage. (The microprocessor provides the time base.)

2. V_{IN} is measured by determining the time between two pulses (negative edges). The F_{OUT} signal is used as a gate for counting the microprocessor's clock. The final count will then be inversely proportional to the input signal.

   By taking the one's complement (changing 1's to 0's and 0's to 1's) of the final binary count a value directly proportional to the input will result.

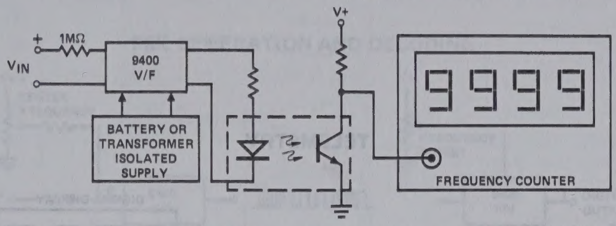
   This technique will give a faster conversion time when resolution is very important, but dynamic range is limited.

13 BIT A/D CONVERTER


VIN
1MΩ
9400 V/F
13 BIT BINARY COUNTER
GATE
RESET
TIME BASE
13 BIT LATCH
LATCH
BIT 12 11 10 9 8 7 6 5 4 3 2 1 0

A 13 bit binary or 4 digit BCD A/D converter can be built by combining the 9400 V/F with a counter, latch and time base. When the V/F is set up for 10KHz full scale a 1 second time base will provide one conversion per second.

4 DIGIT VOLTMETER W/OPTO-ISOLATED INPUT

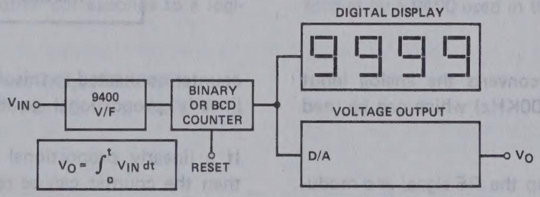

VIN
+
1MΩ
9400 V/F
BATTERY OR TRANSFORMER ISOLATED SUPPLY
V+
9999
FREQUENCY COUNTER

The use of a frequency counter will give a display of the V/F's frequency which is directly proportional to the input voltage.

When the V/F is running at 10KHz full scale, a 0.1 second time base will give 3 digit resolution with 10 readings per second.

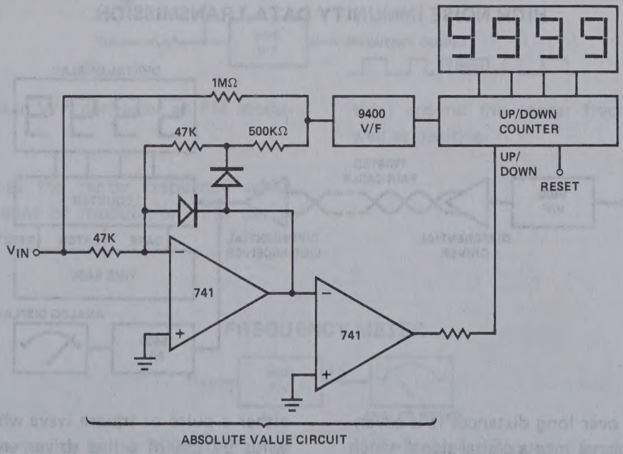
The opto isolator is used for transmitting the frequency so that there is no DC path to the frequency counter. This is especially handy in medical applications where a voltage probe should not be directly connected to a human body.

LONG TERM INTEGRATOR WITH INFINITE HOLD


DIGITAL DISPLAY
9999
VIN
9400 V/F
BINARY OR BCD COUNTER
VOLTAGE OUTPUT
D/A
VO
$V_O = \int_0^t V_{IN}\,dt$
RESET

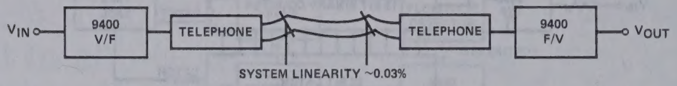
This system will integrate an input signal for minutes or days and hold its output indefinitely. The data is held in a digital counter and will stay there until the counter is reset. Typical applications involve controlling the amount of surface metal deposited in a plating system or how much charge a battery has taken on.

LONG TERM INTEGRATOR FOR BIPOLAR (+/–) SIGNALS


9999
1MΩ
47K
500KΩ
9400 V/F
UP/DOWN COUNTER
UP/ DOWN
RESET
47K
VIN
741
741
ABSOLUTE VALUE CIRCUIT

When the input signal is negative as well as positive there needs to be a way of generating "negative" frequencies. An absolute value circuit accomplishes this by giving the V/F a positive voltage only; and also telling the counter to count up for a positive voltage and to count down for a negative voltage.

ANALOG SIGNAL TRANSMISSION OVER TELEPHONE LINES

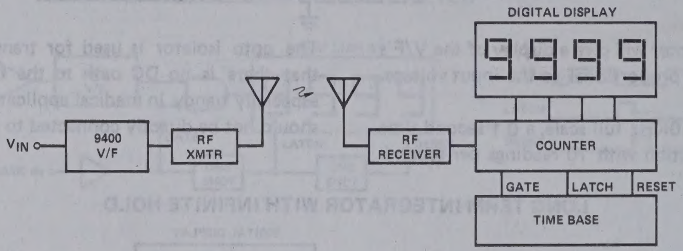

VIN
9400 V/F
TELEPHONE
TELEPHONE
9400 F/V
VOUT
SYSTEM LINEARITY ~0.03%

The 9400's square wave output is ideal for transmitting analog data over telephone lines. A square wave is actually preferred over a pulse waveform for data transmission since the square wave takes up less frequency spectrum than a pulse waveform.

The square wave's spectrum can be further reduced by use of low pass filters.

At the other end of the telephone line a 9400 F/V converts the frequency signal back into a voltage output which is linearly proportional to the original input voltage.

TELEMETRY

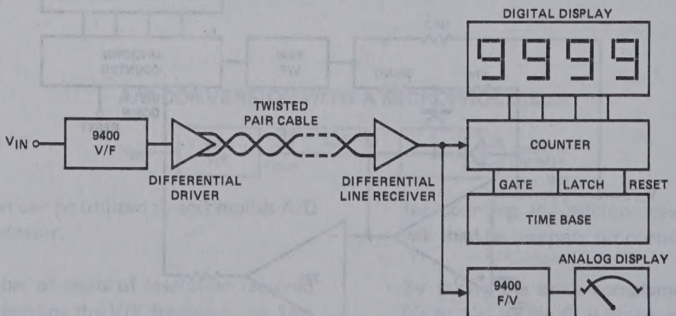

DIGITAL DISPLAY
9999
VIN
9400 V/F
RF XMTR
RF RECEIVER
COUNTER
GATE
LATCH
RESET
TIME BASE

In a telemetry system the 9400 converts the analog input (V_{IN}) into frequencies (10Hz to 100KHz) which can be used to modulate an RF transmitter.

At the other end a receiver picks up the RF signal and modulates it back into the 10Hz to 100KHz spectrum. A frequency counter connected to this signal will then give a count which is linearly proportional to the original analog voltage (V_{IN}).

If a linearly proportional analog output voltage is required, then the counter can be replaced by a 9400 used in the F/V mode.

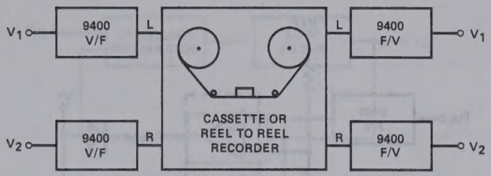
HIGH NOISE IMMUNITY DATA TRANSMISSION


DIGITAL DISPLAY
9999
TWISTED PAIR CABLE
VIN
9400 V/F
DIFFERENTIAL DRIVER
DIFFERENTIAL LINE RECEIVER
COUNTER
GATE
LATCH
RESET
TIME BASE
ANALOG DISPLAY
9400 F/V

When transmitting analog data over long distances it is advantageous to convert the analog signal into a digital signal which will be less susceptible to noise pick-up.

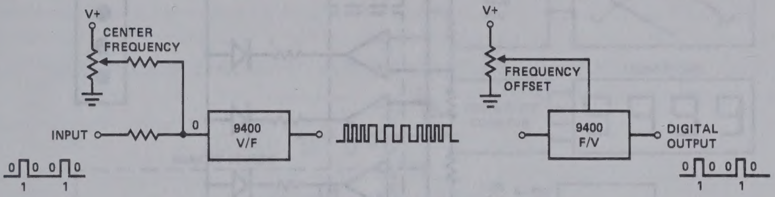
In the above system the 9400 converts the input voltage into either a pulse or square wave which is transmitted on a pair of wires by use of a line driver and receiver. At the other end the original voltage (V_{IN}) can be digitally displayed on a frequency counter or converted back to an analog voltage by use of a 9400 F/V converter.

DC RESPONSE DATA RECORDING SYSTEM


V_1
9400 V/F
L
R
V_2
9400 V/F
CASSETTE OR REEL TO REEL RECORDER
L
9400 F/V
V_1
R
9400 F/V
V_2

Low frequency analog data (DC to 10KHz) can be recorded anywhere, stored and then reproduced. By varying the playback speed, the frequency spectrum of the original data can be shifted up or down.

FSK GENERATION AND DECODING


V+
CENTER FREQUENCY
INPUT
0
9400 V/F
0 1 0 0 1 0
V+
FREQUENCY OFFSET
9400 F/V
DIGITAL OUTPUT
0 1 0 0 1 0

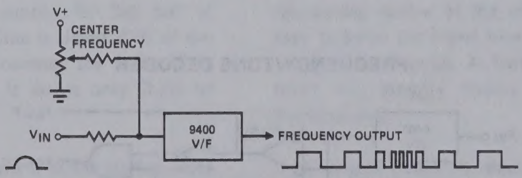
Frequency shift keying (FSK) is a simple means of transmitting digital data over a signal path (two wires, telephone lines, AM transmitters or FM transmitters).

Typically only two frequencies are transmitted. One corresponds to a logical "0" while the other corresponds to a logical "1".

A 9400 V/F will generate these two frequencies when connected as shown above. The potentiometer sets the V/F to the lower frequency. The digital input will then determine which frequency is selected. A "0" selects the lower frequency while a "1" selects the upper frequency.

The digital frequency signal is converted back into a digital format by a 9400 used in the F/V mode.

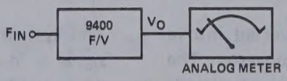
ULTRA LINEAR FREQUENCY MODULATOR


V+
CENTER FREQUENCY
V_{IN}
9400 V/F
FREQUENCY OUTPUT

Since the 9400 is a very linear V/F converter an FM modulator is very easy to build.

The potentiometer determines the center frequency while V_{IN} will determine the amount of modulation (FM deviation) around the center frequency. V_{IN} can be negative as well as positive.

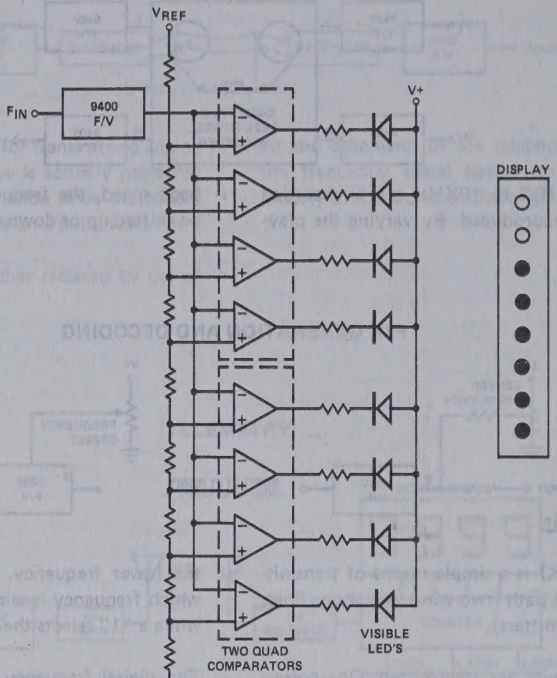
FREQUENCY METER


F_{IN}
9400 F/V
V_O
ANALOG METER

The 9400 will convert any frequency below 100KHz into an output voltage, which is linearly proportional to the input frequency. The equivalent frequency is then displayed on an analog meter.

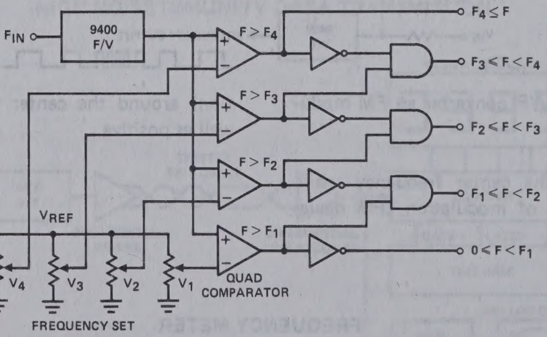
If the incoming frequency is above 100KHz a frequency divider in front of the 9400 can be used to scale the frequency down to the 100KHz region.

TACHOMETER BAR GRAPH DISPLAY


VREF
FIN
9400
F/V
V+
DISPLAY
TWO QUAD
COMPARATORS
VISIBLE
LED'S

A tachometer can be constructed by using the 9400 in the F/V mode to convert the frequency information (RPM) into a linearly proportional voltage. This voltage is then compared to one of n comparators (8 in this example). When the voltage exceeds the trip point of a comparator the respective LED will light up and continue to stay lit as long as the voltage exceeds the trip point. This will give a bar graph type display with the height of the bar being proportional to RPM.

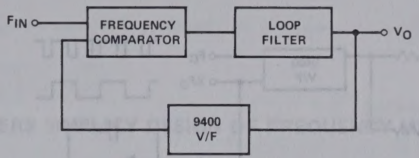
FREQUENCY/TONE DECODER


FIN
9400
F/V
F > F4
F > F3
F > F2
F > F1
F4 ≤ F
F3 ≤ F < F4
F2 ≤ F < F3
F1 ≤ F < F2
0 ≤ F < F1
VREF
V4
V3
V2
V1
QUAD
COMPARATOR
FREQUENCY SET

The frequency or tone to be detected is converted into a proportional analog voltage by the 9400 F/V converter. The quad comparators sense when the voltage (frequency) exceeds any of the four preset frequency limits. A logical "1" at any of the five outputs indicates that the frequency is within those limits.

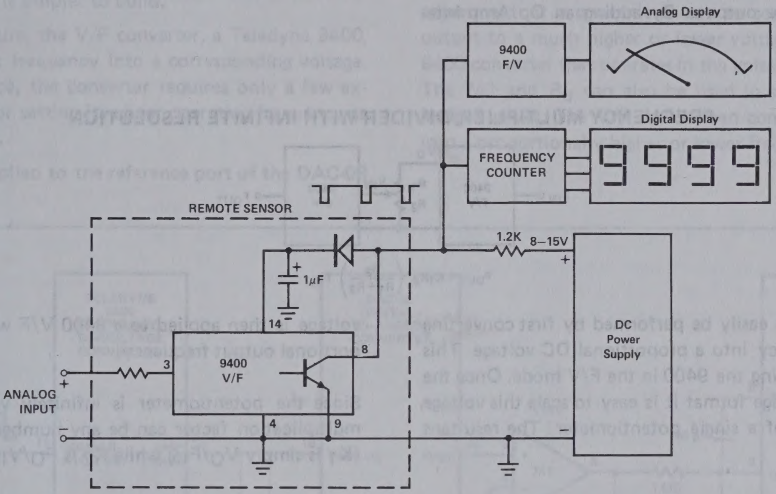
This system is useful for determining which frequency band a signal is in or for remote control where each frequency band corresponds to a different command.

FM DEMODULATION WITH A PHASE LOCKED LOOP


FIN
FREQUENCY COMPARATOR
LOOP FILTER
VO
9400 V/F

e high linearity of the 9400 (0.01%) is used to greatly prove the performance of a phase locked loop, resulting in very precise tracking of V_O with respect to F_{IN}.

ANALOG DATA TRANSMISSION ON DC SUPPLY LINES (TWO WIRE TRANSMITTER)


Analog Display
9400 F/V
Digital Display
9999
FREQUENCY COUNTER
REMOTE SENSOR
1.2K
8–15V
+
1μF
14
8
3
9400 V/F
ANALOG INPUT
+
−
4
9
DC Power Supply
−

y converting an analog voltage to a linearly proportional ulse train of short duration, it is possible to transmit this ata on the same wires that are used to energize the V/F onverter.

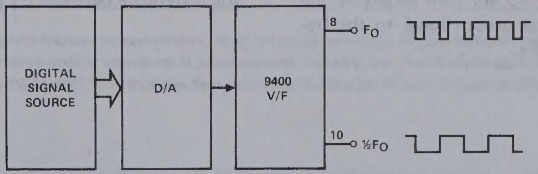
he 9400 V/F shorts out the DC supply for $3\mu s$ out of ch period. At 100KHz the supply line is down 30% of the $0\mu s$ period. As the frequency is lowered the down time ecreases so that at 1KHz the line is down only 0.3% of e time.

wo precautions are necessary to assure that the system does ot stop functioning during the shorting period. At the power pply end a 1.2K resistor limits the current to 10mA on a 5V supply line. This prevents the 9400 from being operated eyond its output rating and at the same time it prevents the pply from being shorted out. At the V/F end a capacitor is used to keep the 9400 energized while the diode keeps the capacitor from being discharged.

Since the 9400 requires only 2mA of current, a $1\mu F$ capacitor ensures a stable voltage (the ripple is only 6mV). Since the $3\mu s$ pulses appear at the left side of the 1.2K resistor, it is easy to sense the signal here and convert the data back into a recognizable format. A frequency counter connected at this point will directly display the input voltage by counting the frequency.

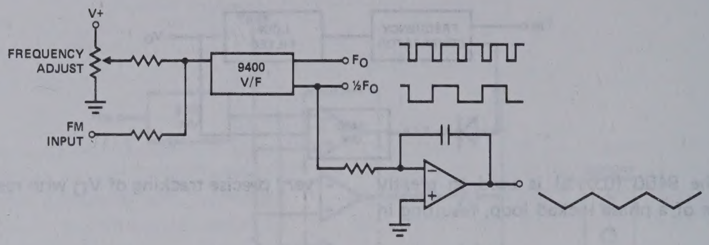
If an analog output is required, a 9400 in the F/V mode can be used to convert the frequency back into a voltage. The overall linearity is in the order of 0.03%, when both V/F and F/V are used. If only the V/F is used, then 0.01% linearity can easily be achieved.

DIGITALLY CONTROLLED FREQUENCY SOURCE


DIGITAL SIGNAL SOURCE
D/A
9400 V/F
8
FO
10
½FO

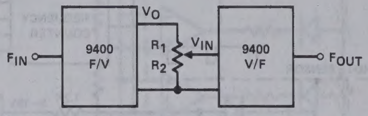
his system generates frequencies which are controlled by a icroprocessor counter, register, or by thumb-wheel switches. Applications for such a system include computer controlled test equipment and numerically controlled machine tools.

WIDE FREQUENCY RANGE PULSE GENERATOR



The 9400 V/F is useful in the laboratory as a portable, battery operated low cost frequency source. The 9400 provides both pulse and square wave outputs. By adding an Op Amp integrator, a triangular waveform can also be generated. Th outputs can be frequency modulated via the FM input.

FREQUENCY MULTIPLIER/DIVIDER WITH INFINITE RESOLUTION

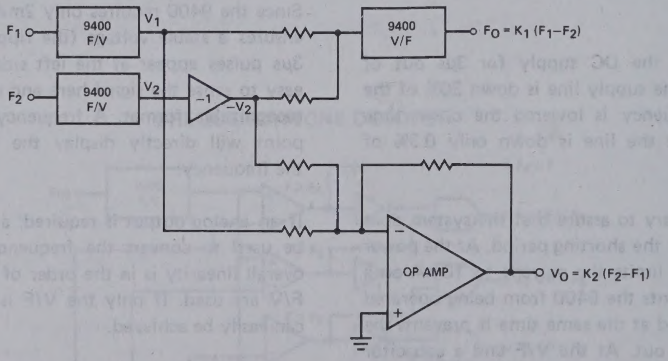


$$F_{OUT} = K_1K_2\left(\frac{R_2}{R_1 + R_2}\right) F_{IN}$$

Frequency scaling can easily be performed by first converting the incoming frequency into a proportional DC voltage. This is accomplished by using the 9400 in the F/V mode. Once the frequency is in a voltage format it is easy to scale this voltage up or down by use of a single potentiometer. The resultant voltage is then applied to a 9400 V/F which generates a pro portional output frequency.

Since the potentiometer is infinitely variable, the division multiplication factor can be any number, including fraction (K_1 is simply V_O/F_{IN} while K_2 is F_O/V_{IN}).

FREQUENCY DIFFERENCE MEASUREMENT



Frequency difference measurement is accomplished by using two 9400's in the F/V mode to convert both frequencies into two proportional analog voltages (V_1 and V_2). V_2 is inverted by a unity gain inverter. V_1 and $-V_2$ are then added by the summing Op Amp to give a voltage proportional to the frequency difference between F_2 and F_1.

Since the 9400 V/F input is actually the summing junctio to an Op Amp, V_1 and $-V_2$ can be summed at the 940 input to generate a frequency output which is proportional t the difference between F_1 and F_2.

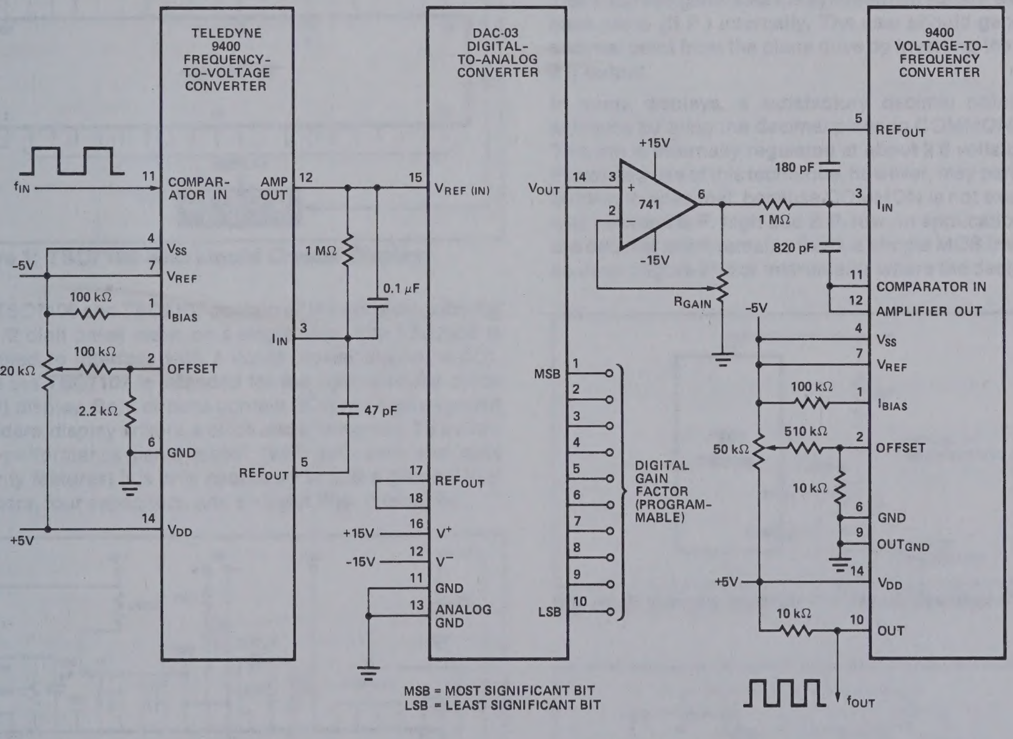
CONVERTERS SIMPLIFY DESIGN OF FREQUENCY MULTIPLIER*

y using a programmable digital-to-analog converter in com- ination with frequency-to-voltage and voltage-to-frequency onverters, this circuit can multiply an input frequency by any umber. Because it needs neither combinational logic nor a igh-speed counter, it is more flexible than competing designs, ses fewer parts, and is simpler to build.

s shown in the figure, the V/F converter, a Teledyne 9400, ransforms the input frequency into a corresponding voltage. n inexpensive device, the converter requires only a few ex- ernal components for setting its upper operating frequency as igh as 100 kilohertz.

ext the signal is applied to the reference port of the DAC-03 d-a converter, where it is amplified by the frequency-multiplying factor programmed into the converter by thumbwheel switches or a microprocessor. The d-a converter's output is the product of the analog input voltage and the digital gain factor.

R_3 sets the gain of the 741 op amp to any value, providing trim adjustment or a convenient way to scale the d-a converter's output to a much higher or lower voltage for the final stage, a 9400 converter that operates in the voltage-to-frequency mode. The 741 and R_3 can also be used to set circuit gain to non-integer values. The V/F device then converts the input voltage into a proportionally higher or lower frequency.



TELEDYNE 9400 FREQUENCY-TO-VOLTAGE CONVERTER
f_{IN}
11 COMPARATOR IN
AMP OUT 12
4 V_{SS}
-5V
7 V_{REF}
100 kΩ
1 I_{BIAS}
100 kΩ
20 kΩ
2 OFFSET
2.2 kΩ
6 GND
14 V_{DD}
+5V
I_{IN} 3
REF_{OUT} 5
1 MΩ
0.1 µF
47 pF
DAC-03 DIGITAL-TO-ANALOG CONVERTER
15 V_{REF (IN)}
17 REF_{OUT}
18
16 V+
+15V
12 V−
-15V
11 GND
13 ANALOG GND
V_{OUT} 14
MSB 1 2 3 4 5 6 7 8 9 10 LSB
DIGITAL GAIN FACTOR (PROGRAMMABLE)
MSB = MOST SIGNIFICANT BIT
LSB = LEAST SIGNIFICANT BIT
+15V
741
-15V
R_{GAIN}
1 MΩ
180 pF
820 pF
-5V
9400 VOLTAGE-TO-FREQUENCY CONVERTER
5 REF_{OUT}
3 I_{IN}
11 COMPARATOR IN
12 AMPLIFIER OUT
4 V_{SS}
7 V_{REF}
100 kΩ
1 I_{BIAS}
510 kΩ
50 kΩ
2 OFFSET
10 kΩ
6 GND
9 OUT_{GND}
14 V_{DD}
+5V
10 kΩ
10 OUT
f_{OUT}

Circuit uses frequency-to-voltage-to-frequency conversion, with intermediate stage of gain between conversions, for multiplying input frequency by any number. Digital-to-analog converter is programmed digitally, by thumbwheel switches or microprocessor, for coarse selection of frequency-multiplying factor; 741 provides fine gain, enables choice of non-integer multiplication values.

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Notes

TELEDYNE SEMICONDUCTOR

Application Note 11
TSC7106/7107
Digital Meter Applications Including Kit Assembly Instructions

Instructions for the LCD and LED Kits

Two kits are offered; the TSC7106 EV/Kit and the TSC7107 EV/Kit. Each kit contains the appropriate IC, a circuit board, a display (LCD/TSC7106, LED/TSC7107), passive components and miscellaneous hardware.

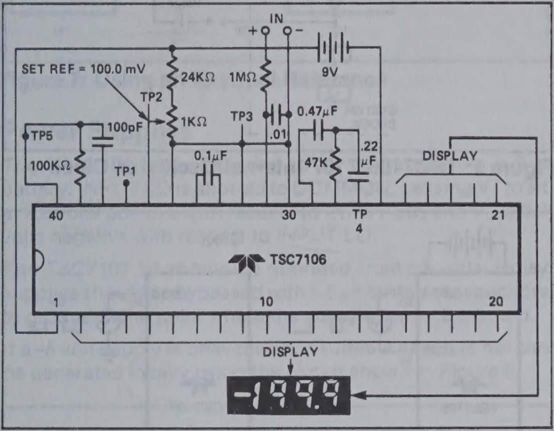

IN
+
−
9V
SET REF = 100.0 mV
24KΩ
1MΩ
TP2
1KΩ
TP3
.01
0.47µF
TP5
100pF
0.1µF
.22 µF
100KΩ
TP1
47K
DISPLAY
40
30
TP 4
21
TSC7106
1
10
20
DISPLAY
-199.9

Figure 1: TSC7106 with Liquid Crystal Display

The TSC7106 and TSC7107 contain all the acive circuitry for a 3-1/2 digit panel meter on a single chip. The TSC7106 is designed to interface with a liquid crystal display (LCD), while the TSC7107 is intended for the light-emitting diode (LED) display. Both circuits contain BCD to seven segment decoders, display drivers, a clock and a reference. To build a high-performance panel meter, (with auto-zero and auto polarity features) it is only necessary to add a display, four resistors, four capacitors, and an input filter if required.

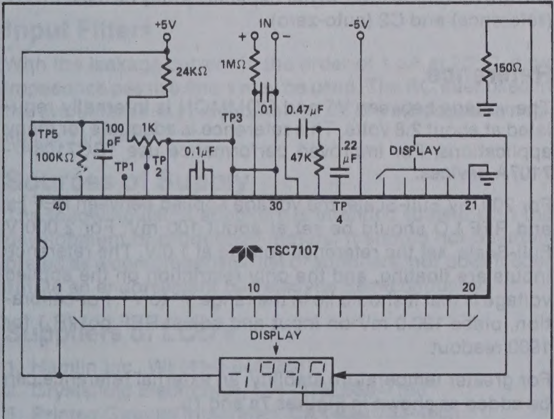

+5V
IN
+
−
-5V
24KΩ
1MΩ
150Ω
TP3
.01
0.47µF
TP5
100 pF
1K
100KΩ
TP 2
TP1
0.1µF
47K
.22 µF
DISPLAY
40
30
TP 4
21
TSC7107
1
10
20
DISPLAY
-1999

Figure 2: TSC7107 with LED Display

Assembly

The circuit board layouts and assembly drawings are shown in Figure 17 (TSC7106) and Figure 18 (TSC7107). Pin strips are used to provide a low-cost socket. One IC board can thus be used to evaluate several IC's. Solder terminals are provided for the first five test points and for the ± 5 V input on the TSC7107 kit. A provision has been made for separating REF LO from COMMON when using an external reference zener. Provision has also been made for connecting an external clock. A value of 150 ohms is used for decimal point (TSC7107 EV/Kit).

Liquid Crystal Display (TSC7106)

The TSC7106 generates the symmetrical square wave to the back plane (B.P.) internally. The user should generate the decimal point from the plane drive by inverting the B.P. (pin 21) output.

In some displays, a satisfactory decimal point can be achieved by tying the decimal plane to COMMON (pin 32). This pin is internally regulated at about 2.8 volts below V^+. Prolonged use of this technique, however, may permanently burn-in the decimal, because COMMON is not exactly midway between B.P. high and B.P. low. In applications where the decimal point remains fixed, a simple MOS inverter can be used (Figure 3). For instruments where the decimal point

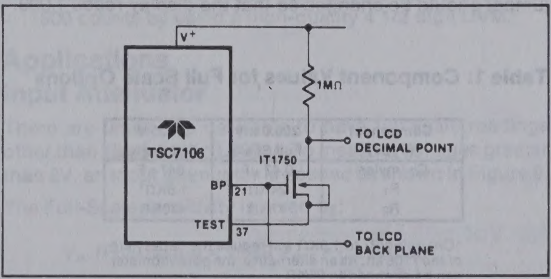

V+
1MΩ
TSC7106
TO LCD DECIMAL POINT
IT1750
BP
21
TEST
37
TO LCD BACK PLANE

Figure 3: Simple Inverter for Fixed Decimal Point

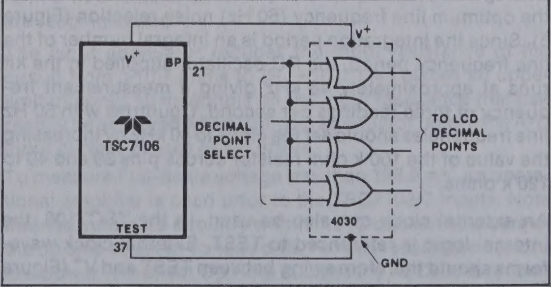

V+
V+
BP
21
TSC7106
DECIMAL POINT SELECT
TO LCD DECIMAL POINTS
4030
TEST
37
GND

Figure 4: Exclusive 'OR' Gate for Decimal Point Drive

must be shifted, a quad exclusive OR gate is recommended (Figure 4). Note that in both instances, TEST (pin 37, TP1) is used as V^- for the inverters. This pin is capable of sinking about 1 mA and is approximately 5 volts below V^+. The B.P. output (pin 21) oscillates between V^+ and TEST.

Light Emitting Diode Display (TSC7107)

The TSC7107 will sink 8 mA per segment. This drive produces a bright display suitable for most applications. A fixed decimal point can be turned on by tying the appropriate cathode to ground through a 150 ohm resistor. The circuit boards supplied with the kits will accommodate either HP 0.3 displays or the MAN 3700 types. Note that the HP has the decimal point cathode on pin 6, whereas the MAN 3700 has the decimal point cathode on pin 9. Not all the decimal points are brought out to jumper pads. It may be necessary to wire directly from the 150 ohm resistor to the display. For multiple range instruments, a 7400 series CMOS quad gate should be used.

Full-Scale Readings

200 mV Full-Scale — The kits have been optimized for 200 mV Full-Scale. The component values supplied are those specified in Figures 1 and 2.

2,000 V Full-Scale — The component values in Table 1 change the integrator time constant and reference and the auto-zero capacitor time constant. These extra components are not supplied in the kits. In addition, the decimal point jumper should be changed so that the display reads 1.999.

Table 1: Component Values for Full Scale Options

Component (Type)	200.0 mV Full Scale	2.000 V Full Scale
C_2 (mylar)	0.47 μF	.047 μF
R_1	24KΩ	1.5KΩ*
R_2	47KΩ	470KΩ

*Changing R_1 to 1.5KΩ will reduce the battery life of the 7106 kit. As an alternative, the potentiometer can be changed to 25KΩ.

Clock

Setting the clock oscillator at precisely 48 kHz will result in the optimum line frequency (60 Hz) noise rejection (Figure 5). Since the integration period is an integral number of the line frequency period, the RC oscillator supplied in the kit runs at approximately 48 kHz giving a measurement frequency of three readings per second. Countries with 50 Hz line frequencies should set the clock to 40 kHz by increasing the value of the 100 k ohm resistor across pins 39 and 40 to 120 k ohms.

An external clock can also be used. In the TSC7106, the internal logic is referenced to TEST. External clock waveforms should therefore swing between TEST and V^+ (Figure 6A). In the TSC7107, the internal logic is referenced to GND so any generator whose output swings from ground to +5 V will work well, (Figure 6b).

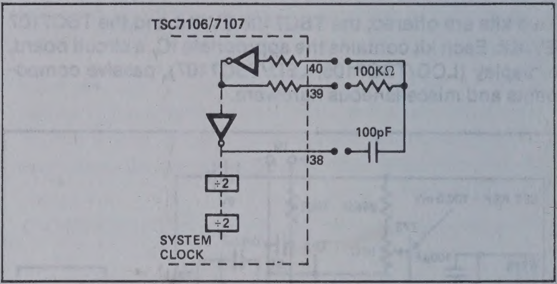


Figure 5: TSC7106/7107 Internal Oscillator/Clock

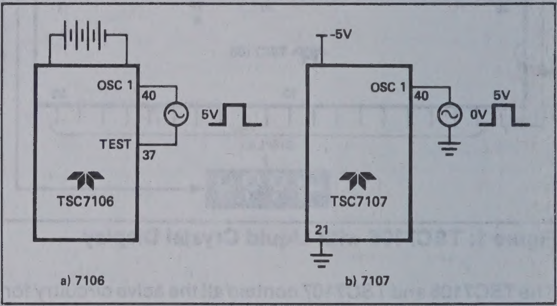


Figure 6: External Clock Options

Capacitors

The dual slope technique cancels the effects of long term stability and temperature coefficient. The integration capacitor should have low dielectric loss. Inexpensive polypropelene capacitors have the low dielectric loss characteristics and are recommended. Mylar capacitors may be used for C1 (reference) and C2 (auto-zero).

Reference

The voltage between V^+ and COMMON is internally regulated at about 2.8 volts. This reference is adequate for many applications. For improved performance use TSC7106A/-7107A devices.

For 200 mV Full-Scale, the voltage applied between REF HI and REF LO should be set at about 100 mV. For 2.000 V Full-Scale, set the reference voltage at 1.0.V. The reference inputs are floating, and the only restriction on the applied voltage is that it should lie in the range V^- to V^+. For calibration, place 190.0 mV on input and adjust REF pot (R_4) for 1900 readout.

For greater temperature stability, an external reference can be added as shown in Figures 7a and 7b.

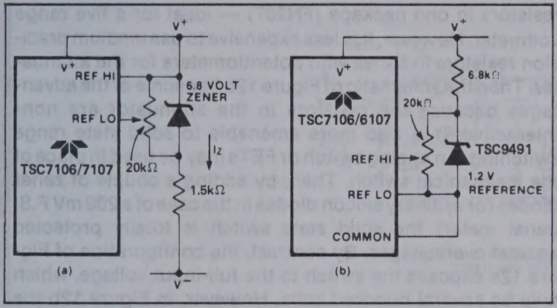


Figure 7: Using an External Reference

Power Supplies

The TSC7106 kit is intended to be operated from a 9 V battery. INPUT LO is shorted to COMMON, causing V^+ to sit at 2.8 volts positive with respect to INPUT LO, and V^- at 6.2 volts negative with respect to INPUT LO.

The TSC7107 kit should be operated from ±5 volts. Noisy supplies should be bypassed with 6.8 μF tantalum capacitors to ground at the point where the supplies enter the board.

If a -5 volt supply is unavailable, a suitable negative rail can be generated locally using the circuit shown in Figure 8.

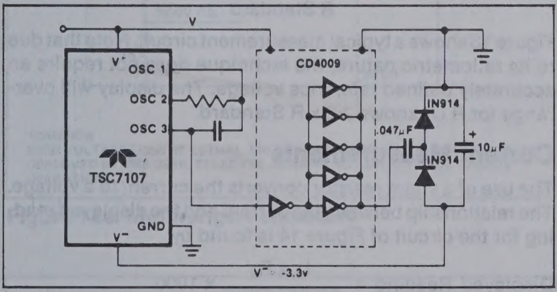


Figure 8: Generating Negative Supply from +5 V

Input Filters

With the leakage current in the order of 1 pA at 25° C, high impedance passive filters may be used. The RC filter used in the evaluation kits (1 megohm — 0.01 μF) introduces a negligible 1 μV error.

Sources of Supply

The following list of suppliers is intended to help with the development of production meters. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Teledyne Semiconductor:

Suppliers of LCD's

1. Hamlin Inc., WI (414) 648-2361
2. Crystalloid Electronics, OH (216) 688-1180
3. Printed Circuits Integrated, CA (408) 733-4603
4. IEE Inc., CA (213) 787-0311

Suppliers of LED's

1. AND, CA (415) 347-9916
2. Litronix Inc., CA (408) 257-7910
3. Hewlett-Packard, CA (415) 493-1212
4. General Instruments, CA (415) 493-0400

Suppliers of Polypropelene Capacitors

1. Plessey Capacitors, CA (213) 889-4120
2. IMB Electronic Products, CA (213) 921-3407
3. Elcap Electronics, CA (714) 979-4400
4. TRW Capacitors, NB (308) 284-3611

Preliminary Tests

1. Solder flux or other impurities on PC boards may cause leakage paths between IC pins and board traces, reducing performance. Rubbing alcohol or another appropriate cleaning agent should be used to remove impurities.
2. In order to insure that unused segments on the LCD displays do not turn on, tie them to the Back Plane pin (pin 22).
3. Auto-Zero — With the inputs shorted the display should read zero. The negative sign will be on about one half of the time, showing the input to be exactly zero volts.
4. Polarity — A negative sign indicates a negative reading. No sign indicates a positive reading.
5. Overrange — For inputs greater than Full-Scale, only 1 or -1 will be displayed. The three least significant digits will be suppressed.
6. Calibration — The instrument should be calibrated at 1900 counts by using a high-quality 4 1/2 digit DVM.

Applications

Input Attenuator

There are times it is desirable to have full scale readings other than 199.9 mV or 1.999 V. To measure voltages greater than 2V, an input attenuator is needed as shown in Figure 9.

The Full-Scale sensitivity is given by:

$$V_{IN}\ (\text{Full-Scale}) = 1.999\ V_{REF} \times \frac{R_2}{(R_1 + R_2)}$$

It is important that R_1 and R_2 remain fixed for the calibration period of the instrument. Metal film resistors with good long-term drift characteristics, and low temperature coefficients are recommended.

The input attenuator reduces the input resistance of the circuit from $>10^{12}$ ohms to (R_1 + R_2). This places an upper limit of about 10 megohms on the input resistance that can readily be achieved when using an attenuator before the A/D input current causes offset errors.

To measure Full-Scale voltage less than 199.9 mV, an operational amplifier is used prior to the TSC7106/7 inputs. Note that the auto-zero circuitry within the IC can not take care of the op amp offset or voltage drift. For this reason the use of a low power low offset Op Amp such as the TSC900 is recommended.

Figure 10 shows a circuit with ±20 mV Full-Scale and an input resistance greater than 10 megohms.

For scale factors between 100 mV and 1 mV per least significant digit (LSD), simply determine the reference voltage required for the following equation:

$$V_{REF} = (\text{Voltage Change represented by one LSD}) \times 10^3$$

For scale factors greater than 1 mV/LSD, the most straight forward approach is to use an input attenuator in conjunction with a 1 volt reference.

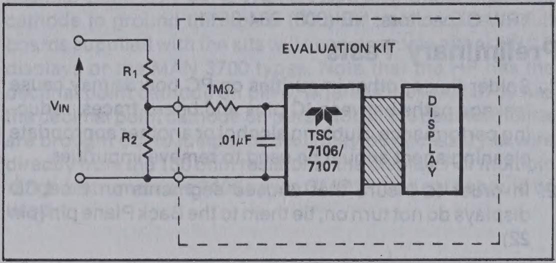


Figure 9: Input Attenuator for $V_{IN} \geq 2.0$ V

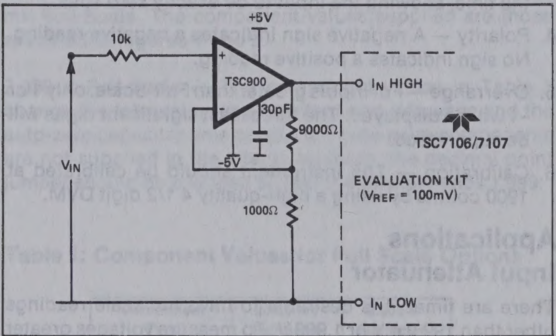


Figure 10:

AC Voltage Measurements

It is necessary to build an AC to DC converter to measure AC voltages with the TSC7106/7. Figure 11 shows a circuit used extensively in commercial 3 1/2 digit DVM's. The circuit responds to the average value of the sinusoidal waveform and assumes low distortion. It has 10 megohms input impedance, 20 Hz to 5 kHz bandwidth, and is AC coupled to the kit introducing to DC errors.

Multi-Range DVM's

Two schemes commonly used are shown in Figures 12a and 12b. The circuit of Figure 12a has the advantage that any switch contact resistance appears in series with the TSC7106/7 input resistance. Since the input resistance is $>10^{12}$ ohms, errors due to the switch are negligible. Precision voltage attenuators (R_1 through R_5) are available from a number of manufacturers. Allen Bradley, for example, makes a thin film network which contains 1 k, 9 k, 90 k, 900 k and 9 M resistors in one package (FN207) — ideal for a five range voltmeter. However, it is less expensive to use medium precision resistors in series with potentiometers for the attenuator. Then the schematic of Figure 12b has some of the advantages because the resistors in the attenuator are non-interactive. It is also more amenable to solid state range switching. An analog switch or FETs may be used in place of the mechanical switch. Then, by adding a couple of zener diodes (or ordinary silicon diodes in the case of a 200 mV F.S. panel meter) the solid state switch is totally protected against overvoltages. By contrast, the configuration of Figure 12a exposes the switch to the full-input voltage, which may be several hundred volts. However, in Figure 12b the switch resistance forms part of the attenuator and could contribute an error.

Resistance Measurements

The ratiometric technique is used. The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input (between IN HI and IN LO), and the voltage across the known resistor applied to the reference input (REF HI and REF LO). If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{\text{R Unknown}}{\text{R Standard}} \times 1000$$

Figure 13 shows a typical measurement circuit. Note that due to its ratiometric nature, the technique does not require an accurately defined reference voltage. The display will overrange for R Unknown ⩾2 x R Standard.

Current Measurements

The use of a shunt resistor converts the current to a voltage. The relationship between the current and the displayed reading for the circuit of Figure 14 is found by:

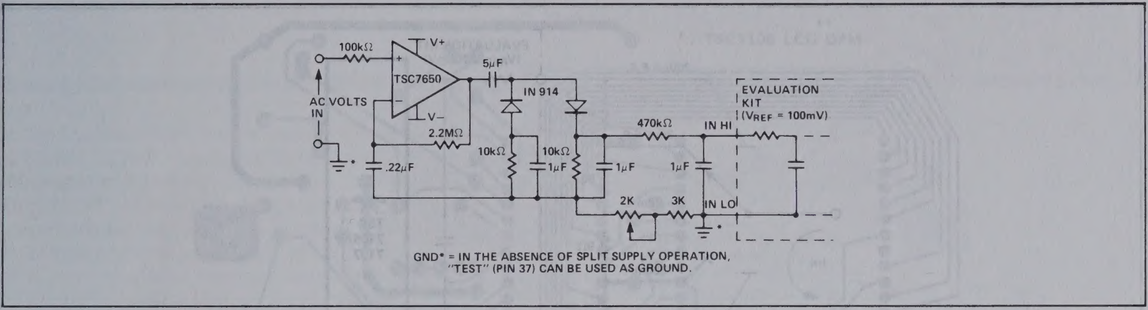
$$\text{Displayed Reading} = \frac{I_{IN} \times R_S}{V_{REF}} \times 1000$$

When measuring current the 199.9 mV scale is used. This limits the voltage drop to 100 µV per count. A multi-range current meter circuit is shown in Figure 15. Note that although the input current passes through the selector switch, IR drops across the switch do not contribute to the measured voltage.

Temperature Measurements

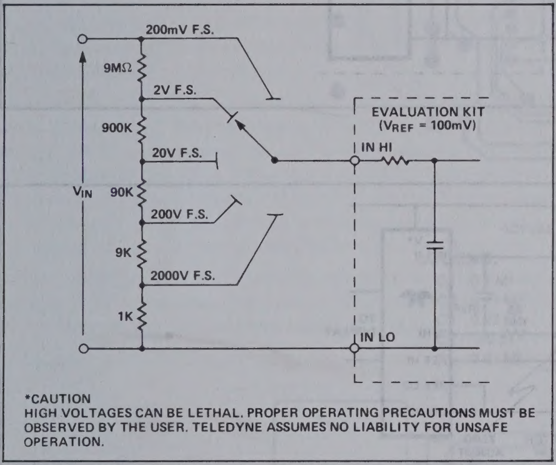
A diode connected transistor may be used as the temperature sensing element. V_{BE} has a temperature coefficient of -2.1 mV/°C. A scale factor of 0.1°C/count may be obtained by setting the reference at 210 mV.

At 0°C and 100µA bias current, the diode connected transistor will have a forward voltage drop of approximately 550 mV. A fixed 500 mV source is set up to offset the diode drop. In the circuit of Figure 16, adjust R5 to give 000.0 output reading with Q1 at 0°C. Then adjust for R4 for a 100.0 reading with Q1 at 100°C.


100kΩ
V+
TSC7650
5μF
AC VOLTS
IN
IN 914
V−
2.2MΩ
EVALUATION
KIT
(V_{REF} = 100mV)
470kΩ
IN HI
10kΩ
10kΩ
1μF
1μF
1μF
.22μF
2K
3K
IN LO

GND* = IN THE ABSENCE OF SPLIT SUPPLY OPERATION, "TEST" (PIN 37) CAN BE USED AS GROUND.

Figure 11: AC to DC Converter


200mV F.S.
9MΩ
2V F.S.
EVALUATION KIT
(V_{REF} = 100mV)
900K
IN HI
20V F.S.
V_{IN}
90K
200V F.S.
9K
2000V F.S.
1K
IN LO

*CAUTION
HIGH VOLTAGES CAN BE LETHAL. PROPER OPERATING PRECAUTIONS MUST BE OBSERVED BY THE USER. TELEDYNE ASSUMES NO LIABILITY FOR UNSAFE OPERATION.

Figure 12a: Multirange Voltmeter

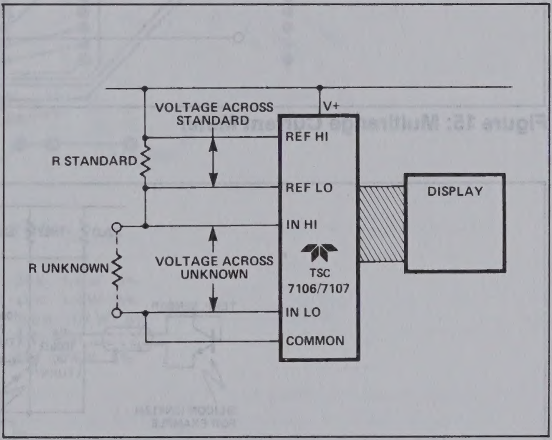
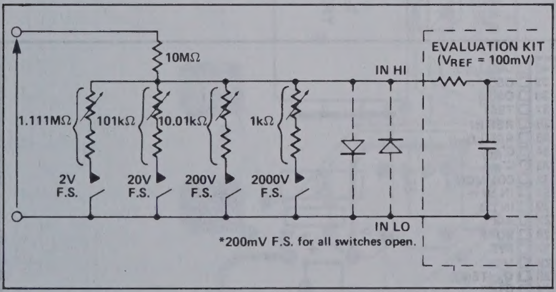

VOLTAGE ACROSS
STANDARD
V+
REF HI
R STANDARD
REF LO
DISPLAY
IN HI
R UNKNOWN
VOLTAGE ACROSS
UNKNOWN
TSC
7106/7107
IN LO
COMMON

Figure 13: Resistance Measurement*
(*Requires some modification to the kit)


10MΩ
EVALUATION KIT
(V_{REF} = 100mV)
IN HI
1.111MΩ
101kΩ
10.01kΩ
1kΩ
2V
F.S.
20V
F.S.
200V
F.S.
2000V
F.S.
IN LO

*200mV F.S. for all switches open.

Figure 12b: Multirange Voltmeter, Alternative Scheme

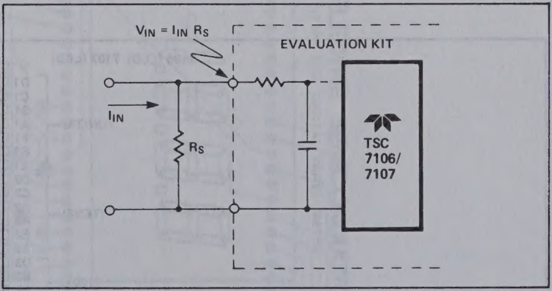

$V_{IN} = I_{IN} R_S$
EVALUATION KIT
I_{IN}
R_S
TSC
7106/
7107

Figure 14: Current Measurement

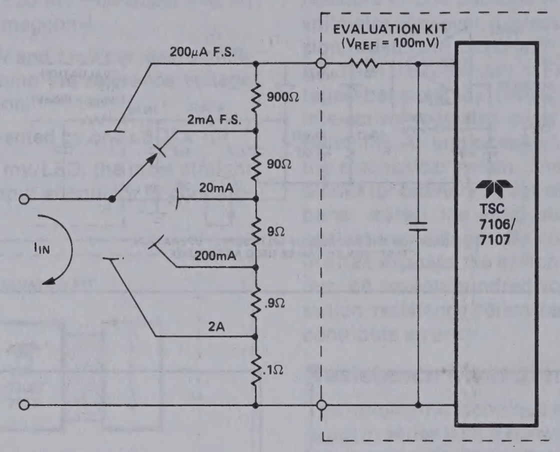

EVALUATION KIT
(V_{REF} = 100mV)
200µA F.S.
900Ω
2mA F.S.
90Ω
20mA
9Ω
200mA
.9Ω
2A
.1Ω
I_{IN}
TSC
7106/
7107

Figure 15: Multirange Current Meter

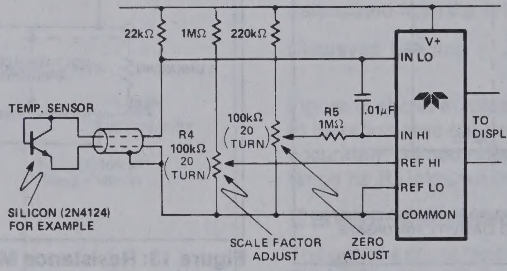
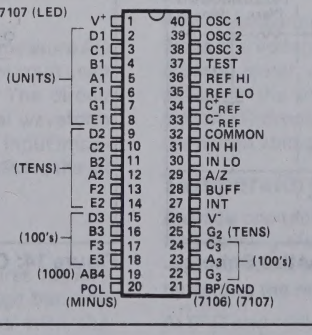
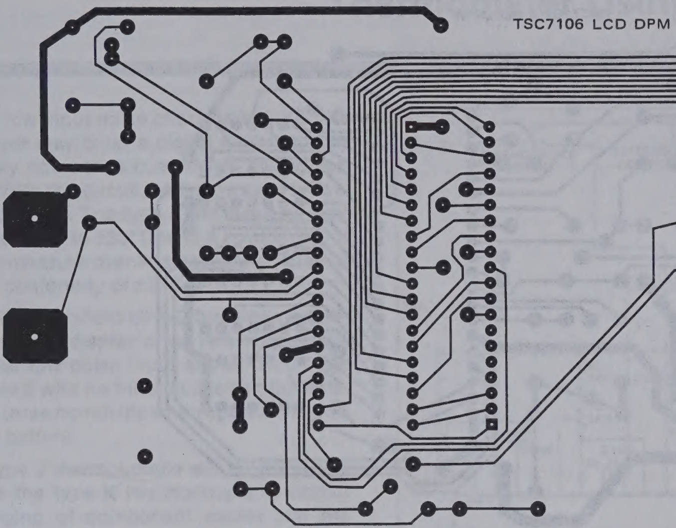

22kΩ
1MΩ
220kΩ
V+
IN LO
TEMP. SENSOR
100kΩ
20
TURN
R5
1MΩ
.01µF
IN HI
TO
DISPLAY
R4
100kΩ
20
TURN
REF HI
REF LO
COMMON
SILICON (2N4124)
FOR EXAMPLE
SCALE FACTOR
ADJUST
ZERO
ADJUST

Figure 16: Digital Thermometer*
(*Requires some modification to the kit)


7106 (LCD) 7107 (LED)
V+ 1
D1 2
C1 3
B1 4
(UNITS) A1 5
F1 6
G1 7
E1 8
D2 9
C2 10
B2 11
(TENS) A2 12
F2 13
E2 14
D3 15
B3 16
(100's) F3 17
E3 18
(1000) AB4 19
POL 20
(MINUS)
40 OSC 1
39 OSC 2
38 OSC 3
37 TEST
36 REF HI
35 REF LO
34 C+REF
33 C-REF
32 COMMON
31 IN HI
30 IN LO
29 A/Z
28 BUFF
27 INT
26 V-
25 G2 (TENS)
24 C3
23 A3 (100's)
22 G3
21 BP/GND
(7106) (7107)

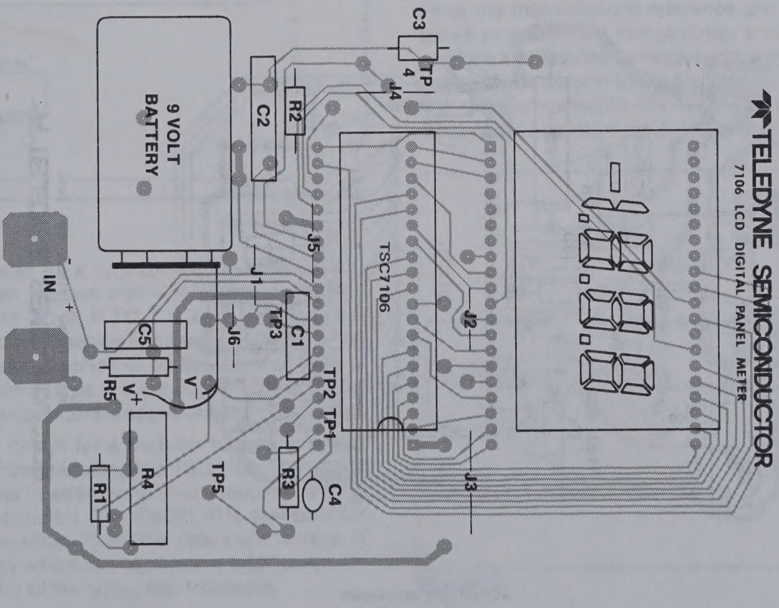
Pin Configuration


TSC7106 LCD DPM

ACTUAL SIZE NOT SHOWN

LEGEND:

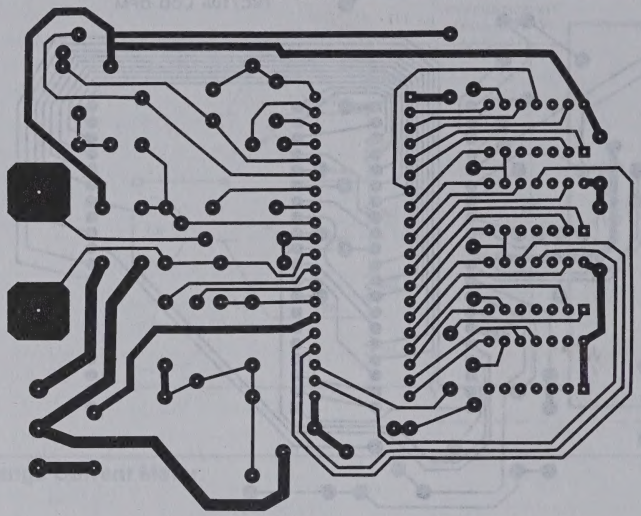
C1	0.1 Mf	R1	24 K 1/4 W 5%
C2	0.47 Mf	R2	47 K 1/4 W 5%
C3	0.22 Mf	R3	100 K 1/4 W 5%
C4	100 pf	R4	1 K POT
C5	0.01 Mf	R5	1 M 1/4 W 5%


C3
TP 4
J4
R2
C2
9 VOLT BATTERY
TSC7106
TELEDYNE SEMICONDUCTOR
7106 LCD DIGITAL PANEL METER
J5
J1
IN
+
TP3
C1
J6
C5
J2
R5
V+
V−
TP2
TP1
R4
R1
TP5
R3
C4
J3

ACTUAL SIZE NOT SHOWN

Figure 17: TSC7106 – Circuit Board Layout and Component Placement

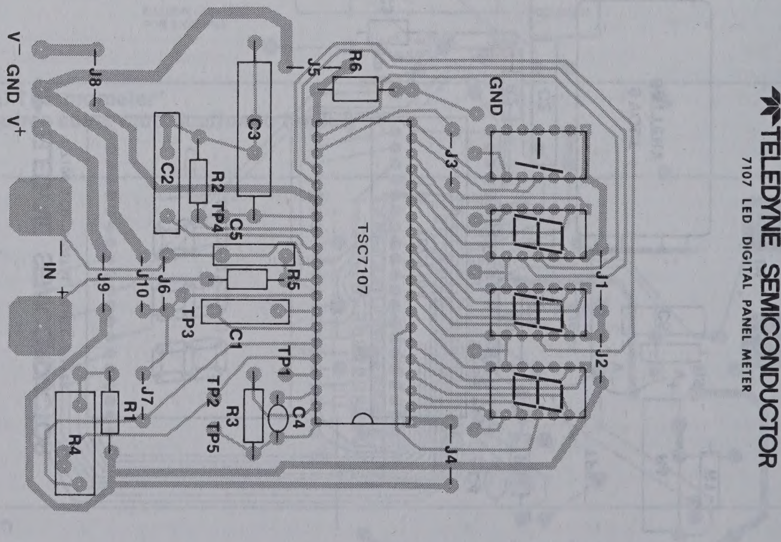
TSC7107 LED DPM



ACTUAL SIZE NOT SHOWN

LEGEND

C1	0.1 Mf	R1	24 K 1/4 W 5%
C2	0.47 Mf	R2	47 K 1/4 W 5%
C3	0.22 Mf	R3	100 K 1/4 W 5%
C4	100 pf	R4	1 K POT
C5	0.01 Mf	R5	1 M 1/4 W 5%
		R6	150 Ω 1/4 W 5%


V⁻ GND V⁺
J8
J5
R6
GND
J3
C3
C2
R2
TP4
C5
TSC7107
R5
J10
J6
J9
IN
TP3
C1
TP1
J1
J2
J7
R1
R4
TP2
R3
TP5
C4
J4
TELEDYNE SEMICONDUCTOR
7107 LED DIGITAL PANEL METER

ACTUAL SIZE NOT SHOWN

Figure 18: TSC7107 – Circuit Board Layout and Component Placement

TELEDYNE SEMICONDUCTOR

Application Note 12

A Single IC Digital Thermocouple Thermometer Using the TSC7106

By Al Kadis

Due to the extremely low input noise characteristics of the TSC7106/7107, the user may build a digital thermocouple thermometer with only one active component and fifteen passive components. With this circuit, both type J and type K thermocouples may be used. The type J will measure over the temperature range of 10 to 530° C with a conformity of ±2° C. The type K will measure over a temperature range of 0° C to 1000° C with a conformity of ±3° C.

In operation, the TSC7106 provides all A/D functions including seven segment decoder, display drive, reference, and a clock. True differential low noise input allows the bridge circuit shown in Figure 2 with no other active components. This circuit will give a three month life when operated from a normal alkaline 9 volt battery.

The circuit using a type J thermocouple will be discussed here. (The circuit for the type K thermocouple is similar except for the changing of component values and the replacement of the type J thermocouple with type K). The extremely low noise front-end of the TSC7106/7107 allows the IC to operate reliably at one-half its minimum reference voltage specifications, approximately 50 microvolts per count.

A thermocouple is made by the junction of two dissimilar metals. Figure 1 shows the type J (iron and constantan) thermocouple in a temperature measuring mode.

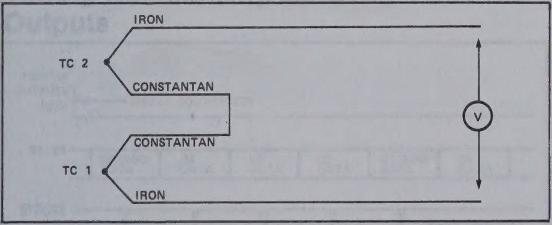

IRON
TC 2
CONSTANTAN
V
CONSTANTAN
TC 1
IRON

Figure 1.

A voltage is generated as a function of the difference in temperature between the two iron — constantan thermocouples — TC 1 and TC 2. If TC 1 is kept at a constant temperature (such as the freezing temperature of water), the voltage generated as a function of temperature of TC 2 is displayed in the normal type J thermocouple charts. The sensitivity at room temperature is approximately 50.4 µV/° C.

Figure 2 shows the circuit for a portable battery operated thermocouple thermometer using the TSC7106. The circuit uses six components in addition to those required for the standard TSC7106 circuitry. The TSC7106 is designed for normal 200 mV operation. Then the reference voltage is readjusted to 50.4 mV which corresponds to 1,000 times the one degree sensitivity of the type J thermocouple.

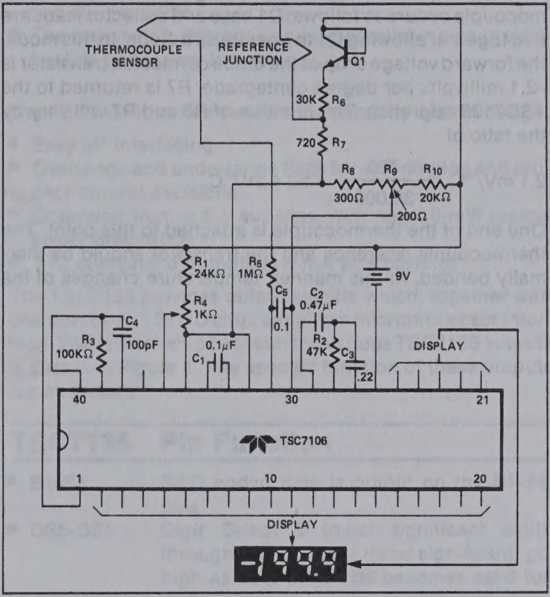

THERMOCOUPLE SENSOR
REFERENCE JUNCTION
Q1
30K R6
720 R7
R8 300Ω
R9 200Ω
R10 20KΩ
R1 24KΩ
R5 1MΩ
C5 0.1
C2 0.47µF
9V
R4 1KΩ
C4 100pF
R3 100KΩ
0.1µF C1
R2 47K
C3 .22
DISPLAY
40
30
21
TSC7106
1
10
20
DISPLAY
-199.9

Figure 2.

Since the thermocouple reference can not be easily maintained at a constant temperature, a circuit is used which provides a voltage that changes with temperature in an equal and opposite manner to the thermocouple. When combined with the thermocouple this has the effect of simulating the reference at a constant temperature over the normal ambient.

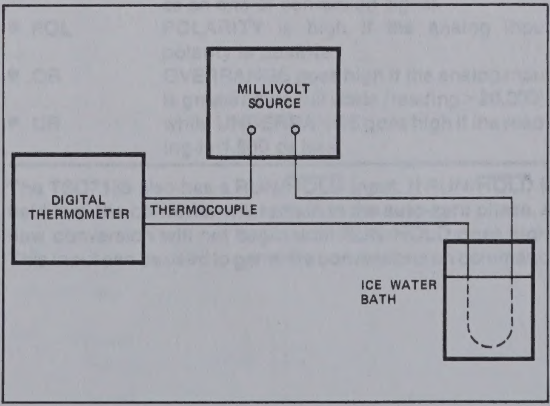

MILLIVOLT SOURCE
DIGITAL THERMOMETER
THERMOCOUPLE
ICE WATER BATH

Figure 3.

The circuit generating the compensating voltage is composed of Q1, R6 and R7. Q1 may be any small signal transistor.

A voltage equal and opposite to that generated by the thermocouple occurs as follows: Q1 base and collector leads are tied together allowing Q1 to operate as a diode. In this mode, the forward voltage drop of the diode connected transistor is -2.1 millivolts per degree centegrade. R7 is returned to the TSC7106 reference. The junction of R6 and R7 will vary by the ratio of

$$2.1\ \text{mV/°C}\ \frac{720}{30{,}000} = 50.4\ \mu\text{V/°C}.$$

One end of the thermocouple is attached to this point. The thermocouple reference and the transistor should be thermally bonded. In this manner, temperature changes of the thermocouple will be compensated by the transistor and resistor divider R6 and R7. R8, R9 and R10 form the other leg of a bridge. The 200 Ω pot (R9) center arm is fed to the negative or reference section of the input amplifier. The thermocouple output is fed to the positive section.

Calibration is accomplished by the use of an ice water bath and millivolt source as shown in Figure 3. The ice water bath is used as a O° C reference. The millivolt source is used to simulate thermocouple temperature over the range of 10 to 530° C. R9 is used for zero adjustment and R4 is used for full-scale. The thermocouple temperature curve is calibrated for best accuracy over the user's temperature range. Type K thermocouple is fabricated in a similar manner by changing the thermocouple type and resistor values and readjusting 0 and full-scale. The TSC7107 may also be used as a laboratory thermometer with similar circuitry.

TELEDYNE SEMICONDUCTOR

Application Note 16
TSC7135 Microprocessor Interface
By Wes Freeman

Many data acquisition systems require both a visual display and a computer interface. The TSC7135 from Teledyne Semiconductor is a 4-1/2 digit Analog-to-Digital converter (ADC) which can easily provide both of these functions. The TSC7135's multiplexed BCD outputs interface easily to low cost LED or LCD decoder/drivers, such as the TSC7211A (LCD) and TSC7212A (LED) or TSC700A (high-current LED). Also, the TSC7135's data outputs simplify computer interfacing.

This application note will present both the hardware and software required to interface the TSC7135 to a microprocessor. The circuit was developed for a 6502 μP and 6522 I/O port, but the design can easily be modified for other μPs and I/O ports.

The TSC7135 has several features which make it an attractive choice for data acquisition where speed is not an overriding consideration. The analog features include:

- High resolution .... 20,000 counts
- High accuracy .... ± 1 count
- Low roll-over error .... ± 1 count
- Valid polarity at 000 reading (the + and - zero states give an extra bit of resolution)
- Negligible zero drift - definitely not the case with a bipolar DAC/SAR type ADC

Timing Relationship Between TSC7135 Outputs

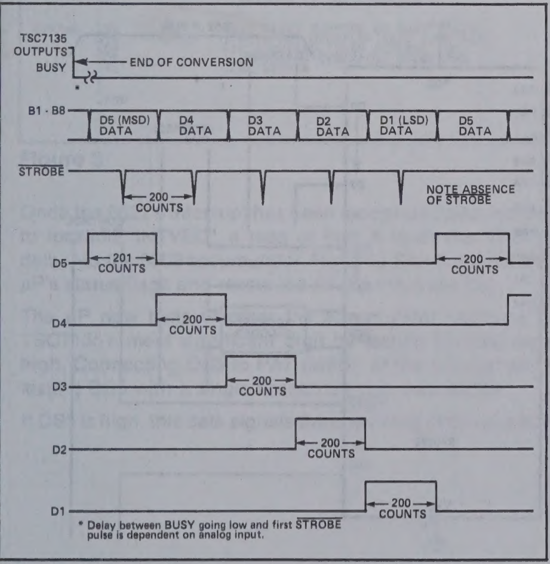


Figure 1

- The dual-slope conversion method rejects 50 Hz, 60 Hz, and 400 Hz noise.
- The ratiometric reference and differential inputs provide flexible transducer interfacing.

The TSC7135 also has features that simplify system design:

- Easy μP Interfacing
- Overrange and underrange flags for autoranging and process control decisions
- Operation from ± 5 V supplies, with only 10 mW typical power dissipation
- TTL compatible outputs (1.6 mA sink current)

The TSC7135 provides output signals which, together with one port of an LSI I/O chip, simplify a microprocessor interface. The relationship between the various TSC7135 outputs is shown in Figure 1. The specific function of these outputs are as follows:

TSC7135	Pin Function
• B1-B8	BCD coded data is output on the B1-B8 pins.
• DS5-DS1	Digit Select 5 (most significant digit) through Digit Select 1 (least significant) go high as data on B1-B8 becomes valid for that digit.
• $\overline{\text{STROBE}}$	For the first digit scan after a conversion $\overline{\text{STROBE}}$ goes low (for 1/2 clock period) in the middle of each digit strobe. After five pulses, $\overline{\text{STROBE}}$ stays high until the next conversion is complete.
• BUSY	BUSY is high while the TSC7135 is in Integrate or Deintegrate phases of a conversion. The falling of BUSY can, therefore, be used as an end of conversion signal.
• POL	POLARITY is high if the analog input polarity is positive.
• OR	OVERRANGE goes high if the analog input is greater than full scale (reading > 20,000), while UNDERRANGE goes high if the reading is 1,800 or less.
• UR	

The TSC7135 also has a RUN/$\overline{\text{HOLD}}$ input. If RUN/$\overline{\text{HOLD}}$ is held low, the converter will remain in the auto-zero phase. A new conversion will not begin until RUN/$\overline{\text{HOLD}}$ goes high. This input can be used to generate conversions on command.

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Interface Hardware

The complete TSC7135 to SYP6522 interface schematic is shown in Fiqure 2. BCD data, POL, OR, UR, and DS5 are connected to the 6522's PA0 through PA7 inputs. The TSC7135's $\overline{\text{STROBE}}$ output interrupts the microprocessor via the 6522's CA1 interrupt. RUN/$\overline{\text{HOLD}}$ can be controlled by programming CA2 as an output.

At first glance, the circuit may appear incomplete because digit selects DS4 through DS1 are not connected. However, DS5 is the only digit select required. As mentioned previously, there are only 5 $\overline{\text{STROBE}}$ pulses per conversion cycle, with the first $\overline{\text{STROBE}}$ occurring during DS5. The µP decodes the logical "AND" of DS5 and $\overline{\text{STROBE}}$ (DS5 · $\overline{\text{STROBE}}$) as a conversion complete signal.

If the µP finds (DS · $\overline{\text{STROBE}}$) true upon responding to an interrupt, an "end of conversion" is assumed and assembling of BCD data from the TSC7135 begins. Each of the next four interrupts will provide another BCD digit. The µP counts interrupts in a register and stores the corresponding BCD data in successive memory locations. After five $\overline{\text{STROBE}}$ pulses, all BCD data has been transferred to the µP and conversion is complete.

One constraint of this interface method is that the µP must respond to each digit's interrupt before the next digit becomes valid. The 6522's CA1 input can be programmed to latch data into Port A, as well as provide an interrupt to the µP. Since latched data remains valid until the next $\overline{\text{STROBE}}$ pulse, the µP has the full interval between $\overline{\text{STROBE}}$ pulses to service each interrupt. $\overline{\text{STROBE}}$ pulses are 200 clock cycles apart. A TSC7135 clock frequency of 100 kHz will allow the µP two milliseconds (10 µsec x 200 clock cycles) to respond to each interrupt without losing data.

Interface Software

Software for the TSC7135 to 6502 interface can be divided into three routines: (1) Programming the 6522's Port A for latched input and interrupt from pin CA1; (2) the interrupt service routine which actually acquires and stores BCD data from the TSC7135; (3) display or manipulation of the acquired data. Figure 3 is a 6502 assembly language listing of the first two routines. An interrupt service routine flow chart is shown in Figure 4. Since the end of a digit scan leaves 5 digits of BCD data in successive memory locations, the user will find the interface software easy to incorporate into a specific display or manipulation routine.

The 6522 I/O port must be programmed before data can be received from the TSC7135. The code in Figure 3, beginning at location "SET-UP", writes data into the 6522's control registers to enable the following functions: (1) Port A will be a latched input, controlled by input CA1; (2) CA2 will be an output, programmed high (TSC7135 in "RUN" mode); (3) Interrupt enabled on the falling edge of CA1. The function of data written to each 6522 register is defined in Figure 5.

When programmed for interrupt operation, the 6522 will pull its IRQ output low on the falling edge of each $\overline{\text{STROBE}}$ pulse from the TSC7135. Assuming interrupts are enabled, IRQ going low will cause the 6502 µP to load the address of an interrupt service routine from memory locations FFFE and

TSC7135 to 6502 µP Interface Schematic

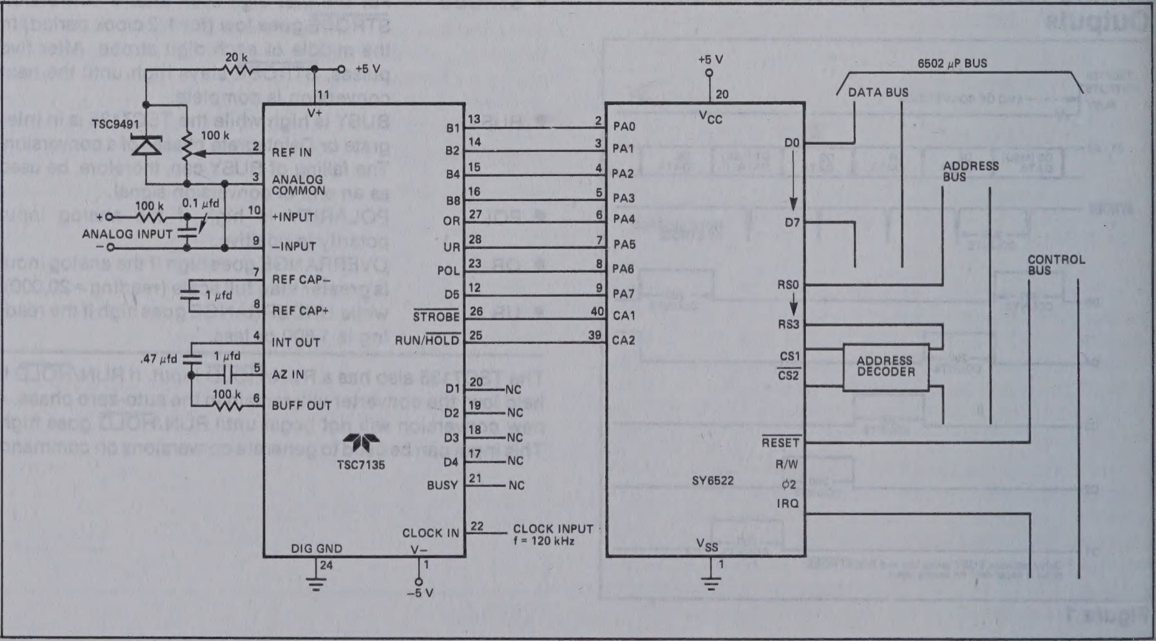

20 k
+5 V
11
V+
TSC9491
100 k
2
REF IN
3
ANALOG COMMON
100 k
0.1 µfd
+
ANALOG INPUT
−
10
+INPUT
9
−INPUT
7
REF CAP−
1 µfd
8
REF CAP+
4
INT OUT
.47 µfd
1 µfd
5
AZ IN
100 k
6
BUFF OUT
TSC7135
DIG GND
24
V−
1
−5 V
B1 13
B2 14
B4 15
B8 16
OR 27
UR 28
POL 23
D5 12
STROBE 26
RUN/HOLD 25
D1 20 NC
D2 19 NC
D3 18 NC
D4 17 NC
BUSY 21 NC
CLOCK IN 22
CLOCK INPUT
f = 120 kHz
+5 V
20
VCC
2 PA0
3 PA1
4 PA2
5 PA3
6 PA4
7 PA5
8 PA6
9 PA7
40 CA1
39 CA2
D0
D7
RS0
RS3
CS1
CS2
RESET
R/W
ϕ2
IRQ
SY6522
VSS
1
6502 µP BUS
DATA BUS
ADDRESS BUS
CONTROL BUS
ADDRESS DECODER

Figure 2

FFFF. This routine will typically identify the interrupting device, determine its priority and jump to a program to service the interrupt. The user must provide software to vector interrupts coming from the TSC7135 to the service routine located at location "INTVEC" of Figure 3. The TSC7135 - 6522 hardware can accommodate interrupt service delays of up to two msec, so a relatively low-priority interrupt status can be used.

6502 - Assembly Language Listing

```
        ;
        ;--------------------------------------------------
        ; TSC7135 INTERFACE TO A 6502 MICROPROCESSOR
        ;  USING A 6522 I/O PORT
        ;
        ; RESULTS ARE STORED IN 5 BYTES OF ZERO-PAGE
        ;  MEMORY, BEGINNING AT LOCATION "DIGSTOR"
        ;  (MOST SIGNIFICANT DIGIT FIRST)
        ;
        ; USER MUST PROVIDE INTERRUPT VECTOR FROM
        ;  THE 6522'S CA1 INTERRUPT TO A ROUTINE
        ;  AT "INTVEC"
        ;
        ;--------------------------------------------------
        ;
        ;SET UP 6522 FOR INTERRUPT OPERATION
        ;
IOPRT   .EQU    0A800   ;ADDRESS OF 6522 I/O PORT
SETUP   .EQU    028D    ;ADDR OF 6522 SET UP ROUTINE
        ;
        .ORG    SETUP
        LDA     #01     ;SET PORT A FOR
        STA     IOPRT+0B;LATCHED INPUT
        LDA     #0E     ;CA1=INT ON NEG EDGE
        STA     IOPRT+0C;CA2=HIGH (7135 IN "RUN" MODE)
        LDA     #082    ;ENABLE CA1 INTERRUPT
        STA     IOPRT+0E;
        JMP     MAINPRG ;I/O PORT SETUP COMPLETE, SO
                        ; JUMP TO OPERATING SYSTEM OR
                        ; TO MAIN PROGRAM
        ;
        ;
        ;BEGIN INTERRUPT SERVICE ROUTINE
        ;
XSTOR   .EQU    81      ;SAVE X REGISTER
DIGSTOR .EQU    82      ;SAVE RESULTS HERE
INTVEC  .EQU    02E0    ;6522'S CA1 INTERRUPT ROUTINE
        .ORG    INTVEC
        ;
        LDA     IOPRT+1 ;GET DIGIT FROM 6522
        BPL     NXTDIG  ;IF MSB=0, THIS IS NOT THE MOST
                        ; SIGNIF DIGIT. SO CONTINUE
        BIT     OVRBIT  ;CHECK FOR OVERRANGE
        BNE     OVRANG  ;BRANCH TO ERROR ROUTINE
        LDX     #00     ;SET THE DIGIT POINTER
        STX     XSTOR   ; AND STORE
        ;
NXTDIG  LDX     XSTOR     ;GET DIGIT POINTER
        STA     DIGSTOR,X ;STORE DIGIT IN ZERO PAGE
        INX               ; AND POINT TO
        STX     XSTOR     ;  THE NEXT DIGIT
        CPX     #05       ;5 DIGITS COMPLETES ONE SCAN
        BEQ     DONE      ;CONVERSION COMPLETE, PROCESS
                          ;OR DISPLAY DATA
                          ;THE 'DONE' ROUTINE MUST END WITH 'RTI'
        RTI               ;RETURN IF NOT COMPLETE
        ;
        ;
OVRANG  LDX     #01     ;SET DIGIT COUNTER SO THAT DIGITS
        STX     XSTOR   ; WILL NOT OVERFLOW ZERO PAGE MEM
        NOP             ;IF REQUIRED, USER PROGRAM FOR
        NOP             ; SERVICING OVERRANGE GOES HERE
        RTI             ;AND RETURN
        ;
        ;
        .END
```

Figure 3

Once the 6522's interrupt has been recognized and vectored to location "INTVEC", a read of Port A loads the TSC7135 data into the 6502 accumulator. Reading Port A also sets the μP's status flags and resets the 6522's interrupt flag.

The μP now tests whether the accumulator contains the TSC7135's most significant digit by testing for DS5 being high. Connecting DS5 to PA7 (MSB) of the I/O port allows testing DS5 with a single branch on plus instruction.

If DS5 is high, this data signals the beginning of a new display scan (i.e., an end of conversion has occurred.) The μP zeros its X index register, which will be used both to count the digits and to provide an offset for storing each digit in zero page memory. Register X is also stored in zero page memory at location XSTOR, since its contents will probably be lost upon returning from interrupt.

An early indication of an overrange condition can be obtained at this time. A bit mask, stored in memory, is used to test for the TSC7135's OVERRANGE output. If OR is high, the program branches to an error routine. An alternative for overrange testing is to wait until all digits have been scanned and then test bit 4 of any digit.

TSC7135 to 6502 μP Interface Program Flow Chart

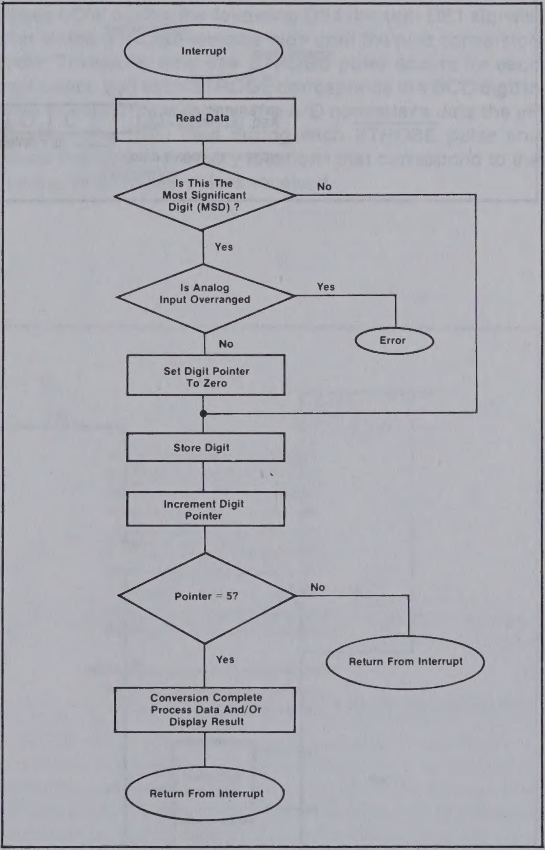
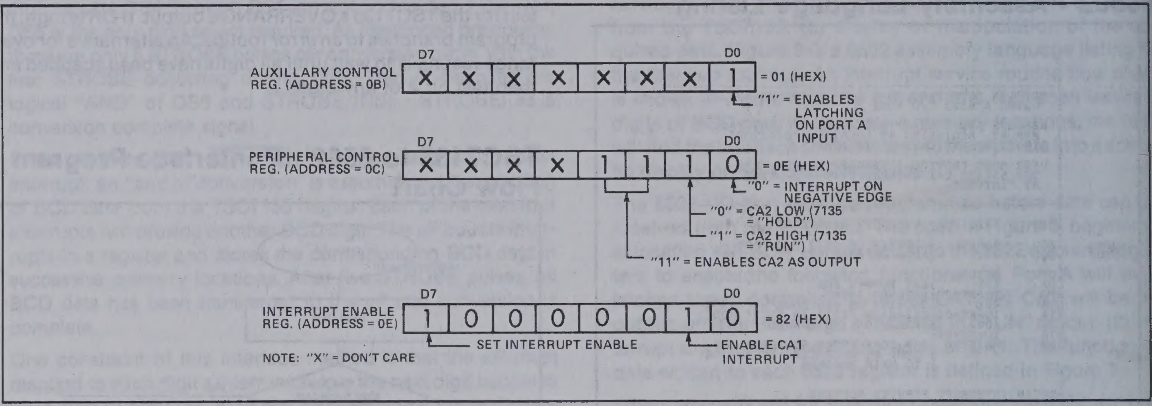

Interrupt
Read Data
Is This The Most Significant Digit (MSD) ?
No
Yes
Is Analog Input Overranged
Yes
Error
No
Set Digit Pointer To Zero
Store Digit
Increment Digit Pointer
Pointer = 5?
No
Return From Interrupt
Yes
Conversion Complete Process Data And/Or Display Result
Return From Interrupt

Figure 4

If DS5 is not high, or after register X is zeroed, program execution proceeds to location "NXTDIG". The BCD data is stored in zero page memory, beginning at location "DIGSTOR" and indexed by register X. After each digit is stored, register X is incremented and compared to five. If register X equals five, the digit scan is complete and data can be processed or displayed. Register X less than five indicates the digit scan is not complete, so an RTI instruction returns operation to the main program to await another digit strobe. Other programs can use memory location XSTOR as a "Data Valid" indication: if XSTOR = 5, then 5 consecutive memory locations begining at DIGSTOR contain the results of the latest TSC7135 conversion.

6522 I/O Port Control Register Functions



D7
D0
AUXILLARY CONTROL REG. (ADDRESS = 0B)
X X X X X X X 1
= 01 (HEX)
"1" = ENABLES LATCHING ON PORT A INPUT
D7
D0
PERIPHERAL CONTROL REG. (ADDRESS = 0C)
X X X X 1 1 1 0
= 0E (HEX)
"0" = INTERRUPT ON NEGATIVE EDGE
"0" = CA2 LOW (7135 = "HOLD")
"1" = CA2 HIGH (7135 = "RUN")
"11" = ENABLES CA2 AS OUTPUT
D7
D0
INTERRUPT ENABLE REG. (ADDRESS = 0E)
1 0 0 0 0 0 1 0
= 82 (HEX)
SET INTERRUPT ENABLE
ENABLE CA1 INTERRUPT
NOTE: "X" = DON'T CARE

TELEDYNE SEMICONDUCTOR

Application Note 17
Simplify A/D Converter Interface With Software
By Gary Grandbois & Wes Freeman

Integrating ADCs featuring BCD outputs for display interface offer a number of excellent features as well as high resolution at a very low cost. These advantages which include auto-zeroing, sign-magnitude coding, noise averaging and high impedance inputs are also attractive for microprocessor based systems. Unfortunately many of the display-oriented A/D converters are difficult to interface due to the multiplexed BCD format of the outputs. An exception to this problem is the 4 1/2 digit TSC7135 ADC which provides a "strobe" output.

This output allows the number of I/O port pins required to interface a 4 1/2 digit analog to digital converter chip to a microprocessor to be reduced from 15 lines (see ref.) to only 10 lines by counting the digit strobes in a software register. Besides freeing I/O pins for other applications, this method also results in slightly faster interrupt response because the μP does not have to loop while identifying each digit. Although the hardware and software shown are designed for the 8080, 8085 or Z-80, the same method can be applied to 6502 or 6800 I/O devices.

Interface Hardware

The complete TSC7135 to I8255A hardware interface is shown in Figure 1. The only digit strobe used is DS5 (the MSD), and the BUSY output is ignored. To understand why the other digit strobes are not required refer to the TSC7135 output timing diagram in Figure 2. The $\overline{\text{STROBE}}$ output goes low five times per conversion cycle. The first $\overline{\text{STROBE}}$ pulse occurs in the middle of DS5, when BCD data for the most significant digit is available on outputs B1-B8. $\overline{\text{STROBE}}$ also pulses LOW during the following DS4 through DS1 signals, after which $\overline{\text{STROBE}}$ remains high until the next conversion cycle. Therefore, only one $\overline{\text{STROBE}}$ pulse occurs for each digit select, and each $\overline{\text{STROBE}}$ corresponds to a BCD digit in MSD to LSD order. To read the A/D converter's data the μP simply reads BCD data during each $\overline{\text{STROBE}}$ pulse and stores that data in memory locations that correspond to the number of $\overline{\text{STROBE}}$ pulses received.

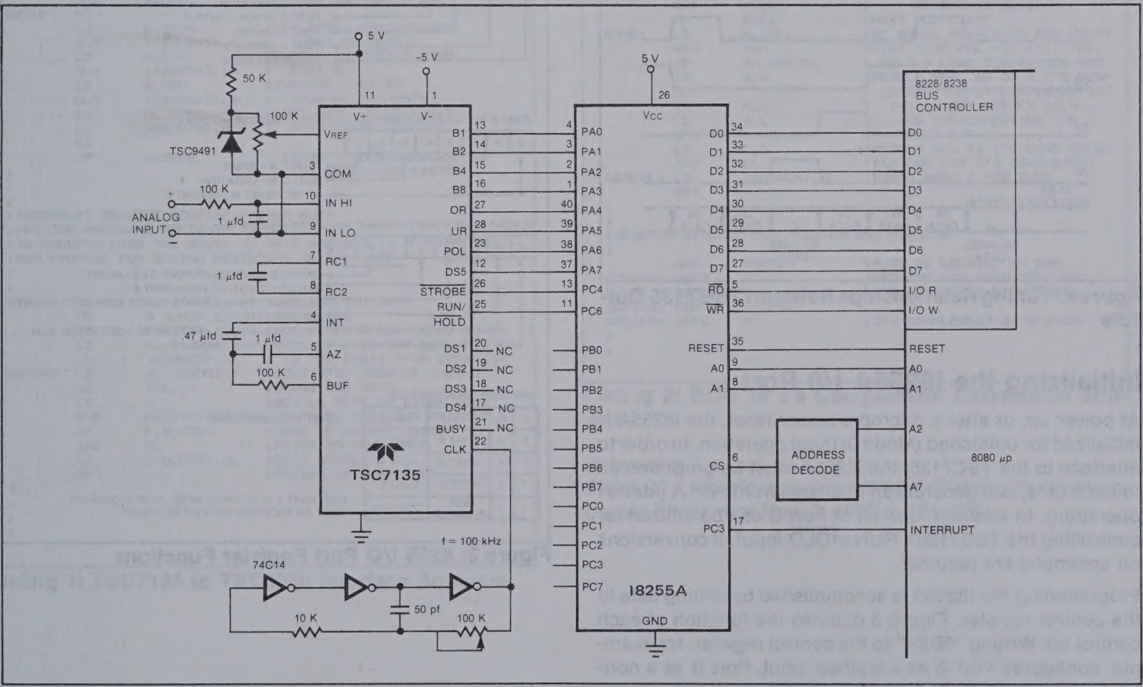

5 V
-5 V
50 K
100 K
TSC9491
100 K
ANALOG INPUT
+
.1 μfd
1 μfd
.47 μfd
1 μfd
100 K
V+
V-
VREF
COM
IN HI
IN LO
RC1
RC2
INT
AZ
BUF
B1
B2
B4
B8
OR
UR
POL
DS5
STROBE
RUN/HOLD
DS1
DS2
DS3
DS4
BUSY
CLK
NC
TSC7135
f = 100 kHz
74C14
50 pf
10 K
100 K
5 V
Vcc
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PC4
PC6
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC7
I8255A
GND
D0
D1
D2
D3
D4
D5
D6
D7
RD
WR
RESET
A0
A1
CS
PC3
ADDRESS DECODE
8228/8238 BUS CONTROLLER
I/O R
I/O W
A2
A7
INTERRUPT
8080 μp

Figure 1: TSC7135 to I/O Port Interface

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Synchronizing Data Transfer

The microprocessor must be able to identify an end-of-conversion, so that each digit will be stored in its proper location. Since the TSC7135 has a BUSY output, the processor could simply monitor this output for end-of-conversion status. However, this method would require an extra input bit, as well as processor time to test for BUSY status. By using software to identify the end-of-conversion, both software and hardware can be simplified.

In order to synchronize data transfer between μP and A/D converter, the μP tests the most significant bit of I/O port A for the presence of DIGIT STROBE 5(DS5). If DS5 is true then an end-of-conversion has occured. The data pointer is then initialized and assembly of five BCD digits begins. The next four $\overline{\text{STROBE}}$ pulses will find DS5 false, so the BCD digits are simply stored in successive memory locations. The fifth $\overline{\text{STROBE}}$ pulse signals an end of data transfer, so the user can display or manipulate the data as desired.

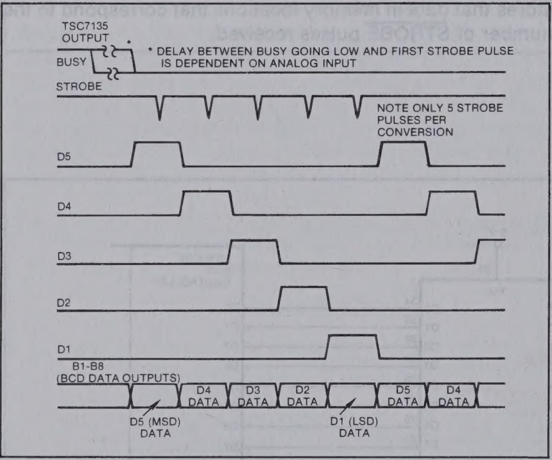

TSC7135
OUTPUT
BUSY
* DELAY BETWEEN BUSY GOING LOW AND FIRST STROBE PULSE IS DEPENDENT ON ANALOG INPUT
STROBE
NOTE ONLY 5 STROBE PULSES PER CONVERSION
D5
D4
D3
D2
D1
B1-B8
(BCD DATA OUTPUTS)
D4 DATA
D3 DATA
D2 DATA
D5 DATA
D4 DATA
D5 (MSD) DATA
D1 (LSD) DATA

Figure 2: Timing Relationships Between TSC7135 Outputs

Initializing the I8255A I/0 Port

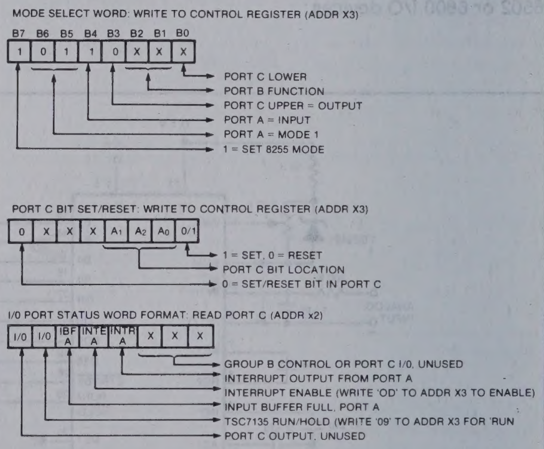
At power up, or after a microprocessor reset, the I8255A is initialized for unlatched (Mode 0) input operation. In order to interface to the TSC7135, the I8255A must be programmed to latch data, and generate an interrupt, from Port A (Mode I operation). In addition, one bit of Port C can be utilized for controlling the TSC7135's RUN/$\overline{\text{HOLD}}$ input, if conversions on command are required.

Programming the I8255A is accomplished by writing data to the control register. Figure 3 outlines the function of each control bit. Writing "0B2H" to the control register, for example, configures Port A as a latched input, Port B as a non-latched input, and remaining Port C bits as outputs.

In the Port A strobed input mode, bit PC3 becomes the interrupt output. In a large system with many interrupting devices, this output would typically go to a priority interrupt controller such as the I8259A. Smaller systems can simply use a single interrupt input, with polling in software to identify the source of the interrupt. To determine whether the TSC7135 has caused the interrupt in a polled system, Port A Input Buffer Full (IBFA) is tested for a HIGH state. If IBFA is high, then data has been latched into Port A by the TSC7135. Reading Port A will clear the interrupt and reset IBFA.

Programming Port A for strobed operation will define bit PC3 as an interrupt output, but a separate operation is required to enable the output. Bit PC4 is the interrupt enable bit for Port A. This bit must be set, using the Port C bit set/reset function, before the I8255A will respond to interrupts.

The circuit of Figure 1 also shows the TSC7135's RUN/$\overline{\text{HOLD}}$ input controlled by bit PC6. Setting PC6 high will result in continuous conversions. When PC6 is low, the TSC7135 will remain in its auto-zero cycle. If PC6 pulses high, the TSC7135 will perform a conversion, output the new data, and return to auto-zero.


MODE SELECT WORD: WRITE TO CONTROL REGISTER (ADDR X3)
B7 B6 B5 B4 B3 B2 B1 B0
1 0 1 1 0 X X X
PORT C LOWER
PORT B FUNCTION
PORT C UPPER = OUTPUT
PORT A = INPUT
PORT A = MODE 1
1 = SET 8255 MODE
PORT C BIT SET/RESET: WRITE TO CONTROL REGISTER (ADDR X3)
0 X X X A1 A2 A0 0/1
1 = SET, 0 = RESET
PORT C BIT LOCATION
0 = SET/RESET BIT IN PORT C
I/0 PORT STATUS WORD FORMAT: READ PORT C (ADDR x2)
I/0 I/0 IBF A INTE A INTR A X X X
GROUP B CONTROL OR PORT C I/0, UNUSED
INTERRUPT OUTPUT FROM PORT A
INTERRUPT ENABLE (WRITE 'OD' TO ADDR X3 TO ENABLE)
INPUT BUFFER FULL, PORT A
TSC7135 RUN/HOLD (WRITE '09' TO ADDR X3 FOR 'RUN
PORT C OUTPUT, UNUSED

8255 REGISTER ADDRESSES

A_1	A_0	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$
0	0	PORT A	PORT A
0	1	PORT B	PORT B
1	0	PORT C	PORT C*
1	1	NOT ALLOWED	CONTROL

NOTE: "X" = DON'T CARE

* WITH PORT A IN STROBED MODE, PORT C OUTPUTS MUST BE ACCESSED WITH BIT SET/RESET

Figure 3: 8255 I/O Port Register Functions

Interface Software

Listing 1 contains software for acquiring data from the A/D converter. Two separate routines are required to program the I/O port and to respond to interrupts. Code at location "SETUP" will configure the I8255A for strobed input and enable Port A's interrupt.

The user must provide software for vectoring interrupts from port A of the 8255A to interrupt service routine "SVC." As mentioned previously, "SVC" will test for digit strobe 5 being high (i.e. beginning of a new digit scan). If DS5 is high then data pointer HL is loaded with the digit storage address.

If DS5 is not high, or after HL has been initialized, the BCD digits are stored in memory. If five digits have not been received, register HL is incremented to point to the next digit storage location. After five STROBE pulses, locations STORAG through STORAG +4 will contain five BCD digits that represent the latest TSC7135 conversion, plus sign, polarity, overrange, and underrange flags.

```
;TSC7135 TO 8255 I/O PORT INTERFACE SOFTWARE, WITH
;SIGN-MAGNITUDE TO 2'S COMPLEMENT CONVERSION
;
;
;CONFIGURE PORT A OF 8255 FOR STROBED INPUT AND
;ENABLE INTERRUPT FROM PORT A
;
;
I8255:  EQU     0               ;8255 I/O PORT ADDRESS
        ORG     2000H           ;CAN BE IN ROM OR RAM
SETUP   DI
        LD      A,0B2H          ;SET 8255A FOR LATCHED
        OUT     (I8255+3),A     ;  INPUT ON PORT A
        LD      A,0DH           ;ENABLE INTERRUPT FROM
        OUT     (I8255+3),A     ;  PORT A
        LD      A,09H           ;TURN ON TSC7135
        OUT     (I8255+3),A     ;  (RUN/HOLD='RUN')
        LD      HL,STOR         ;LOAD DATA POINTER WITH
        LD      (COUNTR),HL     ;  DATA STORE ADDRESS
        EI
        JP      MAINPR              ;JUMP TO USER PROGRAM OR
;                                     TO OPERATING SYSTEM
;
;
;INTERRUPT SERVICE ROUTINE---USER MUST
;PROVIDE HARDWARE/SOFTWARE TO VECTOR
;INTERRUPTS FROM THE 8255A TO THIS ROUTINE,
;AND PROVIDE FOR SAVING REGISTERS AS REQUIRED
;
;
SVC:    IN      A,(I8255)       ;GET TSC7135 DATA
        OR      A               ;SET FLAGS
        JP      P,NXTDG         ;DS5=0;NOT A NEW SCAN, GO ON
        LD      HL,STOR         ;NEW SCAN, SO SET DATA POINTR
        LD      (COUNTR),HL     ; TO 1ST DIGIT STOR LOCATION
NXTDG:  LD      HL,(COUNTR)     ;LOAD STOR ADDR OF THIS DIGIT
        LD      (HL),A          ;STORE BCD DATA
        LD      A,L             ;GET LO BYTE OF STORE ADDR
        SUB     ENDSTR.MOD.256;SUBTRACT ENDING STOR ADDR-1
        JP      P,BCD2BI        ;DONE IF RESULT MINUS
        INC     HL              ;POINT TO NEXT ADDR
        LD      (COUNTR),HL     ;SAVE STORE ADDR
        RET                     ;RETURN TO MAIN PROG
;
;
;
;
```

Listing 1: TSC7135 to TSC8250 Interface Software

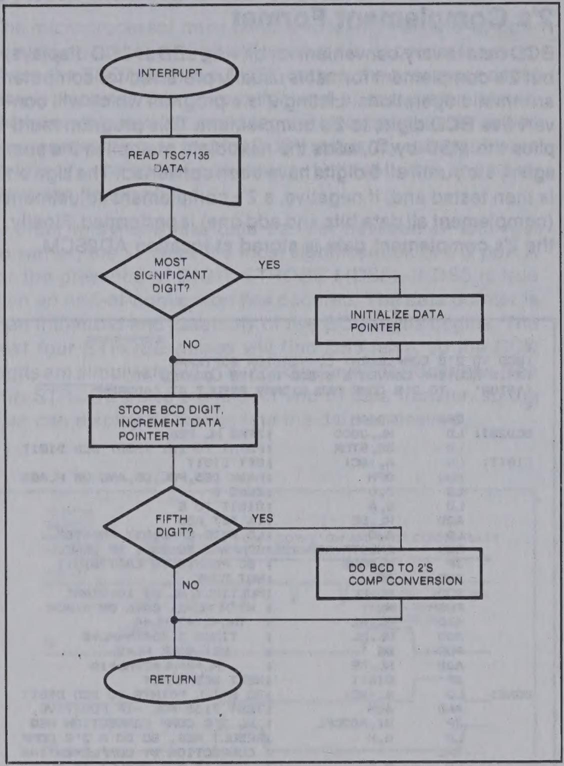
Converting Multiplexed BCD Numbers to 2's Complement Format

BCD data is very convenient for driving LED or LCD displays, but 2's complement format is usually preferred for computer arithmetic operations. Listing 2 is a program which will convert five BCD digits to 2's complement. This program multiplies the MSD by 10, adds the next digit, multiplies the sum again, etc., until all 5 digits have been converted. The sign bit is then tested and, if negative, a 2's complement adjustment (complement all data bits and add one) is performed. Finally, the 2's complement data is stored at location AD2SCM.

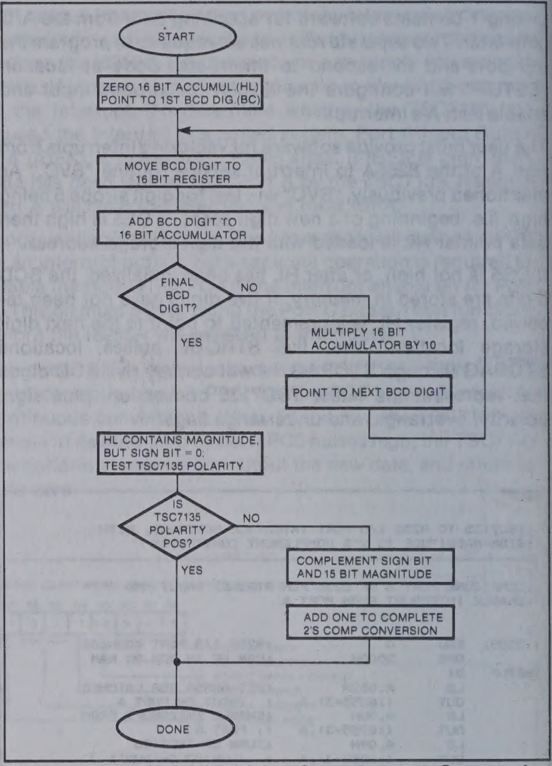
```
;
;BCD TO 2'S COMPLEMENT CONVERSION SOFTWARE
;THIS ROUTINE CONVERTS 5 BCD DIGITS LOCATED AT
;'STOR'   TO 2'S COMP AND STORES RESULT AT 'AD2SCM'
;
        ORG     2040H
BCD2BI: LD      HL,0000         ;ZERO HL REG
        LD      BC,STOR         ;POINT TO 1ST (MSD) BCD DIGIT
DIGIT:  LD      A,(BC)          ;GET DIGIT
        AND     0FH             ;MASK DS5,POL,OR,AND UR FLAGS
        LD      D,0             ;ZERO D
        LD      E,A             ;DIGIT TO E
        ADD     HL,DE           ;16 BIT ADD
        LD      A,C             ;LO BYTE OF DIGIT POINTER
        SUB     ENDSTR.MOD.256;COMPARE TO END; IF DONE,
        JP      P,DONE          ; BC POINTS TO LAST DIGIT
        INC     BC              ;NOT DONE
        ADD     HL,HL           ;MULTIPLY HL BY 10;START
        PUSH    HL              ; WITH HL*2; SAVE ON STACK
        ADD     HL,HL           ;   (HL*2)*2=HL*4
        ADD     HL,HL           ;    TIMES 2 AGAIN=HL*8
        POP     DE              ;     GET BACK HL*2
        ADD     HL,DE           ;      HL*8+HL*2=HL*10
        JP      DIGIT           ;NEXT BCD DIGIT
DONE:   LD      A,(BC)          ;BC STILL POINTS TO BCD DIGIT
        AND     40H             ;TEST 7135 POL -IF POSITIVE,
        JP      NZ,AD2CPL       ; NO 2'S COMP CORRECTION REQ
        LD      A,H             ;RESULT NEG, SO DO A 2'S COMP
        CPL                     ; CORRECTION BY COMPLEMENTING
        LD      H,A             ;  THE 15 BIT RESULT IN HL,
        LD      A,L             ;   AND COMPLEMENTING THE
        CPL                     ;     SIGN BIT
        LD      L,A             ;RESULT NOW IS 1'S COMP IN HL
        INC     HL              ;ADD ONE FOR 2'S COMPLEMENT
AD2CPL: LD      (AD2SCM),HL     ;STORE RESULT AND DONE
        RET
;
;
;RESERVE STORAGE FOR POINTER AND RESULTS
;
        ORG     0BFFCH          ;MUST BE LOCATED IN RAM
COUNTR: DEFS    2               ;STORAGE FOR DATA POINTER
STOR:   DEFS    5               ;STORAGE FOR 5 BCD DIGITS
ENDSTR: EQU     STOR+4
AD2SCM: DEFS    2               ;2'S COMPLEMENT DATA STOR
;
;
```

Listing 2: BCD to 2's Complement Conversion Software

Reference:
Smith, M.F. Interface program links A/D chip with microprocessor *Electronics* Nov. 3, 1982 p. 124, 125


INTERRUPT
READ TSC7135 DATA
MOST SIGNIFICANT DIGIT?
YES
INITIALIZE DATA POINTER
NO
STORE BCD DIGIT, INCREMENT DATA POINTER
FIFTH DIGIT?
YES
DO BCD TO 2'S COMP CONVERSION
NO
RETURN

Flowchart 1: "SVC" Interrupt Service Subroutine


START
ZERO 16 BIT ACCUMUL.(HL)
POINT TO 1ST BCD DIG.(BC)
MOVE BCD DIGIT TO 16 BIT REGISTER
ADD BCD DIGIT TO 16 BIT ACCUMULATOR
FINAL BCD DIGIT?
NO
MULTIPLY 16 BIT ACCUMULATOR BY 10
POINT TO NEXT BCD DIGIT
YES
HL CONTAINS MAGNITUDE, BUT SIGN BIT = 0; TEST TSC7135 POLARITY
IS TSC7135 POLARITY POS?
NO
COMPLEMENT SIGN BIT AND 15 BIT MAGNITUDE
ADD ONE TO COMPLETE 2'S COMP CONVERSION
YES
DONE

Flowchart 2: "BCD2B1" 2's Complement Conversion Subroutine

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Application Note 18
TSC7211AM/TSC7212AM
Display Driver Microprocessor Interface
By Wes Freeman

TSC7211AM/TSC7212AM Microprocessor Interface

The TSC7211AM and TSC7212AM are complete CMOS four-digit display drivers which greatly simplify microprocessor display interfaces. The devices contain data latches, BCD to seven-segment decoders, and either back plane and segment drivers for liquid crystal displays (TSC7211AM) or current controlled outputs for LEDs (TSC7212AM). This application note describes interfacing these display drivers to popular microprocessors.

TSC7211AM/TSC7212AM μP Interface Inputs

The TSC7211AM and TSC7212AM need only eight inputs to transfer data from a μP to the display. Inputs are divided into four data inputs, two address inputs, and two chip selects. Input timing relationships are shown in Figure 1.

BCD data for display is entered on inputs B0(LSB) through B3(MSB). Data inputs from 0000B through 1001B are decoded to correct seven-segment representation, while data inputs from 1010B to 1110B are decoded to "—," "E," "L," "P," and "H" respectively. An input of 1111B results in a blank display, which permits either individual digits or the entire display to be blanked under software control without external hardware.

The digit select inputs (DS1 and DS2) select the digit written to when the chip select inputs become active. Normally DS1 and DS2 are connected to the low-order bits (A0 and A1, respectively) of the microprocessor address bus. The DS1 and DS2 inputs must meet the same setup-and-hold-time limits as the data inputs.

Chip select inputs $\overline{CS1}$ and $\overline{CS2}$ control data entry into the TSC7211AM/TSC7212AM. The two chip selects are interchangeable, since they are logically "ORed" internally. In a typical application one chip select input connects to the READ/WRITE control line and the other chip select will connect to an address decoder. If only one chip select is required the remaining input should be tied to GND.

Microprocessor Bus Interfaces

Microprocessor bus structures can roughly be divided into two groups: the 6800-type, where data is guaranteed valid on a clock edge, and the 8080-type, where data is stable for the duration of a WRITE pulse. Since the TSC7211AM and TSC7212AM are specified in terms of data setup-and-hold-times, either processor type is easily accommodated.

The 6800-type edge activated I/O is used on several popular microprocessors, such as the 8048, 8085, 6809 and 6502. A timing diagram for the 6502 is shown in Figure 2, and a typical 6502 to TSC7211AM interface is shown in Figure 3. To transfer data to the display simply write data to the appropriate memory location.

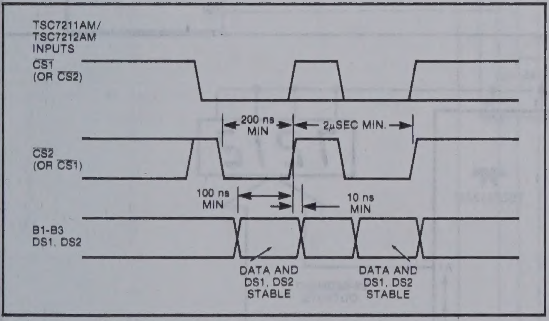


Figure 1. TSC7211AM/TSC7212AM Input Timing Diagram

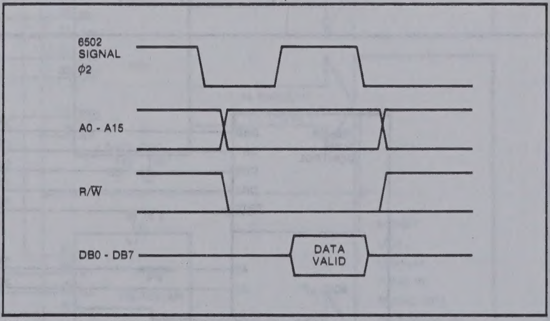


Figure 2. 6502 μP Output Timing Diagram

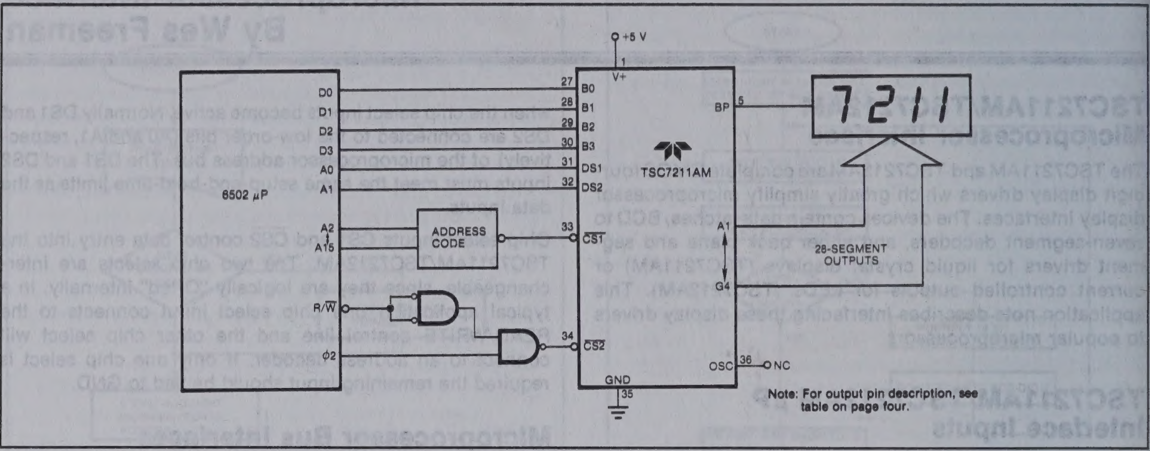

+5 V
1
V+
D0
D1
D2
D3
A0
A1
6502 μP
A2
A15
R/W
ϕ2
ADDRESS CODE
27
28
29
30
31
32
33
34
B0
B1
B2
B3
DS1
DS2
CS1
CS2
TSC7211AM
BP
5
A1
G4
28-SEGMENT OUTPUTS
OSC
36
NC
GND
35
7211
Note: For output pin description, see table on page four.

Figure 3. TSC7211AM Interface to 6502μP

The 8080 bus characteristics, shown in Figure 4, are shared by the Z-80, NSC800 and 8086, among others. A typical 8080 to TSC7212AM interface is shown in Figure 5, where the TSC7212AM is accessed as four I/O port locations. The 8080 can also treat the TSC7212AM as memory, in which case the full range of memory reference instructions can be used to transfer data to the display.

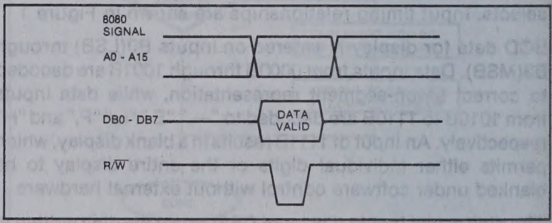

8080 SIGNAL
A0 - A15
DB0 - DB7
DATA VALID
R/W

Figure 4. 8080 μP Output Timing Diagram

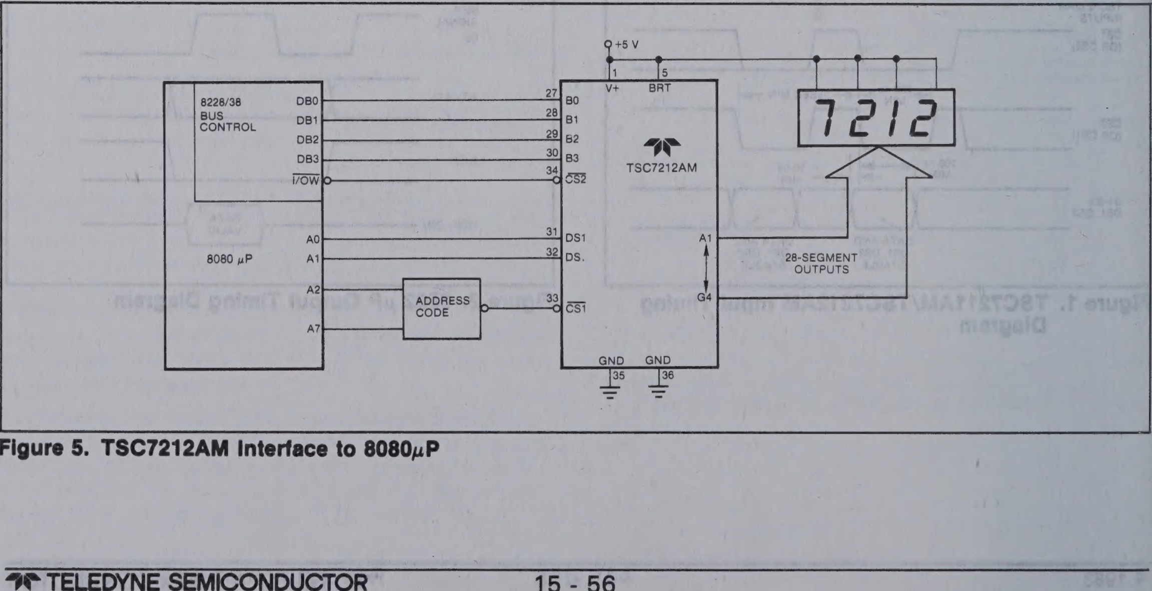

+5 V
1
5
V+
BRT
8228/38 BUS CONTROL
DB0
DB1
DB2
DB3
I/OW
8080 μP
A0
A1
A2
A7
ADDRESS CODE
27
28
29
30
34
31
32
33
B0
B1
B2
B3
CS2
DS1
DS.
CS1
TSC7212AM
A1
G4
28-SEGMENT OUTPUTS
7212
GND
35
GND
36

Figure 5. TSC7212AM Interface to 8080μP

Interfacing to Multiple LCD Displays

LCD displays will be damaged if the display driver causes a DC voltage between the backplane and segment inputs. Therefore, display driver outputs must be synchronized if more than one driver is used with a display. The TSC7211AM backplane outputs can be slaved together, permitting large LCD displays to be driven.

Figure 6, for example, shows three TSC7211AMs driving two six-digit LCD displays to produce a date/time display in MM:DD:YY, HH:MM:SS format. Since the backplane outputs are synchronized, each display can be driven by two separate TSC7211AMs without any display degradation. The processor shown is a Z-80, and the displays are accessed as twelve I/O port locations beginning at address 80H.

The Z-80 indirect output instruction (OUTI) efficiently transfers data from a twelve-byte buffer in memory to three TSC7211AMs. The OUTI instruction transfers the byte data addressed by registers H & L to the output port addressed by reg C, then increments register HL and decrements the buffer count register B. A typical output routine is:

```
Transfer  LD    C,7FH             ; 1st I/O address - 1
          LD    HL,
                Buffer Address    ; 1st byte of data
          LD    B, 12             ; Transfer 12 bytes
Loop1     INC   C                 ; Point to next I/O address
          OUTI                    ; Output byte; inc HL; dec B
          JR    NZ, Loop1         ; Next byte unless B = 0
```

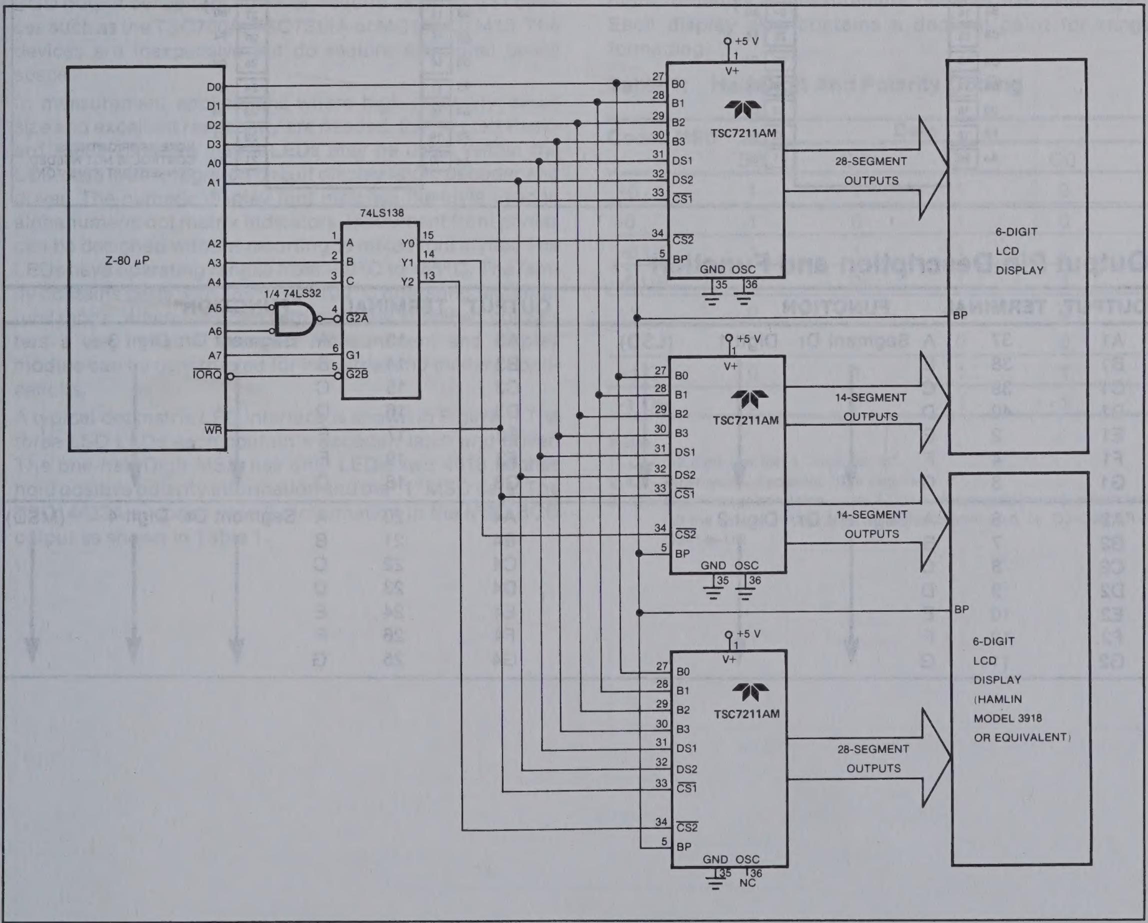
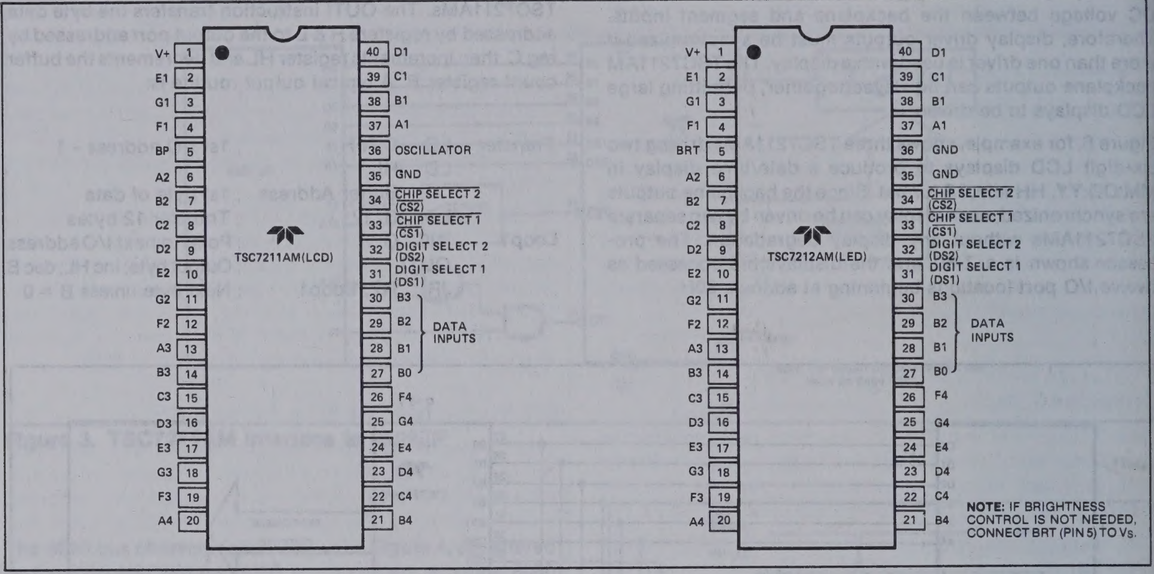

Z-80 μP
D0
D1
D2
D3
A0
A1
A2
A3
A4
A5
A6
A7
IORQ
WR
74LS138
1 A
2 B
3 C
4 G2A
6 G1
5 G2B
Y0 15
Y1 14
Y2 13
1/4 74LS32
+5 V
V+
1
27 B0
28 B1
29 B2
30 B3
31 DS1
32 DS2
33 CS1
34 CS2
5 BP
GND OSC
35 36
TSC7211AM
28-SEGMENT OUTPUTS
14-SEGMENT OUTPUTS
14-SEGMENT OUTPUTS
28-SEGMENT OUTPUTS
6-DIGIT LCD DISPLAY
BP
6-DIGIT LCD DISPLAY (HAMLIN MODEL 3918 OR EQUIVALENT)
NC

Figure 6. Multiple TSC7211AM Interface to Z-80 μP

TSC7211AM/TSC7212AM Pin Configuration


V+ 1
E1 2
G1 3
F1 4
BP 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
40 D1
39 C1
38 B1
37 A1
36 OSCILLATOR
35 GND
34 CHIP SELECT 2 (CS2)
33 CHIP SELECT 1 (CS1)
32 DIGIT SELECT 2 (DS2)
31 DIGIT SELECT 1 (DS1)
30 B3
29 B2
28 B1
27 B0
DATA INPUTS
26 F4
25 G4
24 E4
23 D4
22 C4
21 B4
TSC7211AM(LCD)
V+ 1
E1 2
G1 3
F1 4
BRT 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
40 D1
39 C1
38 B1
37 A1
36 GND
35 GND
34 CHIP SELECT 2 (CS2)
33 CHIP SELECT 1 (CS1)
32 DIGIT SELECT 2 (DS2)
31 DIGIT SELECT 1 (DS1)
30 B3
29 B2
28 B1
27 B0
DATA INPUTS
26 F4
25 G4
24 E4
23 D4
22 C4
21 B4
TSC7212AM(LED)

NOTE: IF BRIGHTNESS CONTROL IS NOT NEEDED, CONNECT BRT (PIN 5) TO Vs.

Output Pin Description and Function

OUTPUT	TERMINAL	FUNCTION	OUTPUT	TERMINAL	FUNCTION
A1	37	A Segment Dr. Digit 1 (LSD)	A3	13	A Segment Dr. Digit 3
B1	38	B	B3	14	B
C1	39	C	C3	15	C
D1	40	D	D3	16	D
E1	2	E	E3	17	E
F1	4	F	F3	19	F
G1	3	G	G3	18	G
A2	6	A Segment Dr. Digit 2	A4	20	A Segment Dr. Digit 4 (MSD)
B2	7	B	B4	21	B
C2	8	C	C4	22	C
D2	9	D	D4	23	D
E2	10	E	E4	24	E
F2	12	F	F4	26	F
G2	11	G	G4	25	G

TELEDYNE SEMICONDUCTOR

Application Note 19
BCD Analog-to-Digital Converter Interface to Dot Matrix LEDs
By David Gillooly

Traditionally 3 1/2 digit analog-to-digital converters have interfaced to seven segment LED or LCD displays. Converters like the TSC7106A, TSC7126A and TSC7107A contain decoder/driver circuits to directly drive seven segment displays. Devices like the TSC14433A and 4 1/2 digit TSC7135 offer users greater flexibility since decoder/drivers are not contained on-chip. Output data is in a multiplexed BCD format. Information can be displayed on LED, LCD, vacuum fluorescent or incandescent displays as the application and environment require. Information can simultaneously be transferred to a microprocessor.

The output data latching, decoding, and drive functions for BCD output converters,however, require external MSI devices such as the TSC700A, TSC7211A or MC14543/1413. The devices are inexpensive but do require additional board space.

In measurement applications where high reliability, small size and excellent readability are needed, the Hewlett Packard #5082-7356 dot matrix LEDs may be used. Within the LCD case is an integrated circuit display latch, decoder and driver. The numeric display font matches the style used in alphanumeric dot matrix indicators. Instrument front panels can be designed without resorting to mixed font styles. The LEDs have operating ranges from -20° C to +85° C. The family contains parts with -55° C to +100° C operating temperature range. When matched with similarly specified converters a very reliable, compact measurement and display module can be constructed for industrial and military applications.

A typical dot matrix LED interface is shown in Figure 1. The three LSD LEDs each contain a decoder, latch and driver. The one-half Digit MSD has only LEDs; two 4013 latches hold positive polarity information and the "1" MSD data. The TSC14433A encodes polarity information in the MSD BCD output as shown in Table 1.

In an overrange condition the data to the three LSDs is forced to all 1's through the 7432 OR gates. The HP#5082-7356 LED display blanks when an all 1's input is decoded. This added feature is at no additional cost since the gates are required as buffers to provide logic input drive to the LEDs. The MSD and sign bits are active in an overrange condition.

A slight modification (Figure 2) causes the three LSD displays to "blink" ON and OFF for overrange analog inputs. The overrange bit (OR) remains low until an in range conversion completes. With OR = O the Blink FF set is removed. The end-of-conversion (EOC) clock causes the display to blink at one-half the conversion rate. This visual blinking indicates more forcefully a measurement channel has overranged. Each display also contains a decimal point for range formatting.

Table 1: Half Digit And Polarity Coding

Coded MSD	Data			
	Q3	Q2	Q1	Q0
+0	1	1	1	0
-0	1	0	1	0
+0 UR	1	1	1	1
-0 UR	1	0	1	1
+1	0	1	0	0
-1	0	0	0	0
+1 OR	0	1	1	1
-1 OR	0	0	1	1

Notes
1. Q3- 1/2 digit, low for "1", high for "0"
2. Q2- Polarity: "1" = positive, "0" = negative
3. Q0- Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e. Q3=0→OR or Q3=1→UR.

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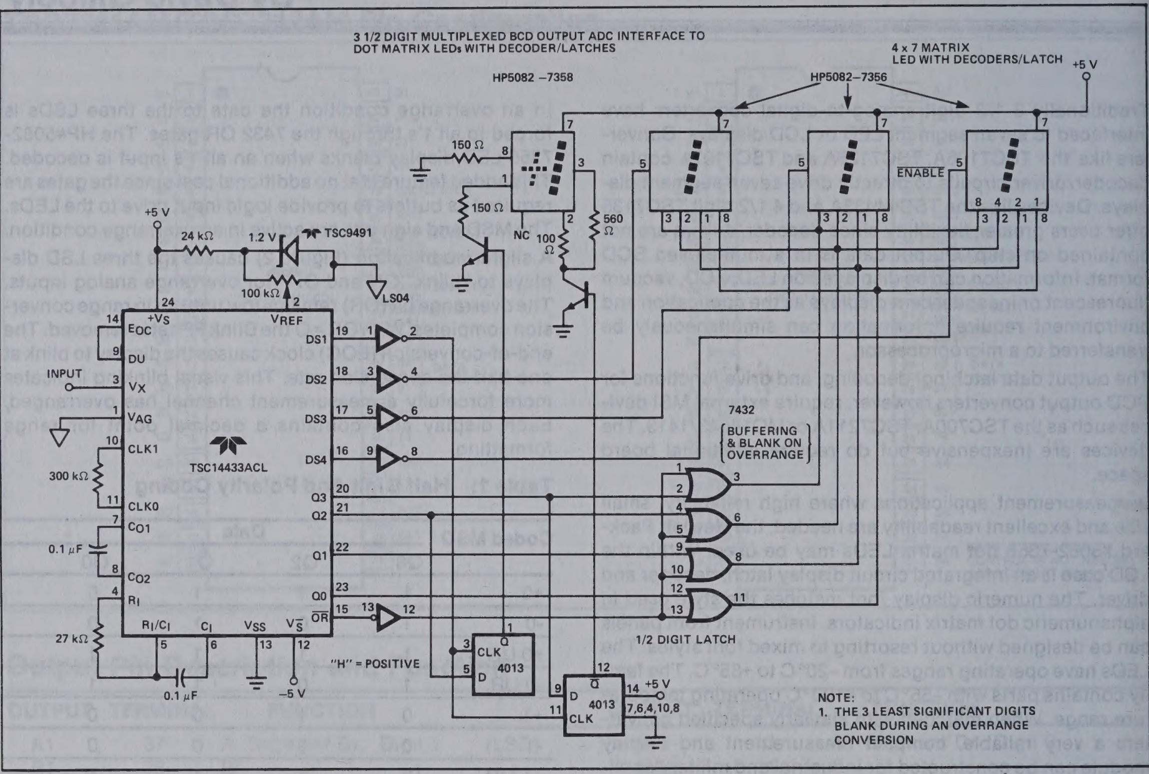
3 1/2 DIGIT MULTIPLEXED BCD OUTPUT ADC INTERFACE TO DOT MATRIX LEDs WITH DECODER/LATCHES
4 x 7 MATRIX LED WITH DECODERS/LATCH
HP5082 –7358
HP5082–7356
+5 V
ENABLE
150 Ω
150 Ω
560 Ω
100 Ω
NC
+5 V
24 kΩ
1.2 V
TSC9491
100 kΩ
LS04
INPUT
+VS
VREF
EOC
DU
VX
VAG
CLK1
CLKO
CO1
CO2
RI
RI/CI
CI
VSS
V$\bar{S}$
DS1
DS2
DS3
DS4
Q3
Q2
Q1
Q0
$\overline{OR}$
TSC14433ACL
300 kΩ
0.1 µF
27 kΩ
0.1 µF
–5 V
"H" = POSITIVE
7432
BUFFERING & BLANK ON OVERRANGE
1/2 DIGIT LATCH
4013
CLK
D
Q
$\bar{Q}$
14 +5 V
7,6,4,10,8
NOTE:
1. THE 3 LEAST SIGNIFICANT DIGITS BLANK DURING AN OVERRANGE CONVERSION

Figure 1: 3 1/2 Digit Multiplexed BCD Output ADC Interface to Dot Matrix LEDs with Decoder/Latches

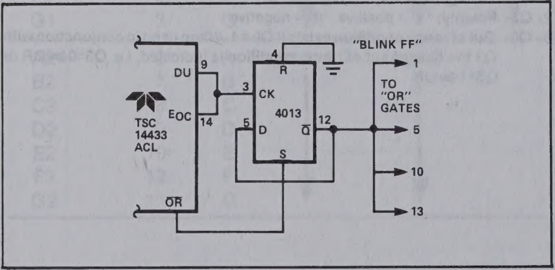
"BLINK FF"
DU
TSC 14433 ACL
EOC
$\overline{OR}$
R
CK
D
S
4013
$\bar{Q}$
TO "OR" GATES
1
5
10
13

Figure 2: Flashing Display on Overrange

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Application Note 20
Two-Digit Serial Input LED Display Driver Using TSC9404
By David Gillooly

Many system applications require microprocessors to display data on seven segment light emitting diode (LED) displays. To minimize the number of input/output lines needed, a serial to parallel data bit conversion scheme can be used. The TSC9404 will perform a serial to 16-bit parallel output conversion. The TSC9404 outputs will each sink 60 mA @ $V_{SAT} < 0.5$ V for directly driving the LED displays.

The sixteen outputs will drive two seven segment displays plus two decimal points or annunciators. A serial output allows devices to be cascaded for more digits. Two digits, however, are adequate for many event, switch position, percentage and temperature display applications.

A basic two digit display circuit is shown in Figure 1. The TSC9404 interfaces with a standard 6522 Versatile Interface Adapter (VIA) I/O chip. The 6522 communicates with a 6502 microprocessor. The VIA chip is widely used since it contains two configurable I/O ports, and timers. It also contains an 8-bit serial input/output shift register. The VIA shift register is configured as an output with the shift rate set by the phase 2 system clock. Data latches are not needed on the TSC9404 as the high speed data transfer is transparent to the eye. Two output shift operations will fill the TSC9404 with data for display.

Program operation is straight forward. (See program listing) The eight least significant data bits are loaded first from memory into the VIA shift register. The appropriate binary to seven segment display code is obtained through a table look-up (Table 1) procedure. The number stored in memory is the table offset. Hex or special symbol display characters are possible by expanding the table. The VIA automatically shifts eight data bits to the TSC9404. The program waits for a complete 8-bit transfer before obtaining the most significant digit data from memory. The wait state is implemented by testing the interrupt register shift complete flag bit with the shift register interrupt disabled. A memory map for the 6522 is shown in Table 2. The program/system was developed on a SYM-01 microcomputer board.

If decimal point drive is desirable the program is easily modified:

```
LDA   Table, X
ORA   LSBDP; Add #01 for decimal point
STA   SR
LDA   Table, X
ORA   MSBDP; Add #01 for decimal point
STA   SR
```

Similar programming techniques can be developed for alpha-numeric display using 14 or 16 segment LEDs. Bar graph displays are also possible.

Table 1: Decimal to Seven Segment Conversion Table

Displayed Character	LED Segment a b c d e f g DP	HEX Equivalent *
0	1 1 1 1 1 1 0 0	FC
1	0 1 1 0 0 0 0 0	60
2	1 1 0 1 1 0 1 0	DA
3	1 1 1 1 0 0 1 0	F2
4	0 1 1 0 0 1 1 0	66
5	1 0 1 1 0 1 1 0	B6
6	1 0 1 1 1 1 1 0	BE
7	1 1 1 0 0 0 0 0	E0
8	1 1 1 1 1 1 1 0	FE
9	1 1 1 0 0 1 1 0	E6
"BLANK"	0 0 0 0 0 0 0 0	00

* For decimal point add 01 to HEX code

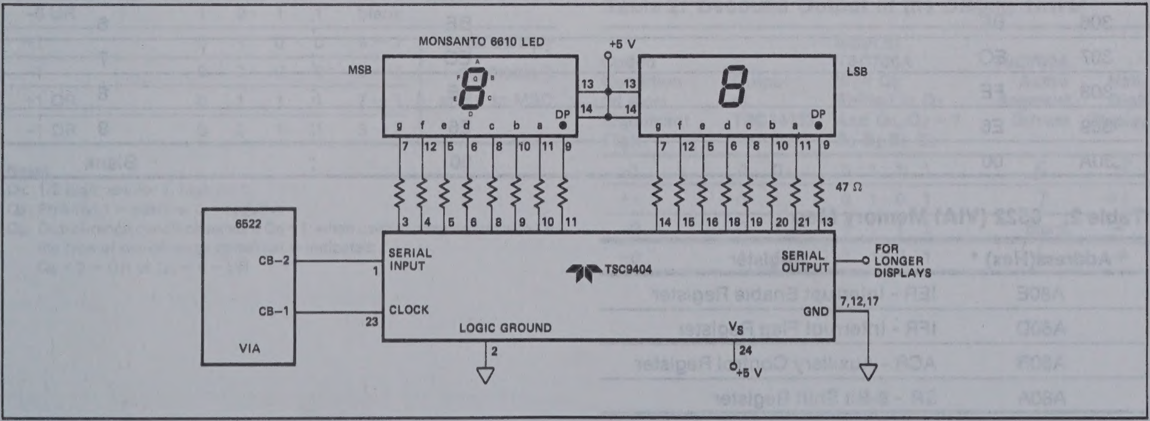

Figure 1: High Current Serial I/O Port Expander

Serial I/O Port Expander; Two Digit, Seven Segment LED Drive Program Listing

Address	Instructions Byte 1	 Byte 2	 Byte 3	Label	Mnemonic	Operand	Comments
200	A9	18		Display	LDA	#18	
202	8D	OB	A8		STA	ACR	; Shift out under $_2$ Control
205	A9	80			LDA	#80	
207	8D	OE	A8		STA	IER	; Disable shift register Interrupt
20A	AE	50	03		LDX	LSB	
20D	BD	00	03		LDA	Table,X	; Convert LSB decimal digit to seven segment code
210	8D	OA	A8		STA	SR	; Send LSB to shift register
213	AD	OD	A8	LSBTST	LDA	IFR	; Load shift register flag
216	29	04			AND	MASK	
218	FO	F8			BEQ	LSBTST	; Test for LSB shift completion
21A	AE	51	03		LDX	MSB	
21D	BD	00	03		LDA	Table,X	; Convert MSB decimal digit to seven segment code
220	8D	OA	A8		STA	SR	; Send MSB to shift register
223	AD	OD	A8	MSBTST	LDA	IFR	; Load shift register flag
226	29	04			AND	MASK	
228	FO	F8			BEQ	MSBTST	; Test for MSB shift completion
22A	60				RTS		; Return from subroutine
300	FC			Table		FC	; Seven segment code 0
301	60					60	; 1
302	DA					DA	; 2
303	F2					F2	; 3
304	66					66	; 4
305	B6					B6	; 5
306	BE					BE	; 6
307	EO					EO	; 7
308	FE					FE	; 8
309	E6					E6	; 9
30A	00					00	; Blank

Table 2: 6522 (VIA) Memory Map

Address(Hex) *	Register
A80E	IER - Interrupt Enable Register
A80D	IFR - Interrupt Flag Register
A80B	ACR - Auxiliary Control Register
A80A	SR - 8-Bit Shift Register

U28 On SYM-01 Single Board Computer

TELEDYNE SEMICONDUCTOR

Application Note 21
TSC700A Drives LED Display for TSC14433 ADC
By Wes Freeman

The TSC700A high current driver chip can demultiplex the TSC14433 3 1/2 digit analog to digital converter data lines and drive an LED display. Because the driver powers the LED statically, the high transient currents associated with multiplexed LEDs are reduced. As a result, the design eases power supply and component layout requirements and minimizes the noise at the input.

An added feature of the TSC700A is the guaranteed 11 mA minimum LED drive current. This is over twice the current available from comparable drivers. LEDs driven by the TSC700A will be very bright and readable, an important consideration when instruments use large character height displays or operate in high ambient light environments.

The TSC14433 is a 3 1/2 digit A/D converter which outputs data via four output pins (Q_0 - Q_3) and four data strobes (DS1 - DS4). The TSC700A contains four sets of 4-bit latches, BCD to 7-segment decoders, and static LED drivers with 11 mA current sink capability.

Circuit operation for the three least-significant digits is straightforward. The TSC14433 puts data on the Q_0 - Q_3 outputs and the appropriate digit strobe goes high, latching data into the TSC700A.

Table 1: TSC14433 Data Output

Coded Condition of Most Significant Digit (MSD)	Q_3	Q_2	Q_1	Q_0	Binary-coded-Decimal-to-Seven-Segment Decoding	
+0	1	1	1	0	blank	
-0	1	0	1	0	blank	
+0 UR	1	1	1	1	blank	
-0 UR	1	0	1	1	blank	
+1	0	1	0	0	4 → 1	hook up only segments b and c to MSD
-1	0	0	0	0	0 → 1	
+1 OR	0	1	1	1	7 → 1	
-1 OR	0	0	1	1	3 → 1	

Notes:

Q_3: 1/2 digit, low for 1, high for 0

Q_2: Polarity: 1 = positive, 0 = negative

Q_0: Out-of-range condition exists if $O_0 = 1$; when used in conjunction with Q_3 the type of out-of-range condition is indicated; $Q_3 = 0 \rightarrow$ OR or $Q_3 = 1 \rightarrow$ UR

Obtaining the proper data for the half digit and polarity sign is more complex. Truth table 1 shows the TSC14433 data output when DS1 goes high. The data format was designed to be used with a discrete polarity-driver transistor and a BCD to 7-segment decoder that blanks the display when an invalid BCD digit is input. Only Q_3 and Q_2 are significant for the half-digit display, however, so a combination of these signals can be found to light the proper segments of the TSC700A.

Truth table 2 shows the TSC700A display that results when Q_2 of the TSC14433 is inverted and shifted to Q_1, and Q_0 and Q_2 are always high. If outputs A1 and C1 of the TSC700A are used to light the half digit, and output F1 lights the positive polarity indicator, then additional external LED drivers are not required.

In the circuit, Q2 is inverted by one half of the CD4013B D-type flip-flop and is then shifted to Q1 by the 74C157 quad 2-input multiplexer. When DS1 is low data passes through the multiplexer unchanged. With DS2 high, the inverted Q2 comes out instead on 2Y and both 1Y and 3Y are set high. The TSC700A decodes the inputs as shown in truth table 2 and the correct segments turn on. Because no segment is "on" for all possible inputs an external resistor is required to turn on the "—" segment of the polarity sign.

A flashing display is useful for indicating overrange, and can be implemented with the remaining 4013 flip-flop. Normally the OR output (pin 15) of the TSC14433 keeps the flip-flop reset, enabling the TSC700A display. An analog input exceeding full-scale causes OR to go low, removing the reset. The flip-flop now toggles at the end of each conversion, causing the display to flash.

Table 2: Decoded Output of the Display Driver

Coded Condition Of Most Significant Digit	Output of TSC14433 Q_3	Q_2	Input to TSC700A With Q_2 Shifted to Q_1 And Q_0, $Q_2 = 1$ B_3	B_2	B_1	B_0	TSC700A Active Segment Drivers	Half-Digit Display
-1	0	0	0	1	1	1	5	-1
+1	0	1	0	1	0	1	7	+1
-0	0	1	1	1	1	1	blank	-
+0	1	1	1	1	0	1	L	+

TSC700A Drives LED Display for TSC14433 ADC

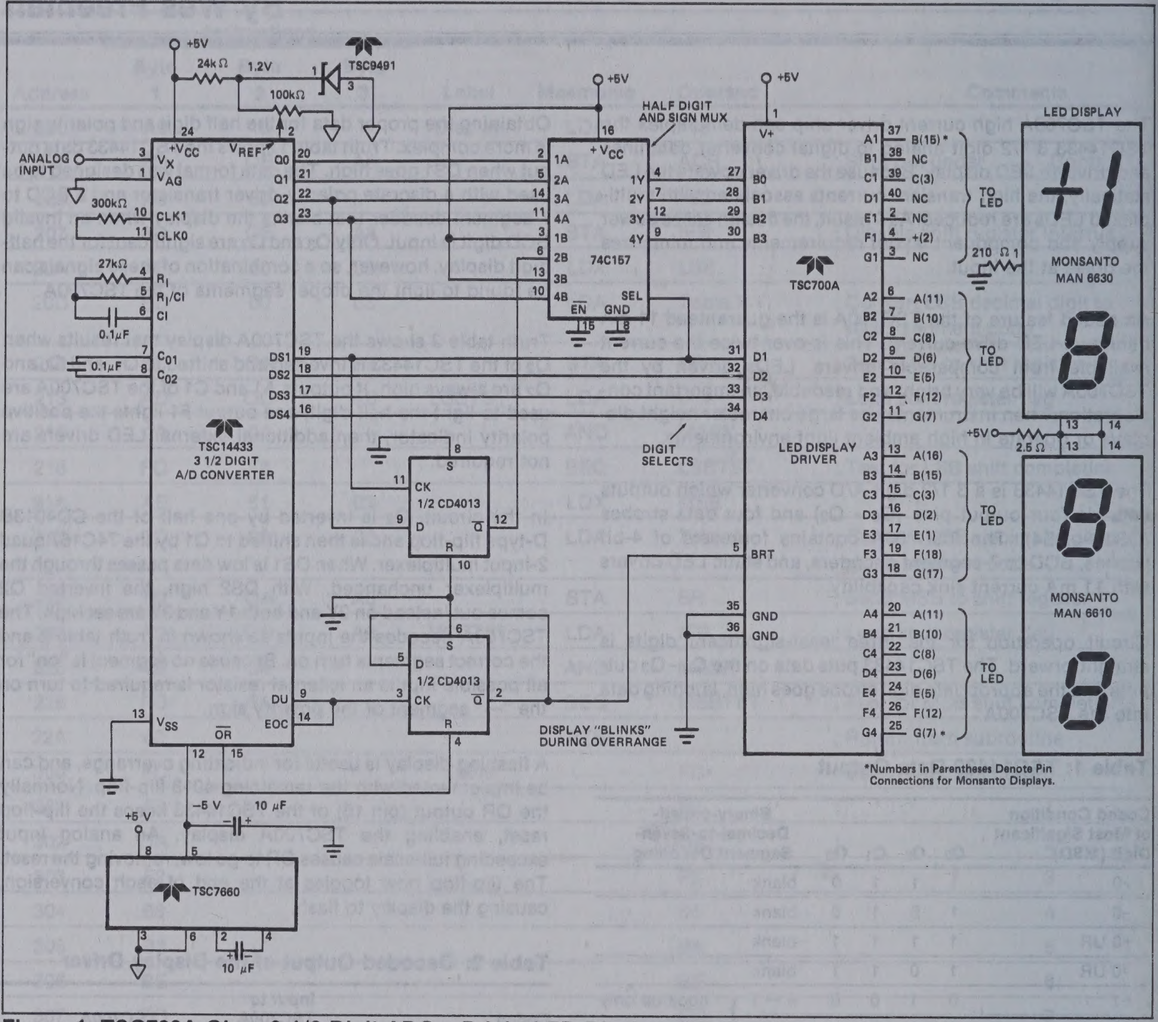
+5V
24kΩ
1.2V
TSC9491
100kΩ
24
+VCC
VREF
ANALOG INPUT
VX
VAG
300kΩ
CLK1
CLK0
27kΩ
RI
RI/CI
CI
0.1µF
CO1
CO2
Q0
Q1
Q2
Q3
DS1
DS2
DS3
DS4
TSC14433
3 1/2 DIGIT
A/D CONVERTER
DU
EOC
VSS
OR
-5 V
10 µF
+5 V
TSC7660
10 µF
HALF DIGIT AND SIGN MUX
+VCC
1A
2A
3A
4A
1B
2B
3B
4B
1Y
2Y
3Y
4Y
74C157
SEL
EN
GND
1/2 CD4013
S
CK
D
Q̄
R
DISPLAY "BLINKS" DURING OVERRANGE
DIGIT SELECTS
LED DISPLAY DRIVER
V+
B0
B1
B2
B3
D1
D2
D3
D4
BRT
GND
TSC700A
A1
B1
C1
D1
E1
F1
G1
A2
B2
C2
D2
E2
F2
G2
A3
B3
C3
D3
E3
F3
G3
A4
B4
C4
D4
E4
F4
G4
B(15)*
NC
C(3)
+(2)
A(11)
B(10)
C(8)
D(6)
E(5)
F(12)
G(7)
A(16)
B(15)
C(3)
D(2)
E(1)
F(18)
G(17)
G(7)*
TO LED
210 Ω
2.5 Ω
LED DISPLAY
MONSANTO MAN 6630
MONSANTO MAN 6610
*Numbers in Parentheses Denote Pin Connections for Monsanto Displays.

Figure 1: TSC700A Gives 3 1/2 Digit ADC a Bright LED Display with Flashing Display on Overrange

Application Note 22

Software Combines With CMOS LSI to Form 3 3/4 Digit DVM

By Wes Freeman

Single chip analog-to-digital (A/D) converters, with on-chip LCD or LED display drivers, have greatly simplified the design of sensor-to-human interfaces. However, the 3 1/2 digit resolution (1,999 counts) typically offered is often inadequate. In particular, temperature systems suffer from a limit of 199.9 degrees farenheit with 0.1 degree resolution. In addition, direct drive outputs of single-chip converters make a microprocessor interface, which is often required for process control, very difficult. Finally, display A/D converters are usually limited to about three readings per second, which is sometimes too slow for systems applications.

By combining a 13-bit, microprocessor-compatible, CMOS-LSI A/D converter with software and a CMOS display driver, you can expand the system's measurement range to "3 3/4" digits (4095 counts). This system retains the low cost, low power, high accuracy and excellent noise rejection of the integrating A/D converter, while providing both sign-magnitude binary and BCD data. In addition, the system A/D converter can operate at speeds up to 30 readings per second. Also, all of the interface functions can be performed by only one LSI microprocessor interface chip. Hardware and software shown are for a 6502 microprocessor, but other processor/interface devices can also be accommodated.

The hardware of the circuit is straightforward. Both A/D converter U2 and display driver U3 are interfaced to the microprocessor via U1, a "versatile interface adapter" with 20 I/O lines. When the falling edge of U2's status output indicates an end of conversion, U1 generates an interrupt. The

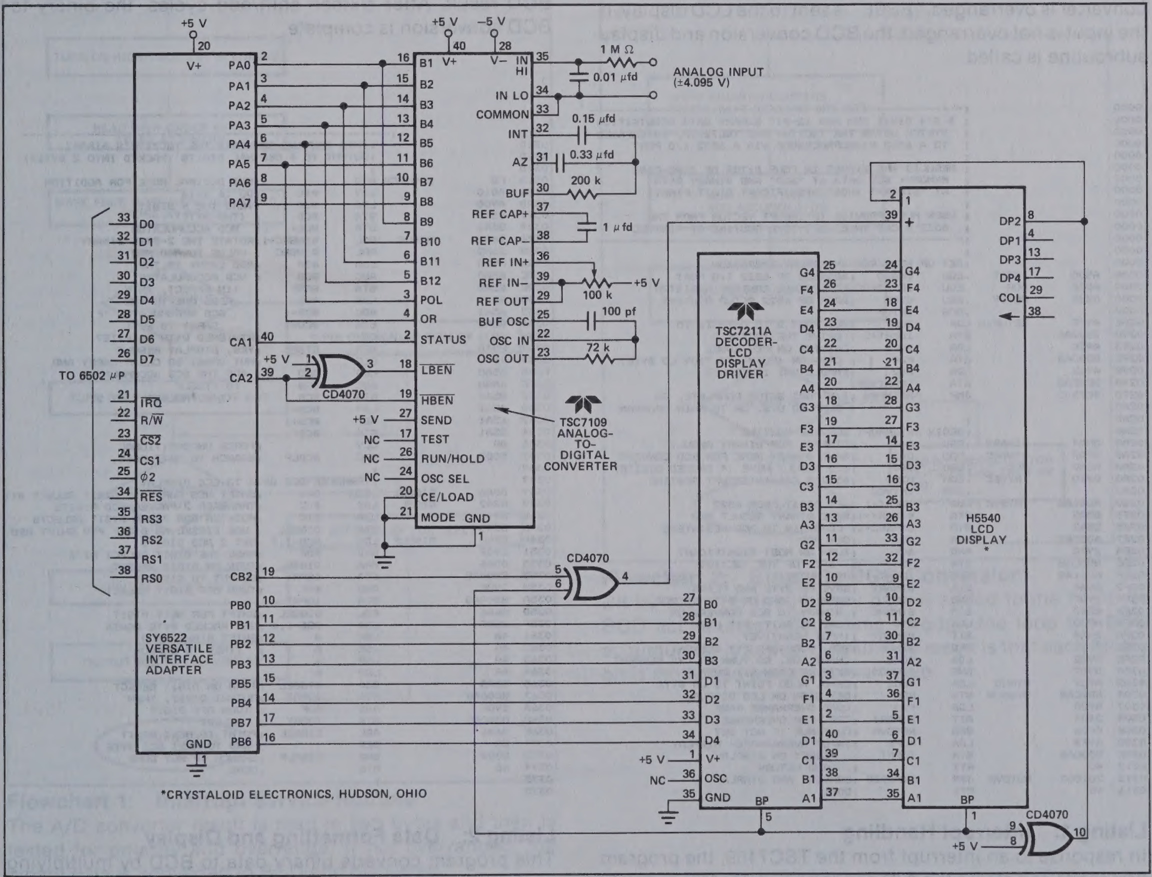
+5 V
20
V+
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
D0
D1
D2
D3
D4
D5
D6
D7
TO 6502 μP
IRQ
R/W
CS2
CS1
φ2
RES
RS3
RS2
RS1
RS0
CA1
CA2
CB2
PB0
PB1
PB2
PB3
PB5
PB4
PB7
PB6
GND
SY6522 VERSATILE INTERFACE ADAPTER
*CRYSTALOID ELECTRONICS, HUDSON, OHIO
CD4070
+5 V
−5 V
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
POL
OR
STATUS
LBEN
HBEN
SEND
TEST
RUN/HOLD
OSC SEL
CE/LOAD
MODE
GND
NC
IN HI
IN LO
COMMON
INT
AZ
BUF
REF CAP+
REF CAP−
REF IN+
REF IN−
REF OUT
BUF OSC
OSC IN
OSC OUT
TSC7109 ANALOG-TO-DIGITAL CONVERTER
1 MΩ
0.01 μfd
ANALOG INPUT (±4.095 V)
0.15 μfd
0.33 μfd
200 k
1 μfd
100 k
100 pf
72 k
TSC7211A DECODER-LCD DISPLAY DRIVER
B0
B1
B2
B3
D1
D2
D3
D4
V+
OSC
GND
BP
H5540 LCD DISPLAY
DP2
DP1
DP3
DP4
COL
G4 F4 E4 D4 C4 B4 A4
G3 F3 E3 D3 C3 B3 A3
G2 F2 E2 D2 C2 B2 A2
G1 F1 E1 D1 C1 B1 A1

Figure 1: 12-Bit A/D Converter with 3 3/4 Digit Display

One I/O device links both the A/D converter and decoder-display driver to a microprocessor. With data formatting in software, the circuit provides faster analog conversion speed and more resolution than 3 1/2 digit display-oriented converters.

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microprocessor then reads U2's conversion data in two bytes, selecting the high or low-order byte via the CA2 handshake output.

After converting binary data to BCD in software, the microprocessor loads LCD driver U3 via port B of U1. BCD digits are output on the lower four bits of port B, while the upper four bits serve as digit select outputs. The CB2 handshake output of U1 controls the polarity segment of the LCD display.

Software for the 3 3/4 digit converter consists of an interrupt service routine and a binary-to-BCD conversion subroutine. In response to a CA1 interrupt, the microprocessor jumps to the service routine of listing 1. Using U1's peripheral control register to toggle U2's byte select inputs, the microprocessor reads and stores two bytes of binary data beginning at location BINARY. After stripping the flag bits from the most significant byte, the conversion's magnitude is stored beginning at BINSRC. The program transfers the sign bit to the display, and then tests for an overrange condition. If the A/D converter is overranged, "EEEE" is sent to the LCD display. If the input is not overranged, the BCD conversion and display subroutine is called.

Binary-to-BCD conversion is accomplished by multiplying each binary bit by its equivalent decimal value and summing the bit values. Since each binary bit is some factor of two, only a multiplication by two is required. The multiplication can be reduced to a decimal add, since A+A=2*A, and the SED (SEt Decimal) mode provides easy BCD addition.

The BCD conversion begins with the binary data in two memory locations, BINSRC and BINSRC+1, which are used as a 16-bit shift register. Two other locations, BCD and BCD+1 serve as a 4 digit BCD accumulator. The sixteen bits of binary data are shifted toward the most significant bit. Bits which are logical "1" are added, via the carry, to the BCD accumulator. After each shift, the BCD accumulator is added to itself (i.e. multiplied by two). On each succeeding pass, the sum of the binary bits is again multiplied by two. For example, bit 11 will go thru the multiplication loop eleven times and will then have a value of 2 ▲11, or 2048. Bit 4 goes thru the loop four times, and ends with a value of 16. The sum of the BCD values for each bit of the binary word is the final BCD result. After sixteen shift/add cycles, the binary-to-BCD conversion is complete.

```
0000                   ;-------------------------------------------------------
0000                   ; 3 3/4 DIGIT DVM AND 12-BIT BINARY DATA ACQUISITION
0000                   ;  SYSTEM USING THE TSC7109 AND TSC7211A, INTERFACED
0000                   ;  TO A 6502 MICROPROCESSOR VIA A 6522 I/O PORT
0000                   ;
0000                   ; RESULTS ARE STORED IN FOUR BYTES OF ZERO-PAGE
0000                   ;  MEMORY: BCD DATA AT "BCD" AND BINARY DATA
0000                   ;  AT "BINARY" (MOST SIGNIFICANT DIGIT FIRST)
0000                   ;
0000                   ; USER MUST PROVIDE INTERRUPT VECTOR FROM THE
0000                   ;  6522'S CA1 INTERRUPT TO A ROUTINE AT "INTVEC"
0000                   ;-------------------------------------------------------
0000                   ;
0000                   ;SET UP 6522 FOR INTERRUPT OPERATION
0000  A800     IOPRT   .EQU    0A800   ;ADDRESS OF 6522 I/O PORT
0000  A80C     PCR     .EQU    IOPRT+0C;PERIPHERAL CONTROL REGISTER
0000  028E     SETUP   .EQU    028E    ;ADDR OF 6522 SETUP ROUTINE
0000                   .ORG    SETUP
028E  A9FF     SETUPIO LDA     #0FF    ;SET PORT B TO OUTPUTS TO
0290  8D02A8           STA     IOPRT+2 ; DRIVE THE TSC7211A
0293  A9EE             LDA     #0EE    ;CA1=INT ON NEG EDGE,
0295  8D0CA8           STA     PCR     ; CA2=LOW (POINT TO 7109 LO BYTE)
0298  A982             LDA     #82     ;ENABLE CA1 INTERRUPT
029A  8D0EA8           STA     IOPRT+0E;
029D  4C7503           JMP     MAINPRG ;I/O PORT SETUP COMPLETE, SO
02A0                                   ; JUMP TO O.S. OR TO MAIN PROGRAM
02A0                   ;
02A0                   ;BEGIN INTERRUPT SERVICE ROUTINE
02A0  00A4     BINARY  .EQU    0A4     ;STORAGE FOR BINARY RESULT
02A0  00A2     BINSRC  .EQU    0A2     ;SAVE BINARY HERE FOR BCD CONVERT
02A0  00A0     BCD     .EQU    0A0     ;BCD RESULT HERE (4 PACKED DIGITS)
02A0  02E0     INTVEC  .EQU    02E0    ;6522'S CA1 INTERRUPT ROUTINE
02A0                   .ORG    INTVEC
02E0  AD01A8   INTSVC  LDA     IOPRT+1 ;GET DIGIT FROM 6522
02E3  85A5             STA     BINARY+1;SAVE BINARY RESULT AND
02E5  85A3             STA     BINSRC+1; LOAD BIN TO BCD REGISTERS
02E7  AD0CA8           LDA     PCR     ;GET PCR
02EA  29FC             AND     #0FC    ;TURN ON MOST SIGNIFICANT
02EC  8D0CA8           STA     PCR     ;  BYTE OF THE TSC7109
02EF  AD01A8           LDA     IOPRT+1 ;GET MS BYTE
02F2  85A4             STA     BINARY  ;SAVE MS BYTE AND FLAGS
02F4  290F             AND     #0F     ;MASK POL AND OR BITS BEFORE
02F6  85A2             STA     BINSRC  ; BINARY TO BCD CONVERSION
02F8  A910             LDA     #10     ;LOAD POLARITY-BIT MASK
02FA  24A4             BIT     BINARY  ;INPUT NEGATIVE?
02FC  F004             BEQ     MINUS   ;YES, TURN OFF "Y" SEGMENT
02FE  A9EE             LDA     #0EE    ;INPUT POS, SO TURN ON "Y" SEGMENT
0300  D002             BNE     SIGNON  ;SKIP TO SIGN-BIT OUTPUT
0302  A9C2     MINUS   LDA     #0CE    ;CB=0, ALSO POINT TO LS BYTE
0304  8D0CA8   SIGNON  STA     PCR     ;SET SIGN ON LCD DISPLAY
0307  A920             LDA     #20     ;LOAD OVERRANGE MASK
0309  24A4             BIT     BINARY  ;TEST FOR OVERRANGE
030B  F006             BEQ     NOTOVR  ;CONTINUE IF NOT SET
030D  A9FB             LDA     #0FB    ;INPUT OVERRANGED- DISPLAY
030F  8D00A8           STA     IOPRT   ;  "EEEE" ON DISPLAY
0312  40               RTI             ;   AND RETURN
0313  201D03   NOTOVR  JSR     BIN2BCD ;CONVERT AND DISPLAY
0316  40               RTI             ;DONE
```

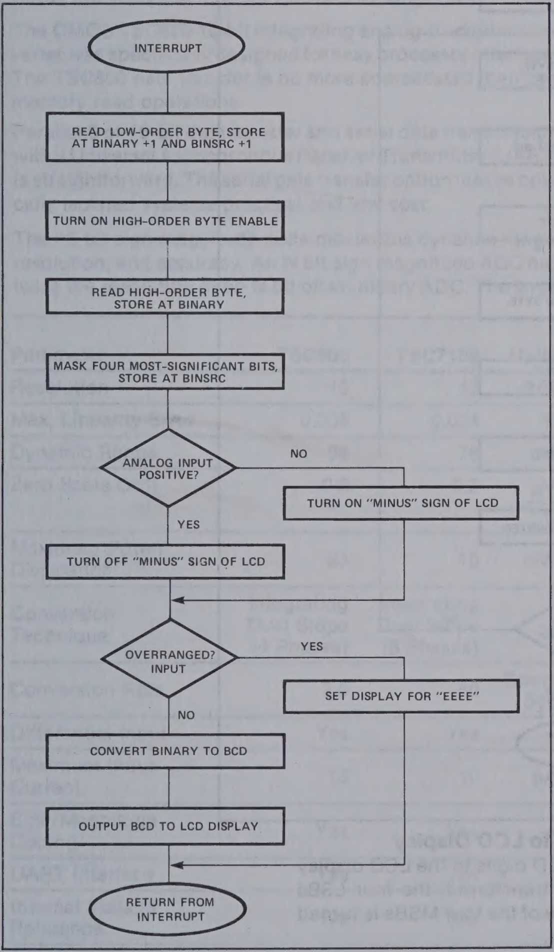
Listing 1: Interrupt Handling
In response to an interrupt from the TSC7109, the program first reads and stores the A/D converter's data. After polarity and overrange tests, the binary data is converted to BCD and transferred to the LCD display.

```
031D                 ;----------------------------------------------------------
031D                   ;THIS ROUTINE CONVERTS THE TSC7109'S BINARY
031D                   ;OUTPUT TO 4 DECIMAL DIGITS (PACKED INTO 2 BYTES)
031D                   ;
031D  F8       BIN2BCD SED                     ;SET DECIMAL MODE FOR ADDITION
031E  A010             LDY     #10     ;DO 16 BITS
0320  A900             LDA     #00     ;ZERO THE 4 DIGIT
0322  85A0             STA     BCD     ; (TWO BYTE)
0324  85A1             STA     BCD+1  .;  BCD ACCUMULATOR
0326  26A3     BCDLP   ROL     BINSRC+1;ROTATE THE 2-BYTE BINARY
0328  26A2             ROL     BINSRC  ; VALUE TOWARD MSB
032A  A900             LDA     #00     ;ADD CARRY TO THE
032C  65A0             ADC     BCD     ; BCD ACCUMULATOR
032E  85A0             STA     BCD     ;  (IN EFFECT, THIS
0330  A900             LDA     #00     ;   ADDS ONE TO THE
0332  65A1             ADC     BCD+1   ;    BCD ACCUMULATOR IF
0334  85A1             STA     BCD+1   ;     CARRY IS SET)
0336  88               DEY             ;FINISHED WITH 16 BITS?
0337  F010             BEQ     DISPL   ;YES, DISPLAY RESULT
0339  18               CLC             ;NOT DONE, SO CLEAR CARRY AND
033A  A5A0             LDA     BCD     ; ADD THE BCD ACCUMULATOR
033C  65A0             ADC     BCD     ;  TO ITSELF
033E  85A0             STA     BCD     ;   (I.E. MULTIPLY BY 2)
0340  A5A1             LDA     BCD+1
0342  65A1             ADC     BCD+1
0344  85A1             STA     BCD+1
0346  B8               CLV             ;FORCE UNCONDITIONAL
0347  50DD             BVC     BCDLP   ;BRANCH TO NEXT PASS
0349                   ;
0349                   ;TRANSFER BCD DATA TO LCD DISPLAY
0349  00A6     DIGSEL  .EQU    0A6     ;SHIFT REG FOR 7211 DIGIT SELECT BIT
0349  A202     DISPL   LDX     #02     ;TRANSFER 2 PACKED-BCD DIGITS -
034B  A910             LDA     #10     ;POINTER FOR 7211A DIGIT SELECTS
034D  85A6             STA     DIGSEL  ; USE DIGSEL AS DIGIT PTR SHIFT REG
034F  B59F     DISPLP  LDA     BCD-1,X ;GET 2 BCD DIGITS
0351  290F             AND     #0F     ;MASK THE DIGIT SELECT BITS
0353  05A6             ORA     DIGSEL  ;TURN ON DIGIT SELECT
0355  8D00A8           STA     IOPRT   ;OUTPUT TO DISPLAY
0358  290F             AND     #0F     ;TURN OFF DIGIT SELECT
035A  8D00A8           STA     IOPRT
035D  06A6             ASL     DIGSEL  ;SHIFT FOR NEXT DIGIT
035F  B59F             LDA     BCD-1,X ;GET PACKED BYTE AGAIN
0361  4A               LSR     A       ;SHIFT RIGHT FOUR
0362  4A               LSR     A       ;  TIMES TO UNPACK
0363  4A               LSR     A
0364  4A               LSR     A
0365  05A5             ORA     DIGSEL  ;TURN ON DIGIT SELECT
0367  8D00A8           STA     IOPRT   ;OUTPUT DIGIT, THEN
036A  290F             AND     #0F     ; TURN OFF DIGIT
036C  8D00A8           STA     IOPRT   ;  SELECT
036F  06A6             ASL     DIGSEL  ;POINT TO NEXT DIGIT
0371  CA               DEX             ; AND TO NEXT BCD BYTE
0372  D0DB             BNE     DISPLP  ;BRANCH IF NOT DONE
0374  60               RTS             ;DONE
0375                   ;
0375                   ;
```

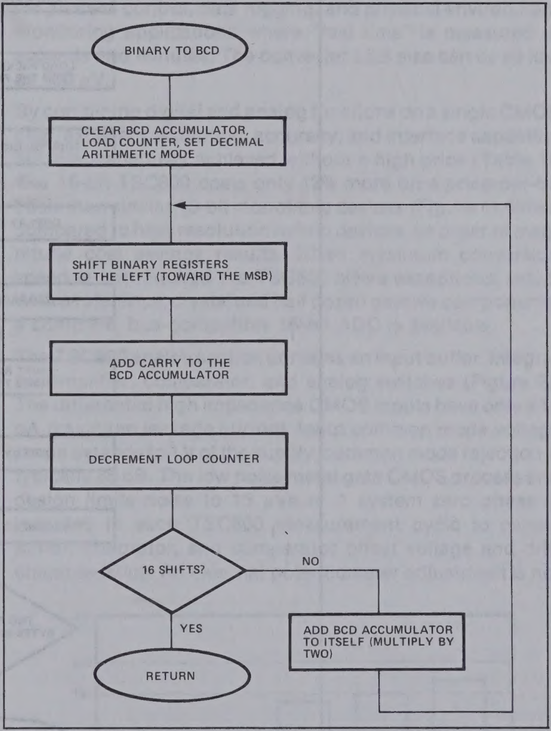
Listing 2: Data Formatting and Display
This program converts binary data to BCD by multiplying each binary bit by its decimal value. The LCD display is accessed one BCD digit at a time, using a shift register in memory to store the digit select bit.

Although the BCD conversion program shifts data sixteen times, only twelve bits are valid. This method was chosen for compact coding. A slight speed penalty is involved, however, since the program unnecessarily loops through the multiplication routine four times. With a 1MHz 6502 clock, the total execution time (listing 1 plus listing 2) is about 1.07 mSec. Program execution will be slightly faster if the binary data is shifted left four times at BIN2BCD and the Y register loop counter is changed from 16 to 12.

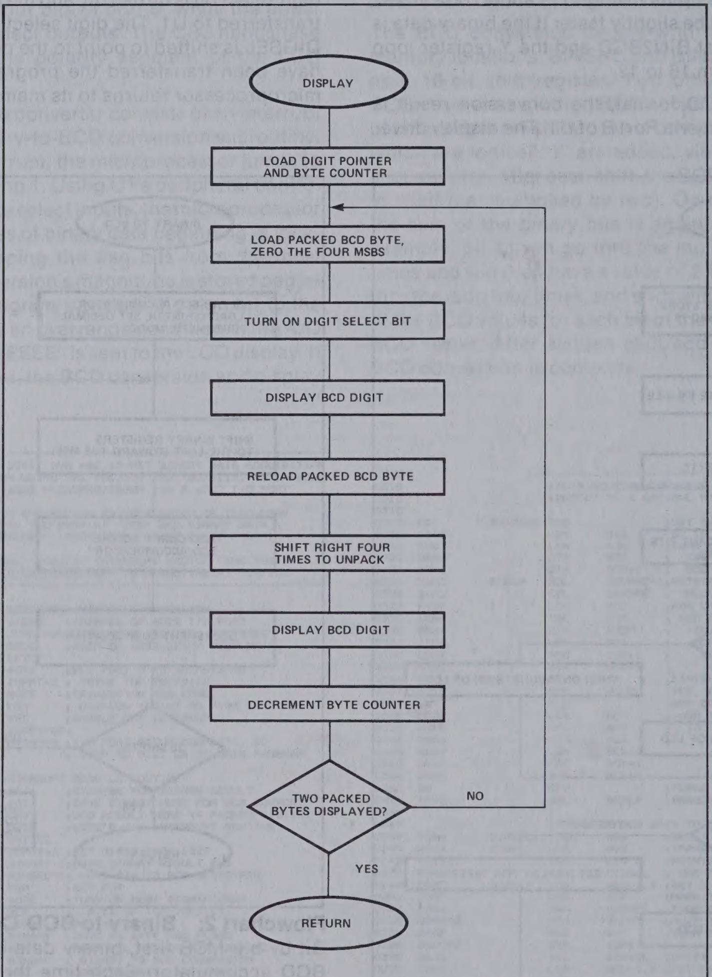
After conversion to BCD format, the conversion result is transferred to the display via Port B of U1. The display driver requires data to be stable on the BO-B3 inputs while the appropriate digit select input (D1 through D4) is strobed high. The program uses memory location DIGSEL as a shift register to sequentially address each of the four digit select inputs. BCD data is loaded into the 6502's accumulator, the digit select bit is turned on, and the accumulator contents are transferred to U1. The digit select bit is then turned off and DIGSEL is shifted to point to the next digit. After four digits have been transferred the program is complete, and the microprocessor returns to its main program.


INTERRUPT
READ LOW-ORDER BYTE, STORE AT BINARY +1 AND BINSRC +1
TURN ON HIGH-ORDER BYTE ENABLE
READ HIGH-ORDER BYTE, STORE AT BINARY
MASK FOUR MOST-SIGNIFICANT BITS, STORE AT BINSRC
ANALOG INPUT POSITIVE?
NO
TURN ON "MINUS" SIGN OF LCD
YES
TURN OFF "MINUS" SIGN OF LCD
OVERRANGED? INPUT
YES
SET DISPLAY FOR "EEEE"
NO
CONVERT BINARY TO BCD
OUTPUT BCD TO LCD DISPLAY
RETURN FROM INTERRUPT

Flowchart 1: Interrupt Service Routine
The A/D converter result is read in two bytes and then is tested for polarity and overrange. If not overranged, the binary data is converted to BCD and displayed.


BINARY TO BCD
CLEAR BCD ACCUMULATOR, LOAD COUNTER, SET DECIMAL ARITHMETIC MODE
SHIFT BINARY REGISTERS TO THE LEFT (TOWARD THE MSB)
ADD CARRY TO THE BCD ACCUMULATOR
DECREMENT LOOP COUNTER
16 SHIFTS?
NO
ADD BCD ACCUMULATOR TO ITSELF (MULTIPLY BY TWO)
YES
RETURN

Flowchart 2: Binary to BCD Conversion
Bit by bit, MSB first, binary data is added to the two-byte BCD accumulator. Each time through the loop the BCD accumulator is added to itself. The result is that each binary bit is multiplied by its decimal value.


DISPLAY
LOAD DIGIT POINTER AND BYTE COUNTER
LOAD PACKED BCD BYTE, ZERO THE FOUR MSBS
TURN ON DIGIT SELECT BIT
DISPLAY BCD DIGIT
RELOAD PACKED BCD BYTE
SHIFT RIGHT FOUR TIMES TO UNPACK
DISPLAY BCD DIGIT
DECREMENT BYTE COUNTER
TWO PACKED BYTES DISPLAYED?
NO
YES
RETURN

Flowchart 3: Data Transfer to LCD Display
Looping twice transfers four BCD digits to the LCD display decoder-driver. For each digit transferred, the four LSBs contain the BCD data, while one of the four MSBs is turned on to function as the digit select.

TELEDYNE SEMICONDUCTOR

Application Note 23
TSC800 Wide Dynamic Range Eliminates System Components
By Wes Freeman and David L. Gillooly

Micro-processor based systems, whether they be complex process controllers, bench top instruments, portable measurement devices, or computer data acquisition systems dominate the market place of the 1980s. Microprocessors maximize creativity and innovation within engineering and marketing teams. The ability to product differentiate and efficiently manufacture products for many market segments from one basic design "customized" through software maximizes the investment return on R&D expenditures.

The CMOS TSC800 16-bit integrating analog-to-digital converter was specifically designed for easy processor interface. The TSC800 data transfer is no more complicated than two memory read operations.

Parallel 8 or 16-bit data transfer and serial data transmission with a Universal Asynchronous Receiver Transmitter (UART) is straightforward. The serial data transfer option makes optically isolated systems practical and low cost.

The 16-bit sign magnitude code maximizes dynamic range, resolution, and accuracy. An N bit sign magnitude ADC has twice the resolution of an N bit offset binary ADC. The large dynamic range can be used to eliminate expensive analog components needed to obtain full 12-bit performance with 12-bit ADCs.

Parameter	TSC800	TSC7109	Units
Resolution	15	12	Bits
Max. Linearity Error	0.006	0.024	%
Dynamic Range	96	78	dB
Zero Scale Drift	0.8	0.2	µV/°C
Maximum Power Dissipation	20	15	mW
Conversion Technique	Integrating Dual Slope (4 Phases)	Integrating Dual Slope (3 Phases)	—
Conversion Rate	2.5	40	Conv/Sec
Differential Input	Yes	Yes	—
Maximum Input Current	15	10	pA
Sign/Magnitude Coding	Yes	Yes	—
UART Interface	Yes	Yes	—
Internal Voltage Reference	No	Yes	—
Automatic 60 Hz Rejection	Yes	Yes	—
Power Supply Voltage	±5 V	±5 V	
Price Per Bit (100 pc Quantity)	$0.95	$0.77	

Table I: TSC800 Electrical Specifications

The TSC800 integrating conversion technique eliminates the need for a sample hold amplifier and automatically attenuates noise. A 400 mS measurement cycle gives a 100 mSec signal integration time. This provides both 50/60 Hz line frequency rejection. The conversion time is more than adequate for process control, data logging, and physical environment monitoring applications where "real time" is measured in seconds and minutes. The converter LSB size can be as low as 100 µV.

By combining digital and analog functions on a single CMOS chip, excellent resolution, accuracy, and interface capability are simultaneously achieved without a high price (Table 1). The 16-bit TSC800 costs only 12% more on a price-per-bit basis than similar 13-bit monolithic devices (Figure 1). When compared to high resolution hybrid devices, an order of magnitude cost savings results. When maximum conversion speed is not required the TSC800 offers exceptional value. With a reference, crystal and half dozen passive components, a complete, bus-compatible 16-bit ADC is available.

The TSC800 analog section contains an input buffer, integrator amplifier, comparator, and analog switches (Figure 2). The differential high impedance CMOS inputs have only a 15 pA maximum leakage current. Input common mode voltage range extends to 1 V of the supply; common mode rejection is typically 86 dB. The low noise metal gate CMOS process and design limits noise to 15 μV_{P-P}. A system zero phase is included in each TSC800 measurement cycle to cancel buffer, integrator, and comparator offset voltage and drift characteristics. An external potentiometer adjustment is not

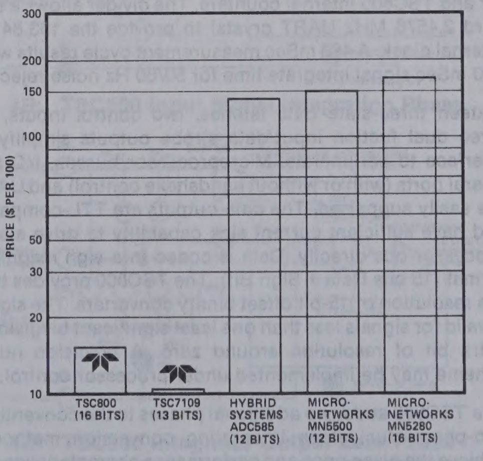


Figure 1: High Resolution TSC800 Features High Performance and Low Price for Low Speed Systems.

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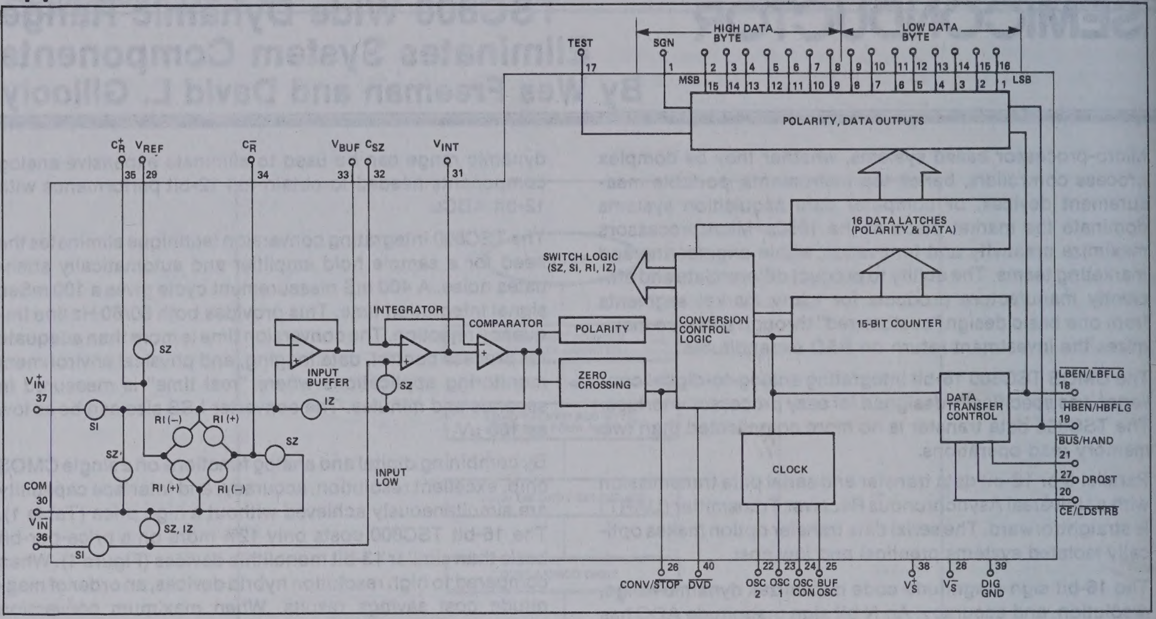

HIGH DATA BYTE
LOW DATA BYTE
TEST
17
SGN
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
MSB
LSB
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
POLARITY, DATA OUTPUTS
C$_R^+$
V$_{REF}$
35
29
C$_R^-$
34
V$_{BUF}$
C$_{SZ}$
33
32
V$_{INT}$
31
16 DATA LATCHES (POLARITY & DATA)
SWITCH LOGIC (SZ, SI, RI, IZ)
INTEGRATOR
COMPARATOR
POLARITY
CONVERSION CONTROL LOGIC
15-BIT COUNTER
SZ
INPUT BUFFER
SZ
IZ
ZERO CROSSING
V$_{IN}^+$
37
SI
RI (−)
RI (+)
SZ
SZ
RI (+)
RI (−)
INPUT LOW
COM
30
V$_{IN}^-$
36
SZ, IZ
SI
DATA TRANSFER CONTROL
LBEN/LBFLG
18
HBEN/HBFLG
19
BUS/HAND
21
27
DRQST
20
CE/LDSTRB
CLOCK
26
40
CONV/STOP
DVD
22
23
24
25
OSC 2
OSC 1
OSC BUF
CON OSC
38
28
39
V$_S^+$
V$_S^-$
DIG GND

Figure 2: Analog and digital compatible CMOS process provides single chip 16-bit converter.

needed to guarantee a zero output for zero volt input. Temperature drift at zero is automatically corrected.

The TSC800 digital section includes an RC or crystal oscillator clock generator, 15-bit counter, 16 three-state data latches, data transfer/conversion control logic, and sign bit logic. The analog and digital compatible metal gate CMOS process allows such extensive circuitry on a single monolithic die.

The oscillator control pin selects either RC or crystal oscillator operation. Normally, crystal operation is desired. In this mode, a divide by 15 counter is inserted between the oscillator and TSC800 internal counters. The divider allows a standard 2.4576 MHz UART crystal to provide the 163.84 kHz internal clock. A 400 mSec measurement cycle results with a 100 mSec signal integrate time for 50/60 Hz noise rejection.

Sixteen three-state data latches, two control inputs, and three dual fuction input/data strobe outputs simplify the interface to peripherals. Microprocessor busses, I/O peripheral ports (with or without handshake control) and UARTs are easily supported. The data outputs are TTL-compatible and have sufficient current sink capability to drive a small processor bus directly. Data is coded in a sign magnitude format (15 bits Data + Sign Bit). The TSC800 provides twice the resolution of 15-bit offset binary converters. The sign bit is valid for signals less than one least significant bit giving an extra bit of resolution around zero. A precision nulling scheme may be implemented under processor control.

The TSC800 adds two additional phases to the conventional two-phase dual slope integrating conversion method to achieve the given price and performance characteristics. The measurement cycle is divided into four separate phases (Figure 3).

- System Zero
- Signal Integrate
- Reference Integrate
- Integrator Zero

The system zero phase (Figure 4A) begins when the internal analog switches connect the buffer input to analog common and a feedback loop closes around the integrator and comparator. The external capacitors charge to compensate for buffer, integrator, and comparator offset errors. With a zero input at the buffer, the integrator output will remain at zero.

Since the converter's major error sources are nulled during each measurement cycle, temperature sensitivity is greatly reduced. The zero scale error drift, always a large error source in successive approximation converters, is reduced to typiclly 0.8 μV/° C.

The signal integrate phase follows (Figure 4B). The differential input signal is applied to the integrator for 16,384 internal clock cycles. The integrator output at the end of the fixed time is proportional to the input. Since the integrate time is fixed by the clock period, the interval can be adjusted to give maximum attenuation of repetitive waveforms such as 50/60 Hz power line signals. A 100 mSec integration rejects 50,60 and 400 Hz signals.

In the reference integrate or deintegrate cycle (Figure 4C), the reference capacitor, which was charged to the reference voltage during system zero, is conneced to ramp the integrator back toward zero. The 15-bit counter is enabled and counts until a zero crossing is detected by the comparator. Data is transferred to the data latches and Data Valid (DVD) goes low. This cycle normally lasts 32,678 clock period.

The final phase is integrator output zero (Figure 4D). This phase provides a rapid recovery from overloads by connec-

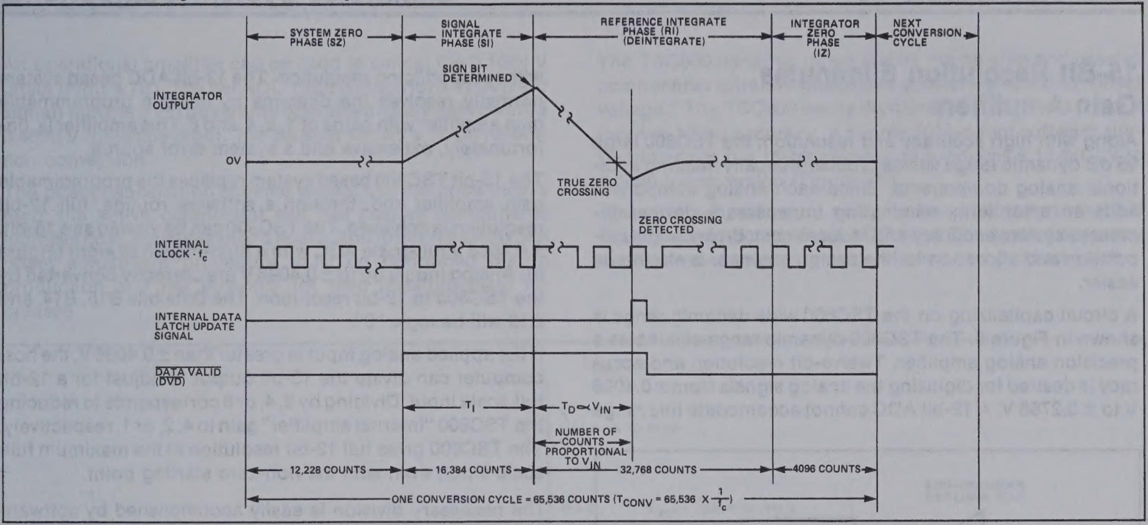
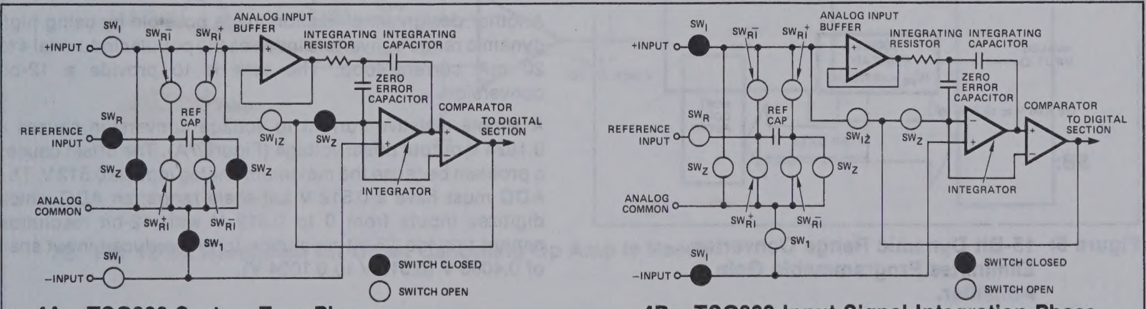


Figure 3: TSC800 integrating converter updates conventional dual slope conversion with system zero and integrator zero phase.

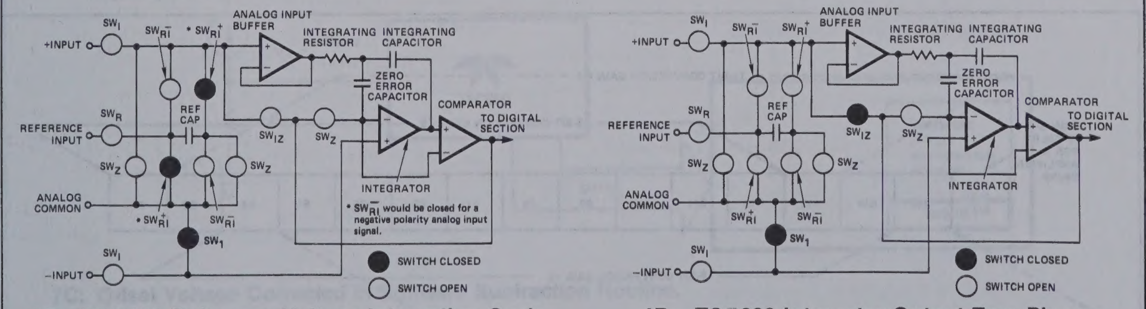
ting the comparator output to the buffer input for 4096 clock cycles. Any charge remaining in the integration capacitor is removed, allowing an accurate system zero cycle.

The TSC800 supports either continuous or convert on command operation. When the Conv/$\overline{\text{Stop}}$ input is low, the converter remains in the system zero phase. A new conversion will not begin until Conv/$\overline{\text{Stop}}$ goes high. Conv/$\overline{\text{Stop}}$ has no effect when Data Valid ($\overline{\text{DVD}}$) is high, but pulsing the Conv/$\overline{\text{Stop}}$ low after a comparator zero will immediately terminate reference integrate and cause entry into the zero integrator phase. In this case, the conversion rate will vary with input signal magnitude.


ANALOG INPUT BUFFER
INTEGRATING RESISTOR
INTEGRATING CAPACITOR
ZERO ERROR CAPACITOR
COMPARATOR
TO DIGITAL SECTION
INTEGRATOR
+INPUT
REFERENCE INPUT
ANALOG COMMON
–INPUT
SW_I
SW_{RI}^-
SW_{RI}^+
SW_R
REF CAP
SW_{IZ}
SW_Z
SW_1
SWITCH CLOSED
SWITCH OPEN

4A: TSC800 System Zero Phase

4B: TSC800 Input Signal Integration Phase


ANALOG INPUT BUFFER
INTEGRATING RESISTOR
INTEGRATING CAPACITOR
ZERO ERROR CAPACITOR
COMPARATOR
TO DIGITAL SECTION
INTEGRATOR
+INPUT
REFERENCE INPUT
ANALOG COMMON
–INPUT
SW_I
SW_{RI}^-
• SW_{RI}^+
SW_R
REF CAP
SW_{IZ}
SW_Z
SW_1
• SW_{RI}^- would be closed for a negative polarity analog input signal.
SWITCH CLOSED
SWITCH OPEN

4C: TSC800 Reference Voltage Integration Cycle

4D: TSC800 Integrator Output Zero Phase

Figure 4: Internal analog gates automatically configure analog circuits for four phases of TSC800 measurement cycle.

15-Bit Resolution Eliminates Gain Amplifiers

Along with high accuracy and resolution, the TSC800 large 96 dB dynamic range solves problems usually needing additional analog components. Since each analog component adds an error term, eliminating unnecessary devices increases system accuracy and reduces cost. Error budget calculation and allocation for the design engineer is also made easier.

A circuit capitalizing on the TSC800 wide dynamic range is shown in Figure 5. The TSC800 dynamic range eliminates a precision analog amplifier. Twelve-bit resolution and accuracy is desired for digitizing the analog signals from ± 0.4096 V to ± 3.2768 V. A 12-bit ADC cannot accomodate this range without sacrificing resolution. The 12-bit ADC based system normally resolves the dilemma by using a programmable gain amplifier with gains of 1, 2, 4, and 8. This amplifier is, unfortunately, expensive and a system error source.

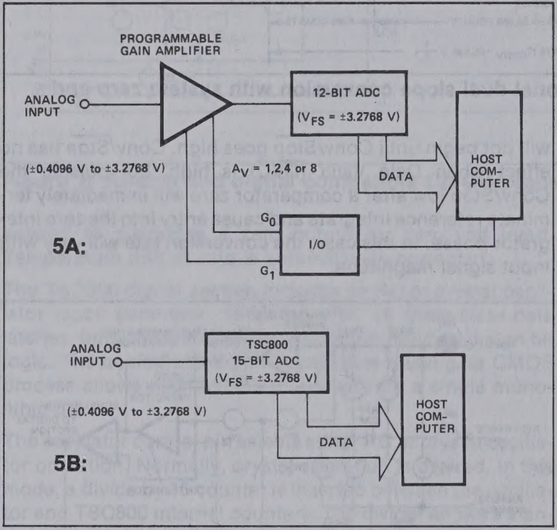

PROGRAMMABLE GAIN AMPLIFIER
ANALOG INPUT
12-BIT ADC
(V_{FS} = ±3.2768 V)
(±0.4096 V to ±3.2768 V)
A_V = 1,2,4 or 8
DATA
HOST COM-PUTER
G_0
I/O
G_1
5A:
ANALOG INPUT
TSC800
15-BIT ADC
(V_{FS} = ±3.2768 V)
(±0.4096 V to ±3.2768 V)
DATA
HOST COM-PUTER
5B:

Figure 5: 15-Bit Dynamic Range Converter Eliminates Programmable Gain Amplifier.

The 15-bit TSC800 based system replaces the programmable gain amplifier and, through a software routine, full 12-bit resolution is achieved. The TSC800 can be viewed as a 15-bit, ± 0.4096 V full-scale ADC with a built-in gain of eight (Figure 6). Analog inputs up to ± 0.4096 V are correctly converted by the TSC800 to 12-bit resolution. The Data bits B15, B14, and B13 will be logic "0".

If the applied analog input is greater than ± 0.4096 V, the host computer can divide the 15-bit output to adjust for a 12-bit full-scale input. Dividing by 2, 4, or 8 corresponds to reducing the TSC800 "internal amplifier" gain to 4, 2, or 1, respectively. The TSC800 gives full 12-bit resolution at the maximum full-scale input, even with the non-zero starting point.

The necessary division is easily accomplished by software with a simple right shift of the TSC800 15-bit output (excluding the sign bit). Shifting right one, two, or three times divides by 2, 4, or 8. Bits B15, B14, and B13 should be set to zero after the shift operation, since the sign bit will shift into the most significant bits during the operation.

Current Loop Monitoring Benefits From Wide Dynamic Range

Another design simplification made possible by using high dynamic range converters involves the popular industrial 4 to 20 mA current loop. The task is to provide a 12-bit conversion.

A simple resistive current to voltage conversion causes a 0.1024 V output offset voltage (Figure 7A). The offset causes a problem because the maximum analog input is 0.512 V. The ADC must have a 0.512 V full-scale range; an ADC which digitizes inputs from 0 to 0.512 V with 12-bit resolution cannot provide 12-bit resolution for the reduced input span of 0.4096 V (0.512 V to 0.1024 V).

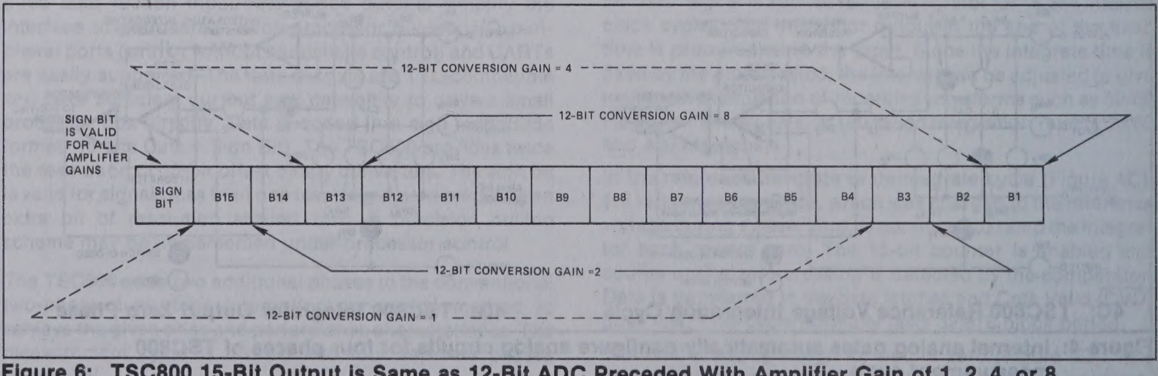

12-BIT CONVERSION GAIN = 4
12-BIT CONVERSION GAIN = 8
SIGN BIT IS VALID FOR ALL AMPLIFIER GAINS
SIGN BIT
B15
B14
B13
B12
B11
B10
B9
B8
B7
B6
B5
B4
B3
B2
B1
12-BIT CONVERSION GAIN =2
12-BIT CONVERSION GAIN = 1

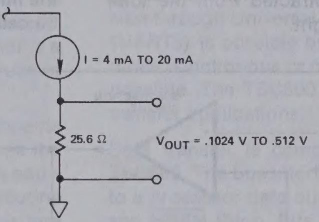
Figure 6: TSC800 15-Bit Output Is Same as 12-Bit ADC Preceded With Amplifier Gain of 1, 2, 4, or 8.

An operational amplifier can be used to cancel the 0.1024 V offset (Figure 7B). The net ADC input voltage for a 4 mA (zero signal) input is 0 V. The op amp operates at unity gain giving a 0.4096 V full-scale input. The op amp allows a 12-bit resolution conversion.

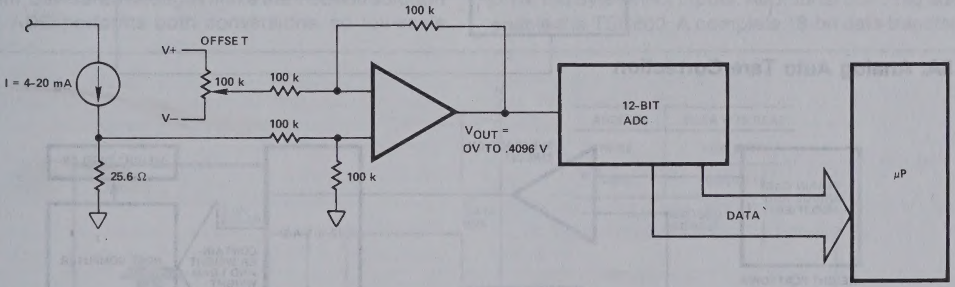
The offset cancellation scheme works, but the price paid is high; the active component and five passive components increase cost, consume board space, and lower reliability. An offset adjustment procedure must be performed during production and the potential for field misadjustment increases.

The TSC800 dynamic range allows the op amp and passive components to be eliminated by a software-generated "offset voltage." The TSC800 easily digitizes the 0.1024 V to 0.512 V input to 12-bit accuracy. A simple 1024-count software subtraction from the 15-bit conversion produces a 12-bit, 0V to 0.4096 V conversion (Figure 7C).

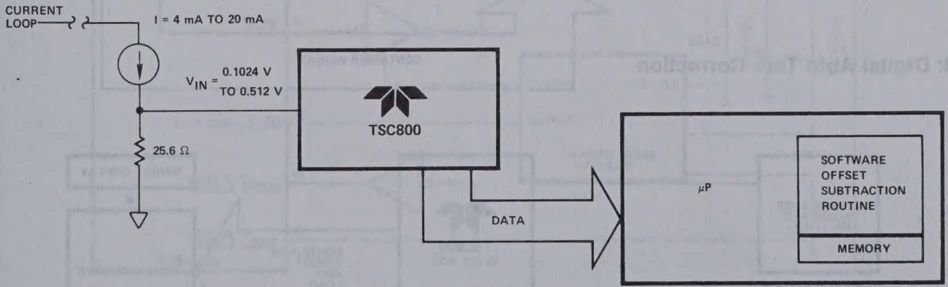
The reduced part count and one less calibration step will offset the additional 15-bit ADC cost. The system accuracy and increased reliability also enhance end product value.


I = 4 mA TO 20 mA
25.6 Ω
V_{OUT} = .1024 V TO .512 V

7A: Resistive Current to Voltage Conversion Causes Offset Voltage.


100 k
OFFSET
V+
I = 4-20 mA
100 k
100 k
V–
100 k
25.6 Ω
100 k
V_{OUT} = 0V TO .4096 V
12-BIT ADC
DATA
µP

7B: For 12-Bit Resolution An Offset Cancelling Op Amp is Needed.


CURRENT LOOP
I = 4 mA TO 20 mA
V_{IN} = 0.1024 V TO 0.512 V
25.6 Ω
TSC800
DATA
µP
SOFTWARE OFFSET SUBTRACTION ROUTINE
MEMORY

7C: Offset Voltage Corrected in Software Subtraction Routine.

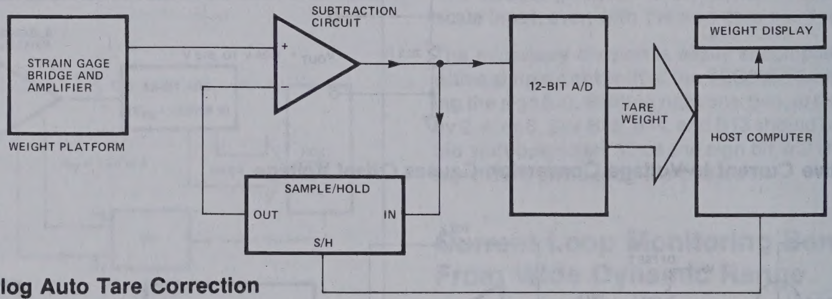
Figure 7: 16-Bit Dynamic Range ADC Provides Full 12-Bit Resolution Without Analog Offset Correcting Components.

Automatic Tare Weighing System Eliminates Analog Components

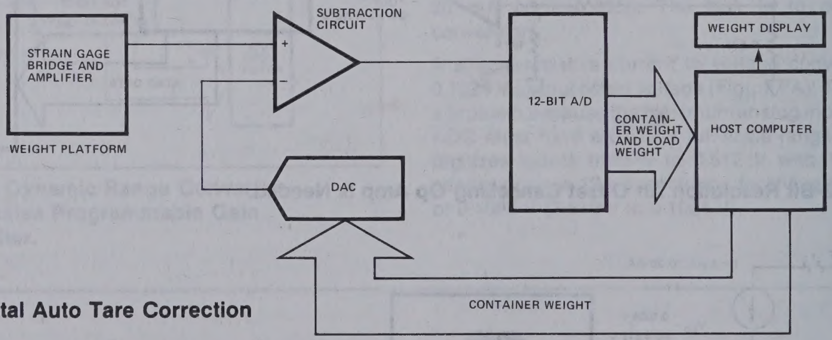
The digital offset correction scheme is useful in digital weighing systems where automatic tare is desired. Auto-tare weighing systems automatically subtract the container's weight from a measurement; the scale displays a true reading just of the contents weight. The container's weight must be measured, stored, and subtracted from the total weight.

A strain gauge or load cell represent typical weight sensors. Strain gauge output levels are below the resolution level of ADCs; amplification is required. Amplifier-related errors are unavoidable, but become magnified in auto-tare systems. The container weight must be subtracted from the total weight to yield the true content weight.

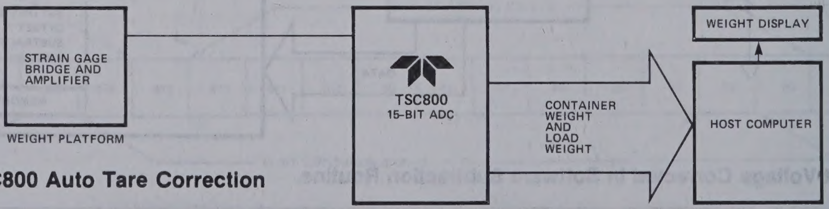
One circuit that subtracts uses a sample/hold amplifier and operational amplifier (Figure 8A). With an empty container on the weighing platform, the sample/hold amplifier samples and holds the op amp output voltage. The voltage stored on the sample/hold amplifier hold capacitor represents the container's weight. The sample/hold output is connected to the op amp's inverting input, effectively subtracting the container's weight. The analog components to store the container's weight limit system performance. For example, the sample/hold droop rate will limit the maximum allowable time between sampling the container's weight and weighing the filled container. The operational amplifier gain must also be calibrated.


STRAIN GAGE BRIDGE AND AMPLIFIER
WEIGHT PLATFORM
SUBTRACTION CIRCUIT
+
−
SAMPLE/HOLD
OUT
IN
S/H
12-BIT A/D
TARE WEIGHT
WEIGHT DISPLAY
HOST COMPUTER

8A: Analog Auto Tare Correction


STRAIN GAGE BRIDGE AND AMPLIFIER
WEIGHT PLATFORM
SUBTRACTION CIRCUIT
+
−
DAC
12-BIT A/D
CONTAIN-ER WEIGHT AND LOAD WEIGHT
WEIGHT DISPLAY
HOST COMPUTER
CONTAINER WEIGHT

8B: Digital Auto Tare Correction


STRAIN GAGE BRIDGE AND AMPLIFIER
WEIGHT PLATFORM
TSC800
15-BIT ADC
CONTAINER WEIGHT AND LOAD WEIGHT
WEIGHT DISPLAY
HOST COMPUTER

8C: TSC800 Auto Tare Correction

Figure 8: TSC800 Scale System Eliminates Analog Droop Errors and Precision DAC.

The droop rate problem inherent in the sample hold subtract circuit can be avoided by using a digital-to-analog converter (DAC) for the feedback subtraction voltage. Figure 8B shows the sample/hold replaced by a DAC. The host computer converts the op amp output to a digital value through an ADC. The digital value is stored and transmitted to the DAC. The reconverted subtraction voltage applied to the op amp input is not subject to droop errors. The time interval between container weighing and substance weighing is unlimited.

The DAC-based subtraction circuit has drawbacks. The DAC must be calibrated so its output exactly tracks the ADC full-scale input voltage. The container weight correction occurs in discrete steps, so the DAC dynamic range must match the range of container weights to be encountered. If not, the cancellation circuit resolution will limit system accuracy. This constraint becomes significant when the container is a significant percentage of total. Weighing gravel in a truck or aspirin in a glass bottle are two examples.

The TSC800 large dynamic range makes analog components unnecessary. In Figure 8C, the TSC800 first measures the container weight. The digital value is stored in memory and a second conversion is made with total load. A software routine subtracts the stored container weight and the result is tare weight.

The TSC800 method is conceptually the same as the DAC-based system. Several advantages make the TSC800 solution better. The ADC performs both conversions, so full-scale errors cancel. The 15-bit TSC800 gives impressive resolution and range; 20,000 pounds of gravel in a 12,000 pound truck, or 0.01 gram of aspirin in a 300 gram bottle!

Data Bus Interface

A commercially successful analog-to-digital converter must offer more than high resolution and accuracy for wide market acceptance. The converter's data transfer capabilities are equally important. A converter able to fit easily in 8 or 16-bit data systems, as well as serial configured systems, will be widely used and offer long-term price advantages over less functional components. The TSC800 transmits data in two 8-bit parallel words, or one 16-bit wide byte. Serial transmission through Universal Asynchronous Receiver Transmitters (UARTs) is possible by using the handshake data transfer mode. Continuous or convert on command conversions are possible. The TSC800 can be used in interrupt-driven data transfer applications.

Data transfer is completely under user control with the TSC800. The bus interface mode allows a direct connection to a processor data bus. The dual function $\overline{\text{LBEN}}$ (Bits 1-8) and $\overline{\text{HBEN}}$ (Sign, Bits 9-15) inputs along with chip enable ($\overline{\text{CE}}$) activate the three state data outputs.

Figure 9 pictures a typical interface. Address bit A0 and $\overline{\text{A0}}$ drive the byte select inputs. Additional decoded address bits enable the TSC800. A complete 16-bit data transfer requires

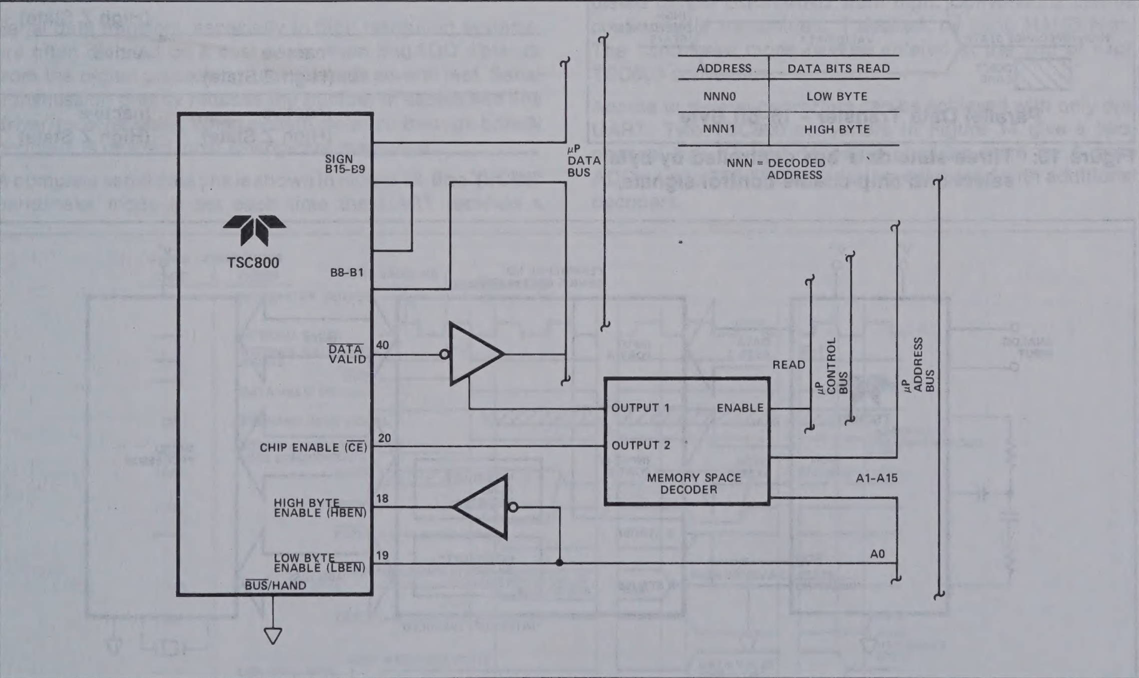
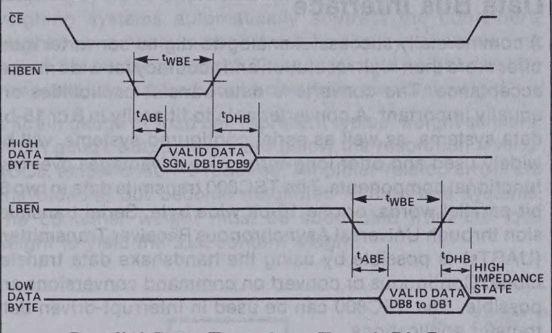
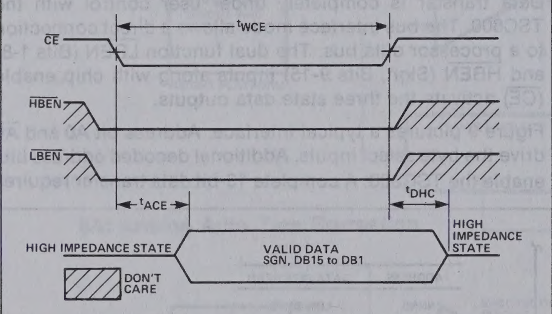


Figure 9: A low-cost interface results when you access the TSC800's 16 data bits directly by treating the converter as two memory locations.

two memory read operations. All 16-bit data lines can be active for 16-bit wide date bus (Figure 10). Monitoring the TSC800 data valid signal ($\overline{\text{DVD}}$) allows the user to verify data did not change during the two byte operation.


$\overline{\text{CE}}$
$\overline{\text{HBEN}}$
t_{WBE}
t_{ABE}
t_{DHB}
HIGH DATA BYTE
VALID DATA SGN, DB15-DB9
$\overline{\text{LBEN}}$
t_{WBE}
t_{ABE}
t_{DHB}
HIGH IMPEDANCE STATE
LOW DATA BYTE
VALID DATA DB8 to DB1

Parallel Data Transfer - Two 8-Bit Bytes


t_{WCE}
$\overline{\text{CE}}$
$\overline{\text{HBEN}}$
$\overline{\text{LBEN}}$
t_{DHC}
t_{ACE}
HIGH IMPEDANCE STATE
VALID DATA SGN, DB15 to DB1
HIGH IMPEDANCE STATE
DON'T CARE

Parallel Data Transfer - 16-Bit Byte

Figure 10: Three state data bus controlled by byte select and chip enable control signals.

The bus data transfer mode supports interfaces using peripheral input/output chips like the 6522 Versatile Interface Adapter and 8255 Programmable Peripheral Interface Device. Data access involves selecting and reading two I/O ports. The interface in Figure 11 does not need additional software, as the 6522 and 8255 I/O ports initialize as input ports at power-up or on reset.

A data error may result if data changes — because of a new conversion update — between the processor's high and low byte read cycles. An easy error detection scheme is implemented with the peripheral I/O chip programmed for strobed input operation. The $\overline{\text{DVD}}$ signal is used to strobe data into the I/O chip. The strobe signal also sets the I/O chip interrupt flag, but a processor interrupt is prevented by clearing the interrupt enable register. To access data, the microprocessor reads port A (which resets Port A's interrupt flag), then port B, and finally the port A interrupt flag. If port A's interrupt flag is set, an output data latch update occurred during the read cycle. If the interrupt flag remained clear, then both data bytes are valid.

$\overline{\text{CE}}$	$\overline{\text{HBEN}}$	$\overline{\text{LBEN}}$	High Data Byte (SGN, DB_{15} - DB_9)	Low Data Byte (DB_8 - DB_1)
1	X	X	Inactive (High Z State)	Inactive (High Z State)
0	0	0	Active	Active
0	0	1	Active	Inactive (High Z State)
0	1	0	Inactive (High Z State)	Active
0	1	1	Inactive (High Z State)	Inactive (High Z State)

"X" = 1 or 0

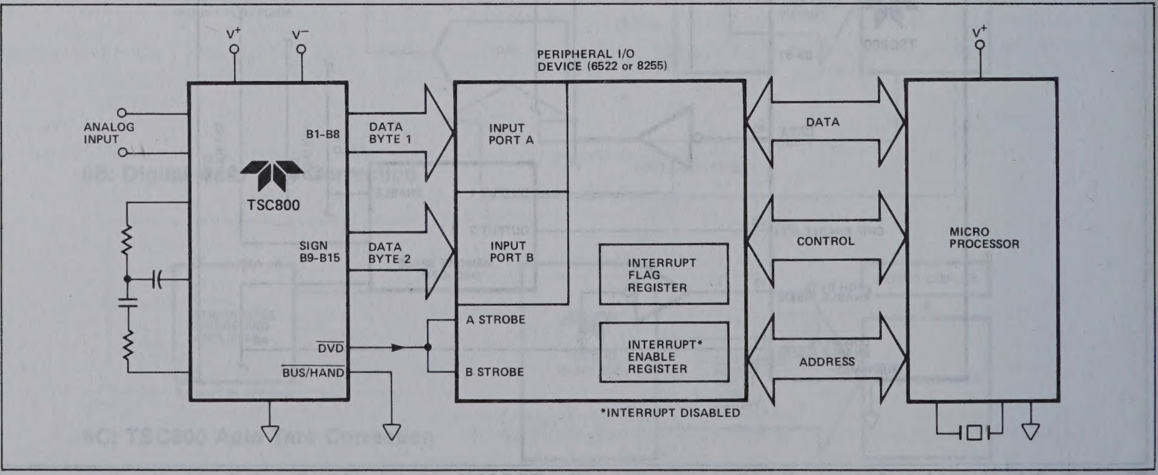

V+
V−
ANALOG INPUT
B1-B8
TSC800
SIGN B9-B15
$\overline{\text{DVD}}$
BUS/$\overline{\text{HAND}}$
DATA BYTE 1
DATA BYTE 2
PERIPHERAL I/O DEVICE (6522 or 8255)
INPUT PORT A
INPUT PORT B
A STROBE
B STROBE
INTERRUPT FLAG REGISTER
INTERRUPT* ENABLE REGISTER
*INTERRUPT DISABLED
DATA
CONTROL
ADDRESS
V+
MICRO PROCESSOR

Figure 11: Using an I/O port simplifies μP interfacing. Reading the interrupt flag register prevents data overrun.

Serial Data Transfer With Handshake Mode

The TSC800 actively controls the data transfer to peripherals in the handshake data output mode. The load strobe ($\overline{\text{LDSTRB}}$) output signal indicates valid data is available for the peripheral receiving device. The low byte ($\overline{\text{LBFLG}}$) and high byte ($\overline{\text{HBFLG}}$) outputs signal which data byte is available. The data request input signal ($\overline{\text{DRQST}}$) informs the TSC800 a peripheral is ready to accept data. A complete cycle transfers two 8-bit bytes.

The handshake mode suports remote data acquisition systems using serial data transmission through current loop, RS232 or fiber optic data links. Universal Asynchronous Receiver Transmitter (UART) communication ICs provide an inexpensive parallel to serial conversion. Start, stop, and parity bits, if required, are automatically inserted on transmission and removed on reception. Data Transmission errors are automatically flagged. The TSC800 handshake mode exactly matches UART input and control requirements, making serial data transmission a practical reality (Figure 12). The UART relieves the system engineer from designing a complex serial data transmission subsystem. The easy TSC800 to UART interface lets the design engineer focus on the data acquisition task, rather than chip interfacing details and serial interface protocols. UARTs are multi-sourced in a variety of technologies: CMOS, NMOS, and PMOS. Some devices lower system part count by including on-chip baud rate generators.

Serial data transfers, especially in high resolution systems, are often dictated on a cost basis when the ADC distance from the digital processing unit exceeds several feet. Serial transmission greatly reduces the number of cables and line driver/receiver units. When system isolation through optical couplers is desired, cost savings are magnified.

A complete serial data link is shown in Figure 13. The TSC800 handshake mode is set each time the UART receives a character. The TSC800 automatically transmits two parallel bytes to the UART for serial transmission. The converter's 2.4576 MHz clock serves double duty by driving the F4702 baud rate generator. Serial data rates between 50 and 19,200 baud are selectable.

When the UART receives a word, the Data Received (DR) output goes high, forcing the TSC800 into the handshake data transfer mode. Once the handshake mode is entered by setting the TSC800 internal handshake flip-flop, the $\overline{\text{BUS}}$/HAND input pin state is ignored.

The DATA REQUEST (DRQST) input is tested for a high UART TRANSMIT BUFFER REGISTER EMPTY (TBRE) signal that indicates the UART is able to accept data. With TBRE high, the High Byte Data Flag ($\overline{\text{HBFLG}}$) goes low and the sign bit plus B15-B9 data bits become active. The Load Strobe ($\overline{\text{LDSTRB}}$) pulse latches the data into the UART transmitter holding register and resets TBRE. The TSC800 tests DRQST again for an indication the UART has sent the first data byte and is ready to accept data (TRBR = 1). $\overline{\text{LBFLG}}$ goes low and output bits B1-B8 become active. $\overline{\text{LDSTRB}}$ pulses low again, latching the final byte into the UART. The $\overline{\text{LBFLG}}$ transition also resets the UART Data Received (DR) output and ends the handshake transfer. Only one conversion is transmitted in response to each word received by the UART.

The TSC800 data latch updating is prevented during the handshake to eliminate improper data transmission. The transmitted data is always the result of the conversion completed before $\overline{\text{BUS}}$/HAND went high. Conversions can be continuously transmitted, if desired, by tying HAND high. The handshake mode is then entered at the end of each TSC800 conversion.

Access to several converters can be achieved with only one UART. Two TSC800 converters in Figure 14 give a two-channel link. Output decoding provides room for 6 more ADCs; up to 256 TSC800s can be addressed with additional decoders.

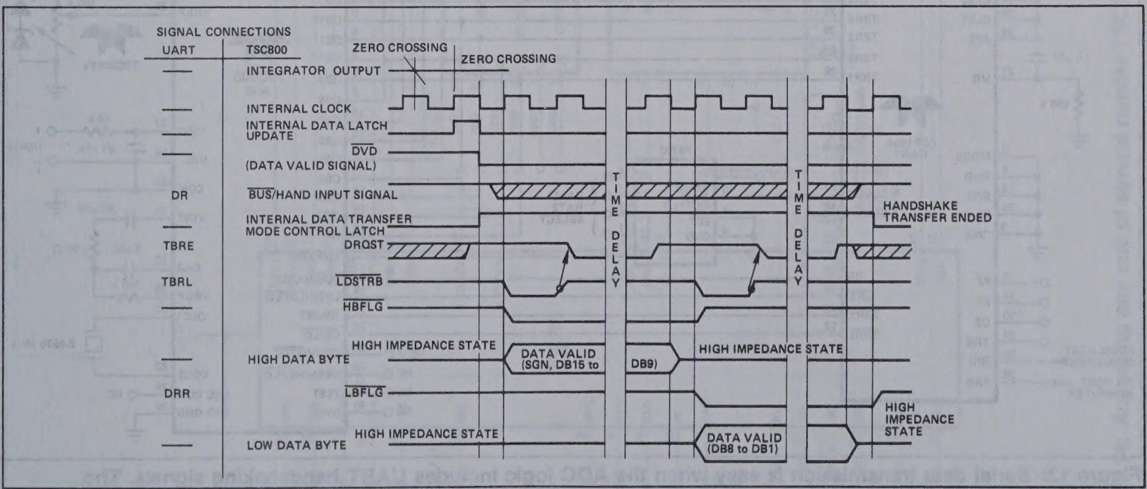

SIGNAL CONNECTIONS
UART
TSC800
ZERO CROSSING
ZERO CROSSING
INTEGRATOR OUTPUT
INTERNAL CLOCK
INTERNAL DATA LATCH UPDATE
DVD
(DATA VALID SIGNAL)
DR
BUS/HAND INPUT SIGNAL
INTERNAL DATA TRANSFER MODE CONTROL LATCH
TBRE
DRQST
TBRL
LDSTRB
HBFLG
HIGH IMPEDANCE STATE
HIGH DATA BYTE
DATA VALID (SGN, DB15 to
DB9)
HIGH IMPEDANCE STATE
DRR
LBFLG
LOW DATA BYTE
HIGH IMPEDANCE STATE
DATA VALID (DB8 to DB1)
TIME DELAY
TIME DELAY
HANDSHAKE TRANSFER ENDED
HIGH IMPEDANCE STATE

Figure 12: UART interface uses data request signal to control handshake data transfer.

The data handshake starts, as before, by the host computer sending a word to the UART. The word's three least significant bits (LSB) address the desired TSC800. The three LSBs are decoded by a three of eight decoder which drives the TSC800 $\overline{\text{BUS}}$/HAND control input. When the word is received, the DR output also goes high. An RC network and CMOS Schmitt trigger delays the DR signal to allow the decoder outputs to settle. The delayed DR pulse enables the decoder and the selected TSC800 is pulsed into the handshake mode. Note that once the handshake mode is entered, the HAND input signal is ingored. The delayed DR output also causes the DATA RECEIVED RESET input to go low. This resets the DR output and disables the decoder until another word is transmitted from the host computer to the UART. The selected TSC800 transmits the last data conversion to the host computer.

Also shown in Figure 14 is a less expensive baud rate generation circuit. A simple CMOS counter can provide common baud rates between 300 and 9600, since the required frequencies are multiples of the 2.4576 MHz TSC800 clock. If more than two ADCs operate from one crystal, the BUF OSC pin should be buffered with an external CMOS buffer.

Interrupt Data Transfer Uses Handshake Mode

The handshake mode is not limited to serial data transmission applications. A system using peripheral I/O circuits like the 6522 or 8255 for interrupt-driven data transfers can use the handshake mode. Only one 8-bit port is required, freeing I/O pins for other tasks. The handshake interface guarantees data will not be accessed as the internal data latches are updated. Two processor interrupts will transfer data.

The TSC800 to 8255 interface in Figure 15 uses HAND tied high. This forces the handshake mode whenever a new conversion is completed. The 8255 negated INPUT BUFFER FULL ($\overline{\text{IBF}_\text{A}}$)signal is the DRQST input signal. $\overline{\text{LDSTRB}}$ strobes data into the 8255 port latch and sets the data request ($\text{IBF}_\text{A} = 1$) signal. DRQST is removed and the TSC800 remains in the handshake mode checking DRQST for the next data byte request. Once IBF is set, the 8255 generates an interrupt request. During the interrupt service routine, port A is read resetting the IBF bit. The second data byte request is generated and the low data byte becomes active. $\overline{\text{LDSTRB}}$ initiates the second interrupt request cycle. A similar interface based on the 6522 is shown in Figure 16.

Versatility and Performance At An Affordable Price

The TSC800 design achieves 0.006% linearity without requiring laser trimming. Self-correction circuits automatically compensate for CMOS amplifier shortcomings. This lowers process complexity and increases reliability; both factors contribute to a modest selling price and low non-delivery risk. A proven metal gate CMOS process was chosen for the TSC800 to guarantee manufacturability. The development programs focused on functional performance, technical specifications, and device producibility. The TSC800 gives the designer interface options and excellent electrical performance at a price that will make new products and systems technically feasible and financially successful.

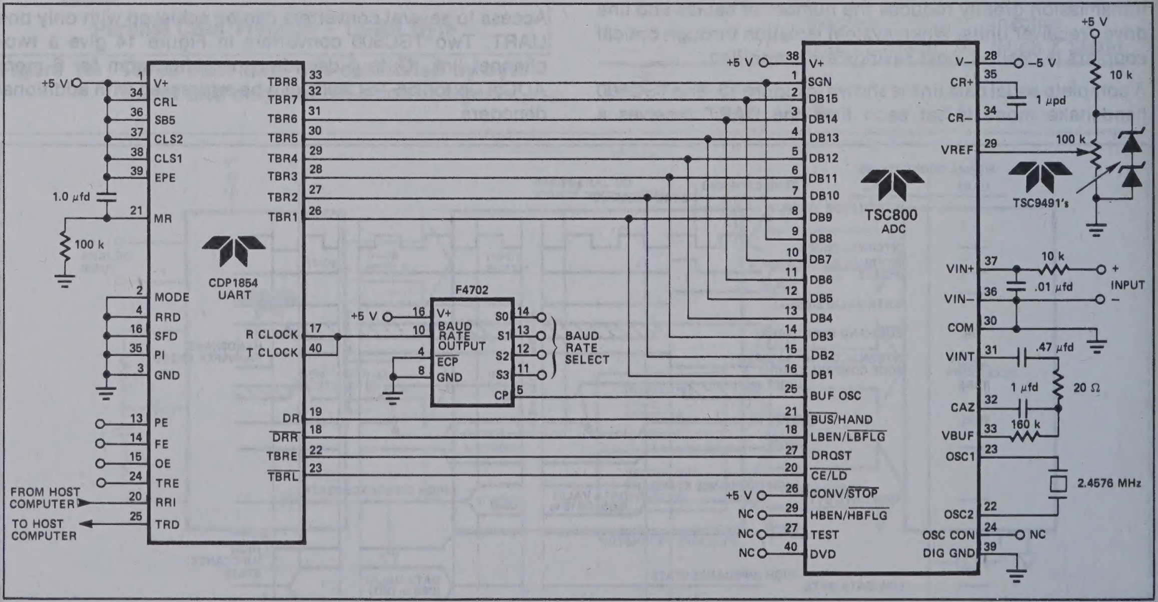

+5 V
V+
CRL
SB5
CLS2
CLS1
EPE
1.0 μfd
MR
100 k
MODE
RRD
SFD
PI
GND
PE
FE
OE
TRE
RRI
TRD
FROM HOST COMPUTER
TO HOST COMPUTER
TBR8
TBR7
TBR6
TBR5
TBR4
TBR3
TBR2
TBR1
CDP1854 UART
R CLOCK
T CLOCK
DR
$\overline{\text{DRR}}$
TBRE
$\overline{\text{TBRL}}$
F4702
BAUD RATE OUTPUT
$\overline{\text{ECP}}$
S0
S1
S2
S3
CP
BAUD RATE SELECT
SGN
DB15
DB14
DB13
DB12
DB11
DB10
DB9
DB8
DB7
DB6
DB5
DB4
DB3
DB2
DB1
BUF OSC
$\overline{\text{BUS}}$/HAND
LBEN/$\overline{\text{LBFLG}}$
DRQST
$\overline{\text{CE/LD}}$
CONV/$\overline{\text{STOP}}$
HBEN/$\overline{\text{HBFLG}}$
TEST
DVD
NC
TSC800 ADC
V−
CR+
CR−
VREF
VIN+
VIN−
COM
VINT
CAZ
VBUF
OSC1
OSC2
OSC CON
DIG GND
−5 V
10 k
1 μpd
100 k
TSC9491's
+ INPUT −
.01 μfd
.47 μfd
1 μfd
20 Ω
160 k
2.4576 MHz

Figure 13: Serial data transmission is easy when the ADC logic includes UART handshaking signals. The TSC800 monitors its DATA REQUEST pin until the UART is ready to receive data.

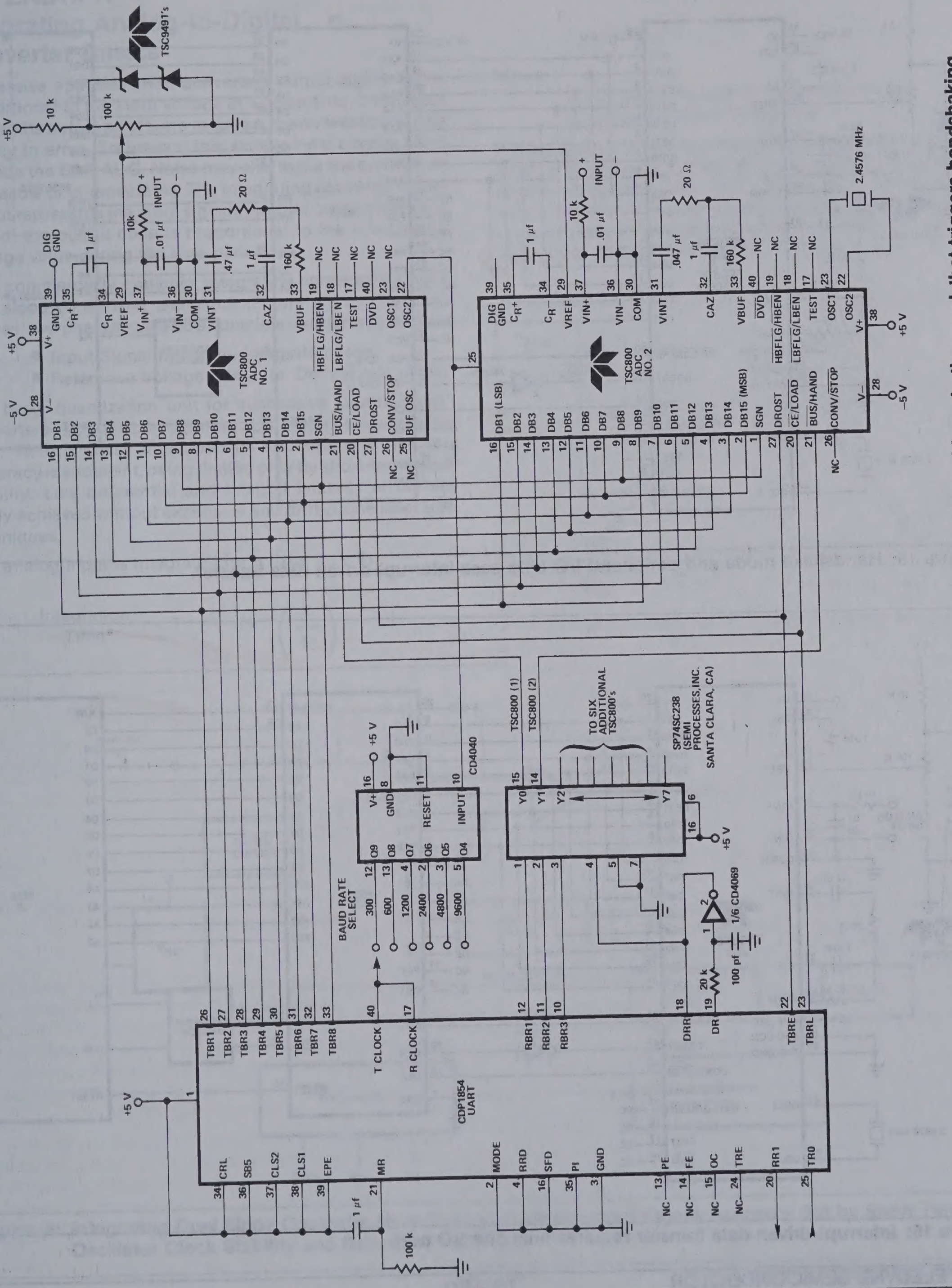

+5 V
10 k
100 k
TSC9491's
DIG GND
1 µf
10k
.01 µf
INPUT
.47 µf
20 Ω
160 k
TSC800 ADC NO. 1
TSC800 ADC NO. 2
-5 V
V+
V−
GND
CR+
CR−
VREF
VIN+
VIN−
COM
VINT
CAZ
VBUF
HBFLG/HBEN
LBFLG/LBEN
TEST
DVD
OSC1
OSC2
DB1 (LSB)
DB15 (MSB)
SGN
BUS/HAND
CE/LOAD
DROST
CONV/STOP
BUF OSC
NC
.047 µf
2.4576 MHz
BAUD RATE SELECT
300
600
1200
2400
4800
9600
CD4040
RESET
INPUT
TSC800 (1)
TSC800 (2)
TO SIX ADDITIONAL TSC800's
SP74SC238 (SEMI PROCESSES, INC. SANTA CLARA, CA)
1/6 CD4069
100 pf
20 k
CDP1854 UART
TBR1
TBR2
TBR3
TBR4
TBR5
TBR6
TBR7
TBR8
T CLOCK
R CLOCK
RBR1
RBR2
RBR3
DRR
DR
TBRE
TBRL
CRL
SBS
CLS2
CLS1
EPE
MR
MODE
RRD
SFD
PI
PE
FE
OC
TRE
RR1
TRO

Figure 14: Accessing any one of several remote TSC800s is simple. Just send the ADC address in the word that triggers handshaking.

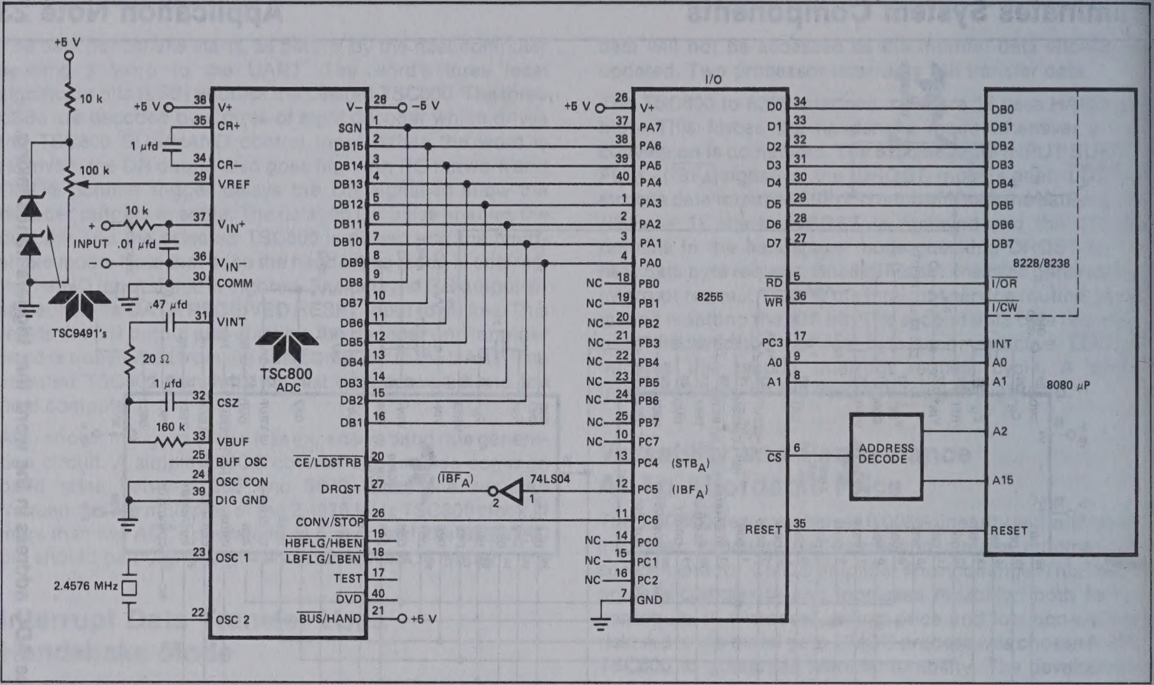

+5 V
10 k
+5 V
1 μfd
100 k
10 k
+ INPUT −
.01 μfd
.47 μfd
TSC9491's
20 Ω
1 μfd
160 k
2.4576 MHz
V+
CR+
CR−
VREF
VIN+
VIN−
COMM
VINT
CSZ
VBUF
BUF OSC
OSC CON
DIG GND
OSC 1
OSC 2
V−
SGN
DB15
DB14
DB13
DB12
DB11
DB10
DB9
DB8
DB7
DB6
DB5
DB4
DB3
DB2
DB1
CE/LDSTRB
DRQST
CONV/STOP
HBFLG/HBEN
LBFLG/LBEN
TEST
DVD
BUS/HAND
−5 V
+5 V
TSC800 ADC
(IBFA)
74LS04
I/O
8255
V+
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC7
PC4 (STBA)
PC5 (IBFA)
PC6
PC0
PC1
PC2
GND
NC
D0
D1
D2
D3
D4
D5
D6
D7
RD
WR
PC3
A0
A1
CS
RESET
ADDRESS DECODE
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
8228/8238
I/OR
I/CW
INT
A0
A1
A2
A15
RESET
8080 μP

Figure 15: Handshake mode and peripheral I/O chip ease interrupt-driven data transfer.

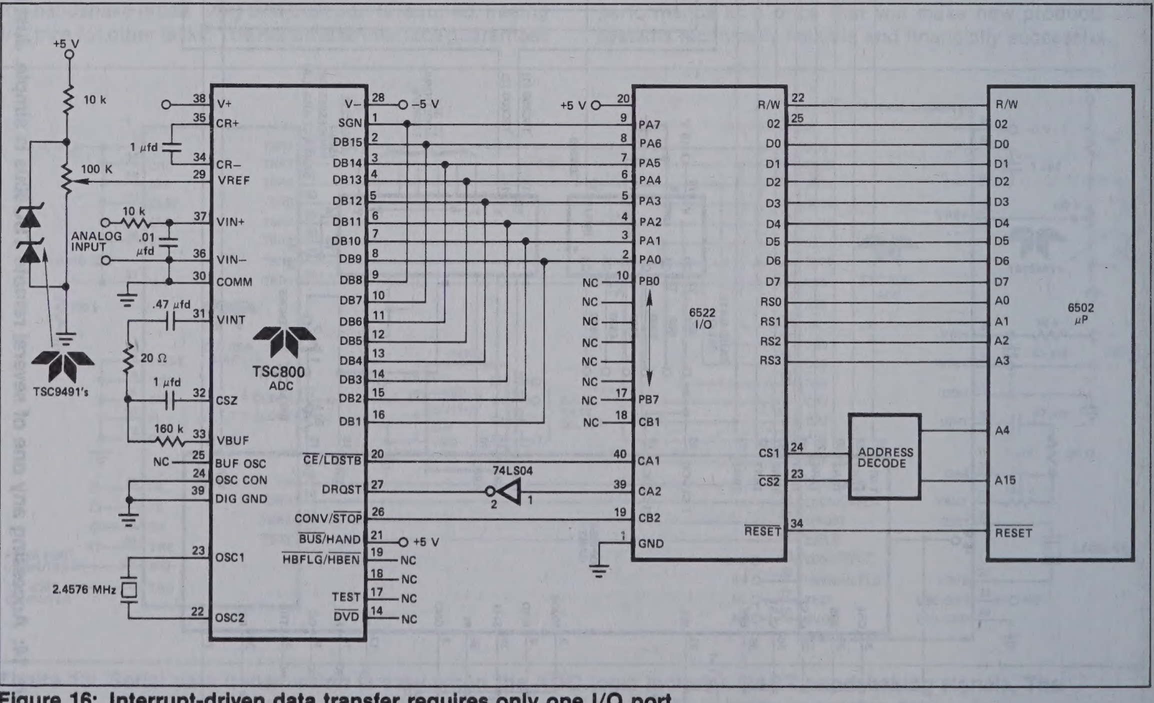

+5 V
10 k
1 μfd
100 K
10 k
ANALOG INPUT
.01 μfd
.47 μfd
TSC9491's
20 Ω
1 μfd
160 k
NC
2.4576 MHz
V+
CR+
CR−
VREF
VIN+
VIN−
COMM
VINT
CSZ
VBUF
BUF OSC
OSC CON
DIG GND
OSC1
OSC2
V−
SGN
DB15
DB14
DB13
DB12
DB11
DB10
DB9
DB8
DB7
DB6
DB5
DB4
DB3
DB2
DB1
CE/LDSTB
DRQST
CONV/STOP
BUS/HAND
HBFLG/HBEN
TEST
DVD
−5 V
+5 V
NC
TSC800 ADC
74LS04
+5 V
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
PB0
PB7
CB1
CA1
CA2
CB2
GND
6522 I/O
R/W
02
D0
D1
D2
D3
D4
D5
D6
D7
RS0
RS1
RS2
RS3
CS1
CS2
RESET
ADDRESS DECODE
6502 μP
A0
A1
A2
A3
A4
A15
RESET

Figure 16: Interrupt-driven data transfer requires only one I/O port.

APPENDIX A
Integrating Analog-to-Digital Converter Basics

Successive approximation converters output digital words proportional to the input voltage at a given time. If the input level shifts before all bits are resolved, the conversion will be grossly in error. To prevent this sample-hold circuits often precede the SAR ADC. Noise may also make the conversion unuseable or unrepeatable. The integrating converter digital output represents the input signals integral over a given time period; the output code is proportional to the input signal average value during the time period.

Most commercially available, integrating converters use the dual slope conversion technique (Figure A). As the name implies, two phases make up a complete measurement cycle:

- Input Signal Integrate: Integrate phase
- Reference Voltage Integrate: Deintegrate phase

The basic quantization unit for successive approximation converters is current. Integrating dual slope converters use time. Time is easily monitored by counting clock pulses. Accuracy is excellent, being limited only by short-term clock stability. Low differential and integral linearity errors are easily achieved without expensive and drift-prone laser trim techniques.

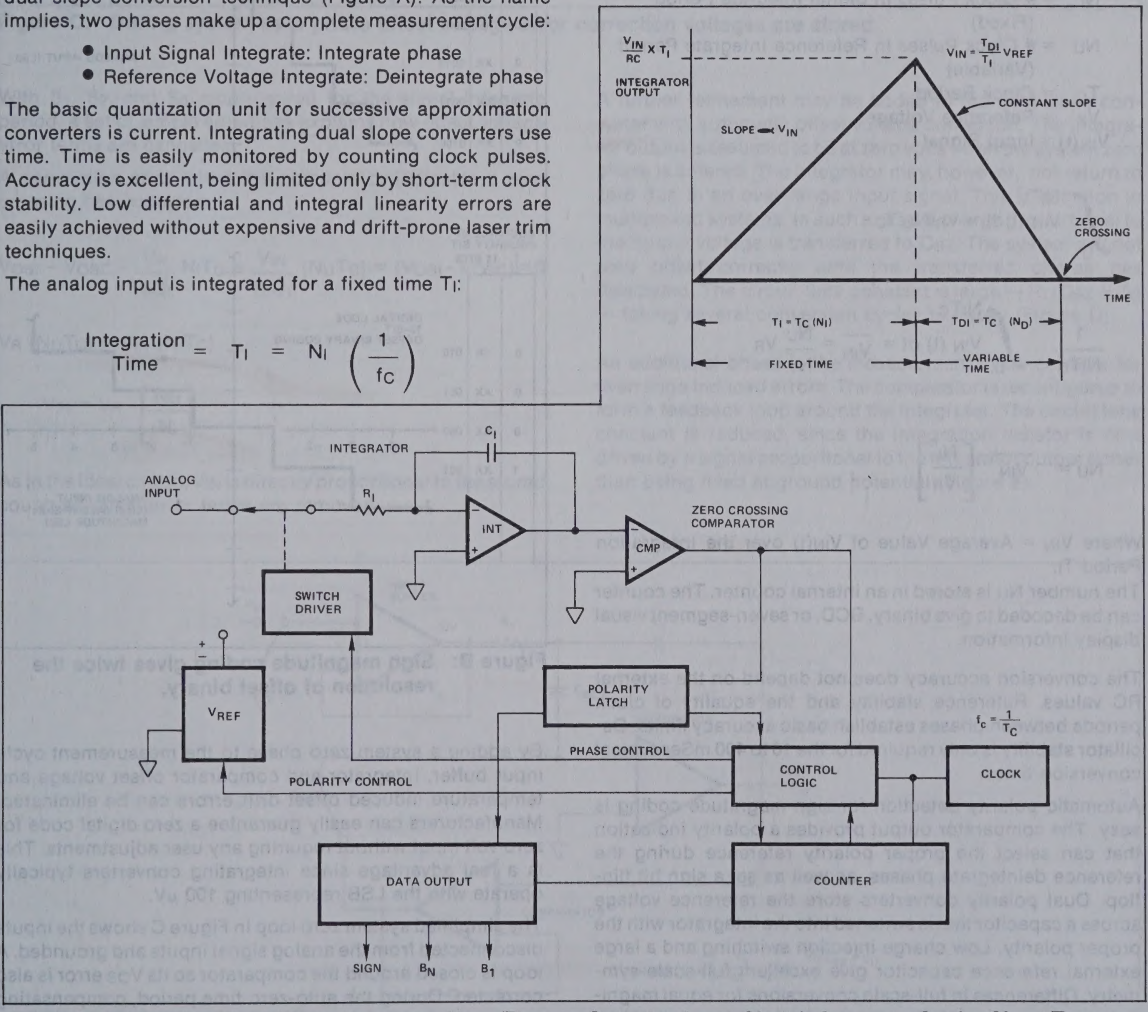
The analog input is integrated for a fixed time T_I:

$$\text{Integration Time} = T_I = N_I\left(\frac{1}{f_C}\right)$$

Where:

N_I = # Clock Periods in Integration Phase
f_C = Counter Clock Frequency

Following the signal integrate phase, a constant magnitude reference voltage is applied to the integrator input. With a polarity opposite to the input signal, the reference signal ramps the integrator output toward zero at a constant rate. A counter totals the number of clock pulses until a comparator signals the integrator has returned to zero volts.



$\frac{V_{IN}}{RC} \times T_I$
INTEGRATOR OUTPUT
$V_{IN} = \frac{T_{DI}}{T_I} V_{REF}$
CONSTANT SLOPE
SLOPE ∝ V_{IN}
ZERO CROSSING
TIME
$T_I = T_C (N_I)$
$T_{DI} = T_C (N_D)$
FIXED TIME
VARIABLE TIME
INTEGRATOR
C_I
ANALOG INPUT
R_I
INT
ZERO CROSSING COMPARATOR
CMP
SWITCH DRIVER
V_{REF}
POLARITY LATCH
$f_c = \frac{1}{T_C}$
PHASE CONTROL
POLARITY CONTROL
CONTROL LOGIC
CLOCK
DATA OUTPUT
COUNTER
SIGN
B_N
B_1

Figure A: Integrating Dual Slope Converter Uses Time to Quantize Input Signal. Accuracy Set by Short Term Oscillator Clock Stability and Reference Stability.

Since the "ramp-up" and "ramp-down" voltages are equal, a simple formula characterizes the conversion:

"Ramp-Up" Voltage — "Ramp-Down" Voltage = 0

$$\frac{1}{RC}\int_0^{N_I T_C} V_{IN}(t)\,dt = \frac{1}{RC}\int_0^{N_U T_C} V_R\,dt$$

Where:

N_I = # Clock Pulses in Signal Integrate Period (Fixed)
N_U = # Clock Pulses in Reference Integrate Period (Variable)
T_C = Clock Period
V_R = Reference Voltage
$V_{IN}(t)$ = Input Signal

$$\int_0^{N_I T_C} V_{IN}(t)dt = V_R N_U T_C$$

$$\frac{1}{N_I T_C}\int_0^{N_I T_C} V_{IN}(t)\,dt = \overline{V_{IN}} = \frac{N_U}{N_1} V_R$$

$$N_U = \overline{V_{IN}}\left[\frac{N_I}{V_R}\right]$$

Where V_{IN} = Average Value of $V_{IN}(t)$ over the Integration Period T_I.
The number N_U is stored in an internal counter. The counter can be decoded to give binary, BCD, or seven-segment visual display information.

The conversion accuracy does not depend on the external RC values. Reference stability and the equality of clock periods between phases establish basic accuracy limits. Oscillator stability is only required for the 10 to 400 mSec typical conversion times.

Automatic polarity detection for sign magnitude coding is easy. The comparator output provides a polarity indication that can select the proper polarity reference during the reference deintegrate phases, as well as set a sign bit flip-flop. Dual polarity converters store the reference voltage across a capacitor that is switched into the integrator with the proper polarity. Low charge injection switching and a large external reference capacitor give excellent full-scale symmetry. Differences in full-scale conversions for equal magnitude but opposite polarity signals can be as low as 1 count. An N bit + sign integration converter has twice the resolution of an N bit offset binary ADC (Figure B). The sign bit is also accurate for signals less than 1 LSB. This can be useful in precision nulling applications.

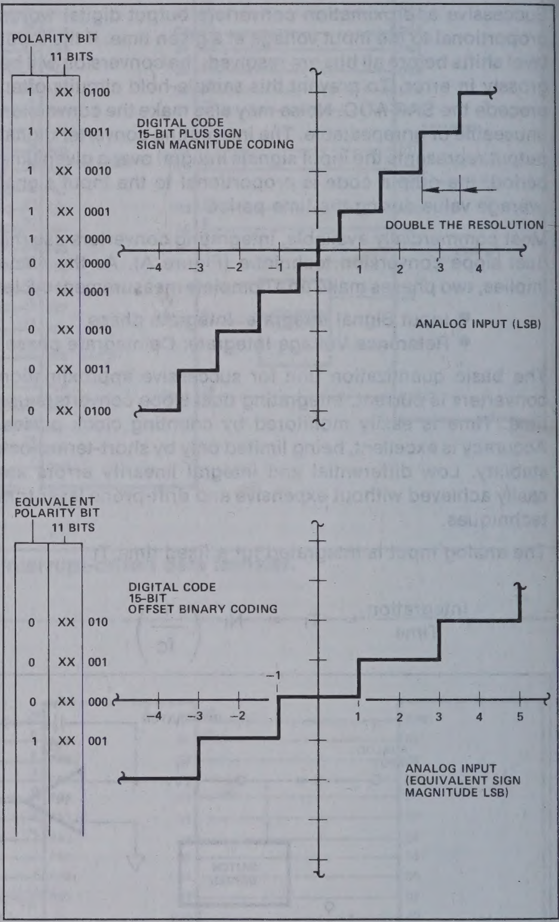

POLARITY BIT
11 BITS
1 XX 0100
1 XX 0011
1 XX 0010
1 XX 0001
1 XX 0000
0 XX 0000
0 XX 0001
0 XX 0010
0 XX 0011
0 XX 0100
DIGITAL CODE
15-BIT PLUS SIGN
SIGN MAGNITUDE CODING
DOUBLE THE RESOLUTION
−4
−3
−2
−1
1
2
3
4
ANALOG INPUT (LSB)
EQUIVALENT
POLARITY BIT
11 BITS
0 XX 010
0 XX 001
0 XX 000
1 XX 001
DIGITAL CODE
15-BIT
OFFSET BINARY CODING
−1
−4
−3
−2
1
2
3
4
5
ANALOG INPUT
(EQUIVALENT SIGN
MAGNITUDE LSB)

Figure B: Sign magnitude coding gives twice the resolution of offset binary.

By adding a system zero phase to the measurement cycle input buffer, integrator and comparator offset voltage and temperature induced offset drift errors can be eliminated. Manufacturers can easily guarantee a zero digital code for zero volt input without requiring any user adjustments. This is a real advantage since integrating converters typically operate with the LSB representing 100 μV.

The simplified system zero loop in Figure C shows the inputs disconnected from the analog signal inputs and grounded. A loop is closed around the comparator so its V_{OS} error is also corrected. During the auto-zero time period, compensating error voltages are stored on the system zero capacitor C_{AZ} and integration capacitor C_I.

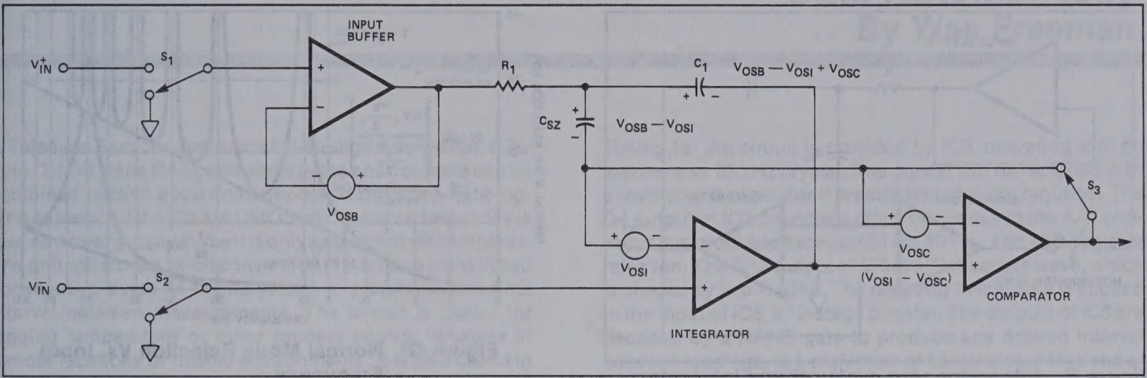

INPUT BUFFER
V_{IN}^{+}
S_1
R_1
C_1
$V_{OSB} - V_{OSI} + V_{OSC}$
C_{SZ}
$V_{OSB} - V_{OSI}$
V_{OSB}
V_{OSI}
V_{OSC}
S_3
V_{IN}^{-}
S_2
$(V_{OSI} - V_{OSC})$
COMPARATOR
INTEGRATOR

Figure C: During system zero phase offset voltage error correction voltages are stored.

With S_1, S_2, and S_3 reconfigured for the signal integrate period, a set of simple equations explains how offset voltage error terms are cancelled.

A conversion ends when the comparator indicates a zero crossing has occurred:

$$V_{OSI} - V_{OSC} - \frac{V_R}{R_I C_I} N_I T_C + \frac{V_{IN}}{R_I C_I} (N_U T_C) = (V_{OSI} - V_{OSC}) = 0$$

$$V_R (N_U T_C) = V_{IN} (N_I T_C)$$

$$V_{IN} = V_R \left[\frac{N_U}{N_I}\right]$$

As in the ideal circuit, V_{IN} is directly proportional to the stored count; all offset error terms are removed.

A further refinement may be added to the dual slope converter with automatic offset voltage correction. The integrator output is assumed to be at zero volts when the system zero phase is entered. The integrator may, however, not return to zero due to an over-range input signal. This is common in multiplexed systems. In such a case, a charge proportional to the output voltage is transferred to C_{SZ}. The system will not zero offset correctly until the transferred charge has dissipated. The circuit time constant is large — $R_I (C_{SZ} + C_I)$ — taking several conversion cycles to decay (Figure D).

An additional phase in the measurement cycle corrects for overrange induced errors. The comparator is reconfigured to form a feedback loop around the integrator. The circuit time constant is reduced, since the integration resistor is now driven by a signal proportional to the integrator output rather than being fixed at ground potential (Figure E).

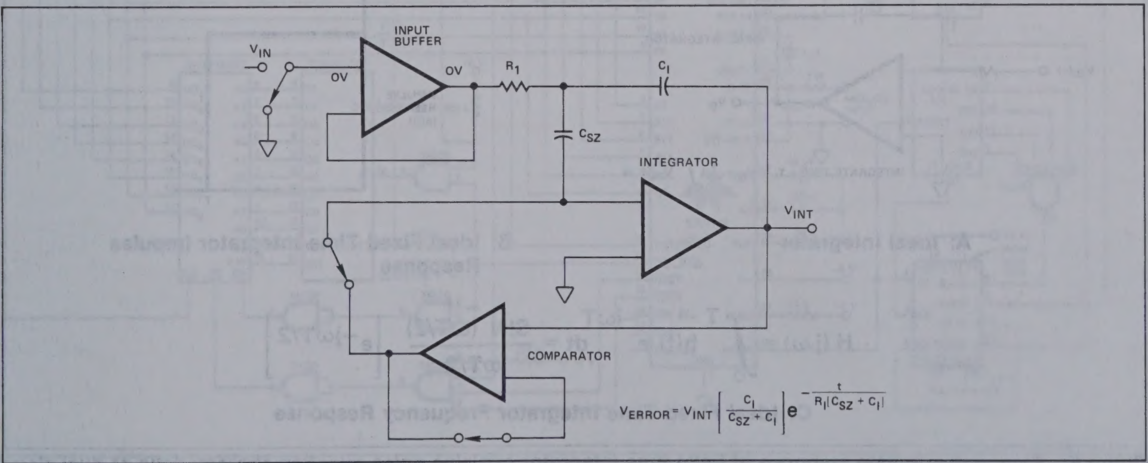

INPUT BUFFER
V_{IN}
OV
OV
R_1
C_I
C_{SZ}
INTEGRATOR
V_{INT}
COMPARATOR
$V_{ERROR} = V_{INT} \left[\frac{C_I}{C_{SZ} + C_I}\right] e^{-\frac{t}{R_I (C_{SZ} + C_I)}}$

Figure D: Non-zero integrator output causes error when system zero cycle is entered.

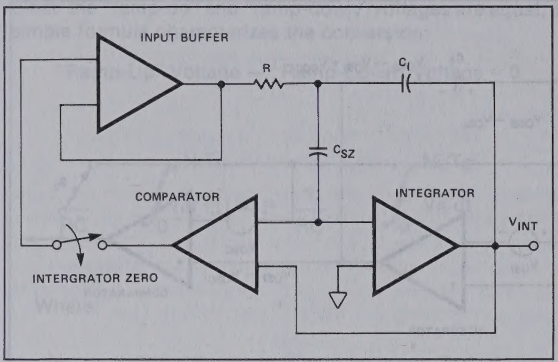


Figure E: **Integrator zero cycle returns integrator output to zero volts before system zero cycle is entered.**

Integrating converters provide noise rejection automatically with at least a 20 dB/decade attenuation rate. In addition, interference signals with frequencies at integral multiples of the integration period are theoretically completely removed. This intuitively makes sense, since the average value of a sine wave of frequency 1/T averaged over a period T is zero. The finite time integrator frequency attenuation characteristic is easily derived by doing a Fourier transform on the circuits impulse response function (Figure F).

Integrating converters often establish the integration period to reject 50/60 Hz line frequency interference signals. The ability to reject such signals is shown in a normal mode rejection plot (Figure G). Normal mode rejection is practically set to 50-65 dB, since the 50/60 Hz line frequency can deviate by a few tenths of a percent (Figure H).

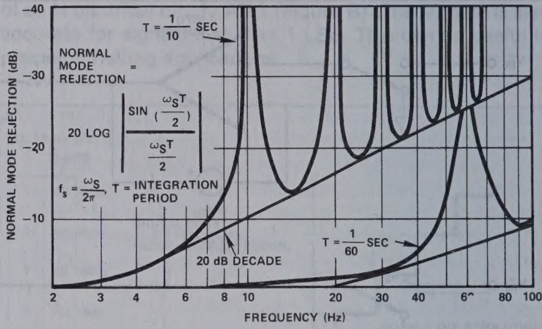


Figure G: **Normal Mode Rejection Vs. Input Frequency.**

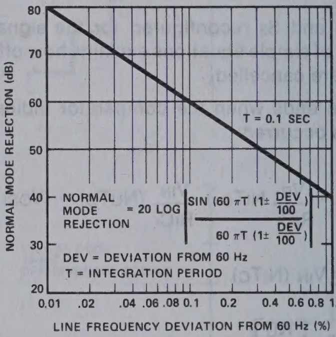
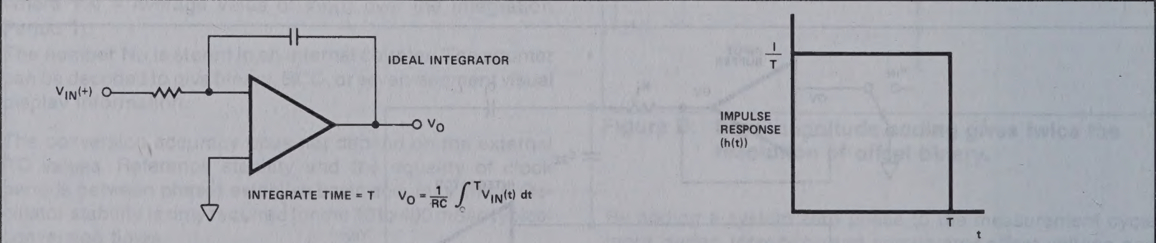


Figure H: **Integrating converter normal mode rejection vs. 60 Hz line frequency variations.**



A: Ideal Integrator

B: Ideal Fixed Time Integrator Impulse Response

$$H(j\omega) = \int_0^T h(t)\, e^{-j\omega T}\, dt = \frac{\text{SIN }(\omega T/2)}{\omega T/2}\left[e^{-j\omega T/2}\right]$$

C: Ideal Fixed Time Integrator Frequency Response

Figure F: **Frequency domain response of finite time integrator explains noise rejection characteristic of dual slope ADC.**

TELEDYNE
SEMICONDUCTOR

Application Note 24

TSC7109 Records Remote Data Automatically

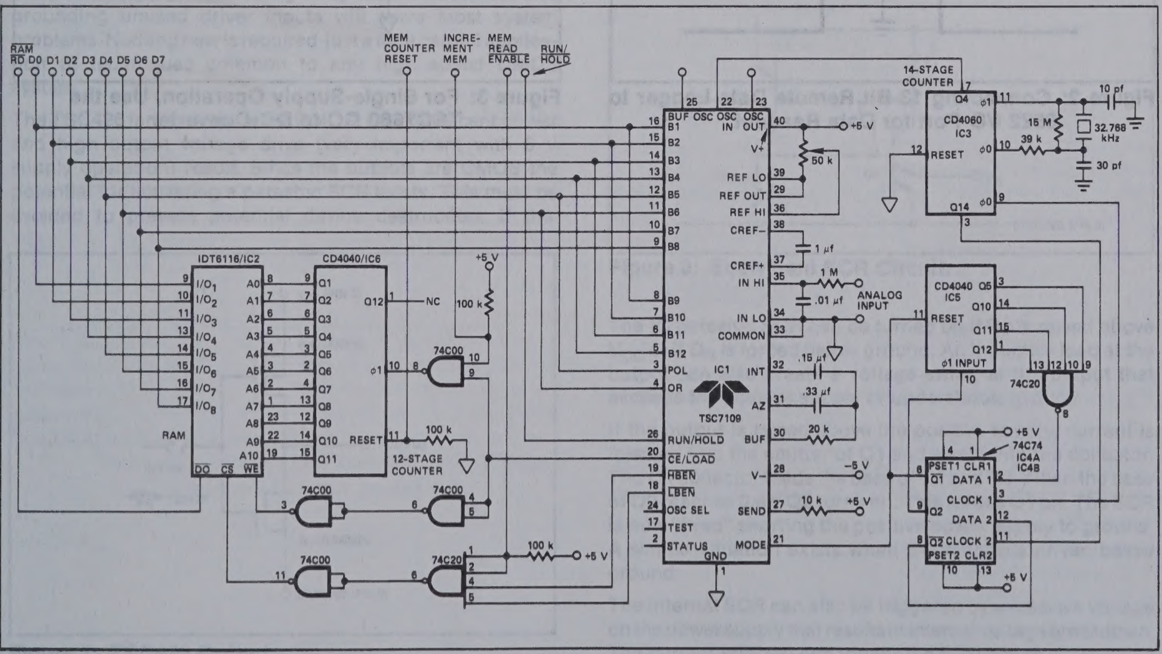
By Wes Freeman

A Teledyne Semiconductor analog-to-digital converter, a 2k-byte CMOS static RAM, and some gates and counters can be combined to form a low cost, flexible, stand alone data logging system. All the ICs are CMOS and the clock frequency is low, so power supply current is only a couple of milliamperes. The unit will store a 13-bit conversion (12-bit plus sign) in two consecutive bytes of memory, with a programmable time interval between measurements. The circuit is useful for logging temperature or other process control variables in remote locations or hostile environments. It is also useful in the lab for making unattended, repetitive measurements of long term drift, component aging, etc.

The heart of the circuit is a TSC7109 (IC1), a 12-bit plus sign CMOS A/D converter. The TSC7109 has a handshake mode in which the result of the latest conversion is output, in two consecutive bytes, each time the MODE input is strobed high. The data logger stores each byte in sequential RAM locations for later processing by a host computer. The IDT 6116 CMOS static RAM stores 2048 bytes and therefore can store 1024 readings. This permits, for example, one 13-bit measurement per hour for seven weeks.

Timing for the circuit is provided by IC3, operating with an inexpensive 32 kHz crystal. The crystal can be replaced with a resistor and capacitor if precise timing is not required. The Q4 output of IC3 provides a clock frequency to the A/D converter that produces excellent 50 Hz, 60 Hz, and 400 Hz noise rejection. The Q12 output of IC3 is a 2 Hz square wave, which is divided by two in IC4A. The resulting 1 Hz output is applied to the input of IC5, a 12-stage counter. The outputs of IC5 are decoded by a NAND gate to produce any desired interval between readings, to a maximum of 68 minutes. At the end of the time interval, IC4B generates a pulse which resets the counter and places the TSC7109 in the handshake mode.

When the TSC7109's MODE input is pulsed high, the result of the latest conversion is output in two bytes. First, $\overline{\text{HBEN}}$ goes low, outputs B9 through B12, POL and OR become active, and $\overline{\text{CE}}/\overline{\text{LOAD}}$ goes low. After one clock cycle $\overline{\text{CE}}/\overline{\text{LOAD}}$ goes high and the high byte of the conversion is latched into memory. The rising edge of $\overline{\text{CE}}/\overline{\text{LOAD}}$ also increments IC6, to address the next memory location. Then $\overline{\text{HBEN}}$ goes high, $\overline{\text{LBEN}}$ goes low, outputs B1 through B8 become active and $\overline{\text{CE}}/\overline{\text{LOAD}}$ again goes low for one clock cycle. After $\overline{\text{CE}}$/



RAM RD
D0 D1 D2 D3 D4 D5 D6 D7
MEM COUNTER RESET
INCRE-MENT MEM
MEM READ ENABLE
RUN/HOLD
IDT6116/IC2
I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 I/O8
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
RAM
DO CS WE
CD4040/IC6
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11
Q12
NC
ϕ1
RESET
12-STAGE COUNTER
+5 V
100 k
74C00
74C20
BUF OSC OSC IN OSC OUT
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12
POL
OR
RUN/HOLD
CE/LOAD
HBEN
LBEN
OSC SEL
TEST
STATUS
GND
V+
REF LO
REF OUT
REF HI
CREF−
CREF+
IN HI
IN LO
COMMON
INT
AZ
BUF
V−
SEND
MODE
IC1
TSC7109
50 k
1 µf
1 M
.01 µf
ANALOG INPUT
.15 µf
.33 µf
20 k
−5 V
10 k
14-STAGE COUNTER
CD4060 IC3
Q4 ϕ1 ϕ0 ϕ0 Q14
RESET
10 pf
15 M
39 k
32.768 kHz
30 pf
CD4040 IC5
Q5 Q10 Q11 Q12
ϕ1 INPUT
74C74 IC4A IC4B
PSET1 CLR1
Q1 DATA 1
CLOCK 1
Q2 DATA 2
Q2 CLOCK 2
PSET2 CLR2

Figure 1: 13-Bit Remote Data Logger

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$\overline{\text{LOAD}}$ goes high the low byte of the conversion is latched into memory, IC6 is again incremented, $\overline{\text{LBEN}}$ goes high and the data outputs return to their high impedance state.

Data can be read out of RAM by any micro or minicomputer. An I/O port with handshaking (6522, Z8420, 8255A, etc.) makes the task easy. The I/O port is simply programmed to prooduce a handshake strobe when the port is read. The strobe then increments IC6 after each byte is read and-sequences through RAM automatically. Figure 2 shows pin connections for a 6522 I/O device.

Because of CMOS's low power requirements, battery power is ideal for the data logger. Average power dissipation of the TSC7109 is only 10.5 mW, and the IDT 6116 is in its power-down mode (Isy = 20 μA) except for the time when $\overline{\text{CS}}$ is low. Power dissipation, therefore, is only about 15 mW. On-board battery operation allows modules to be exchanged at remote locations and returned to a central location for data removal and analysis without danger of data loss.

The TSC7660, a DC to DC converter, permits the circuit to operate from a single power supply. This CMOS device contains a switch matrix and on-board oscillator which convert a positive voltage to negative polarity with a power efficiency of about 98%. Using the TSC7660, as shown in figure 3, permits the circuit to operate, for example, on two small 3-volt lithium cells.

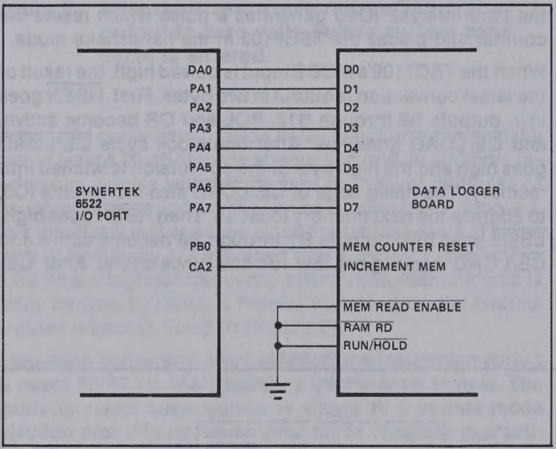
DA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
SYNERTEK
6522
I/O PORT
PB0
CA2
D0
D1
D2
D3
D4
D5
D6
D7
DATA LOGGER
BOARD
MEM COUNTER RESET
INCREMENT MEM
MEM READ ENABLE
RAM RD
RUN/HOLD

Figure 2: Connecting 13-Bit Remote Data Logger to 6522 I/O Port for Data Readout.

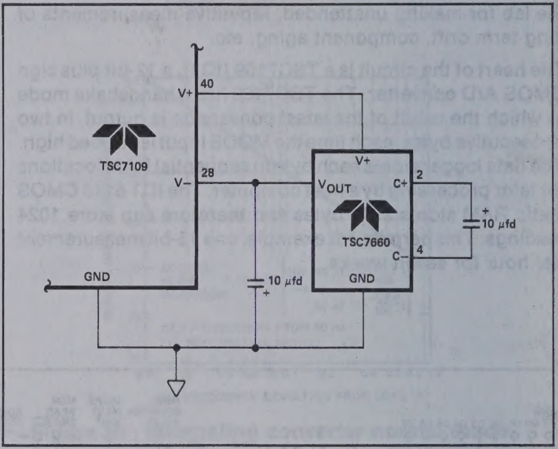
40
V+
TSC7109
28
V−
GND
V+
VOUT
C+
2
TSC7660
4
C−
GND
10 μfd
10 μfd

Figure 3: For Single-Supply Operation, Use the TSC7660 DC to DC Converter

TELEDYNE SEMICONDUCTOR

Application Note 25
TSC426/427/428 System Design Practice
By David Gillooly

The TSC426/427/428 fast switching times are made possible by a low impedance CMOS output stage. The high peak currents make 30 ns rise/fall times possible.

The rapid rise/fall times do, however, require systems be designed with adequate power supply decoupling and stray lead inductance minimization. Practices which are adequate for 1 μs rise/fall times and 20 mA peak currents will not be adequate with TSC426 family. The same laws of physics apply in both systems. The results may be negligible in one and of prime importance in another.

For example, a 0.1 μH power lead inductance (4" of 0.025" diam. wire) can cause a voltage spike 1000 times larger in a fast system with an unbypassed supply.

Low Speed System	**High Speed System**
$L_S = 0.1\ \mu H$	$L_S = 0.1\ \mu H$
$\Delta V_{OUT} = 18\ V$	$\Delta V_{OUT} = 18\ V$
$t = 1\ \mu s$	$t = 30\ ns$
$I_{PK} = 20\ mA$	$I_{PK} = 600\ mA$
$C_L = 1000\ pf$	$C_L = 1000\ pf$
$\Delta V_{supply} = L \frac{dI}{dt}$	$\Delta V_{supply} = L \frac{dI}{dt}$
$= 2\ mV$	$= 2.0\ V$

The system design practices needed are not difficult to apply. The simple good engineering practice of bypassing the power supply, minimizing stray lead inductance, and grounding unused driver inputs will solve most system problems. Nothing new is required-just a little careful application of techniques common to any high speed CMOS system.

The TSC426 family outputs are CMOS. Low quiescent power and high output voltage drive (very important with 5 V supply operation) result. Since the outputs are CMOS the potential for activating a parasitic SCR exists. This must be avoided to prevent potential device destruction. If the TSC 426 output, like any CMOS chip, is driven below ground or above the positive power supply an internal parasitic SCR can be turned on. The high current flow can damage the device. The actual TSC426 output stage is shown in Figure 1. The IC layout and simplified equivalent SCR circuit are shown in Figures 2 and 3.

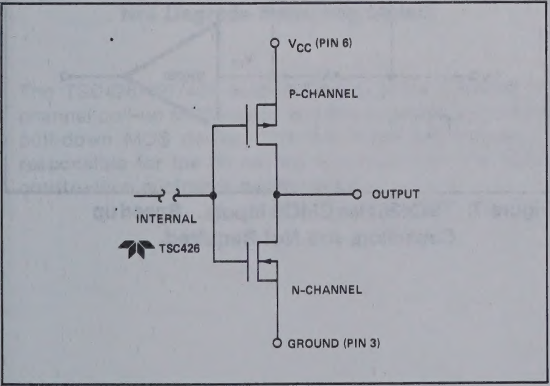

Figure 1: TSC426 Output.

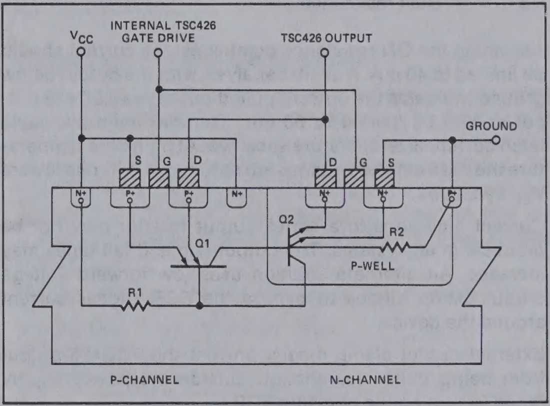

Figure 2: Output Stage IC Layout.

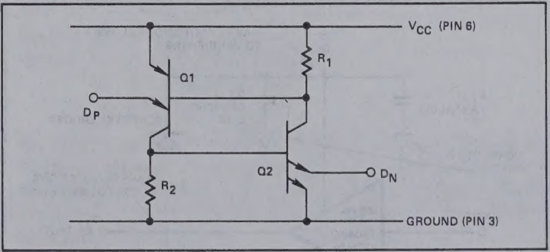

Figure 3: Equivalent SCR Circuit.

The IC parasitic SCR can be turned on if Dp is raised above V_{CC} or if D_N is forced below ground. An inductive load at the output can also create a voltage swing at the output that exceeds the positive supply or undershoots ground.

If the output is raised above the positive supply, current is injected into the emitter of Q1 and swept into the collector. The Q1 collector feeds the base of Q2 and R2. When the base of Q2 reaches 0.6 V Q2 turns on. This forces Q1 on. The SCR is now "fired" shorting the positive power supply to ground. A similar situation exists when the output is driven below ground.

The internal SCR can also be triggered by excessive voltage on the power supply that results in internal voltage breakdown. The current injected can trigger the SCR action.

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By limiting the current injected into the TSC426 output when the output is above the positive power supply latch up is avoided. The limiting current is:

$$I \le \frac{V_{BE}}{R2 \parallel RONP}$$

where:

RONP = ON resistance of P channel device. (15 ohms maximum)
V_{BE} = Q_2 base emitter turn on voltage. (Approximately 0.6 V)
R2 = Bulk resistance

Assuming the ON resistance dominates, the current should be limited to 40 mA. A similar analysis with the output below ground indicates the current pulled out of the TSC426 output should be limited to 60 mA. The maximum allowable latch current is temperature sensitive. At high chip temperature the base emitter voltages are reduced. A 1 °C rise lowers V_{BE} by 2.2 mV.

Current limiting with a series output resistor may not be practical in all systems. The output rise and fall times may increase. An alternate solution uses low forward voltage output clamp diodes to bypass the SCR trigger current around the device.

External output clamp diodes prevent the TSC426 output from being pulled far enough outside the power supply range to turn on the parasitic SCR.

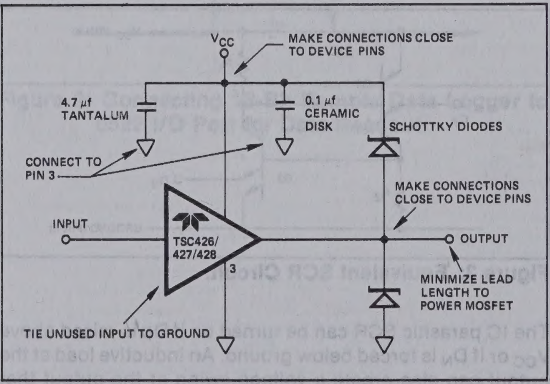
VCC
MAKE CONNECTIONS CLOSE TO DEVICE PINS
4.7 µf TANTALUM
0.1 µf CERAMIC DISK
SCHOTTKY DIODES
CONNECT TO PIN 3
MAKE CONNECTIONS CLOSE TO DEVICE PINS
INPUT
TSC426/ 427/428
OUTPUT
3
MINIMIZE LEAD LENGTH TO POWER MOSFET
TIE UNUSED INPUT TO GROUND

Figure 4: Diode Output Clamp Prevents SCR Action.

The external diodes must have a lower forward on base to emitter voltage than the parasitic transistor junctions. Schottky small signal diodes are suitable. Several possible types are:

- Hewlett Packard: P/N 5082-2303
- Motorola: P/N MBR120P
- Varo: P/N VSB52 (Four diode bridge)

To be effective the output clamp diodes must be connected close to the output, supply and ground device pins.

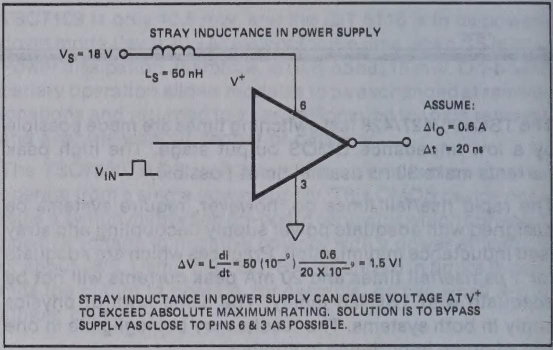
STRAY INDUCTANCE IN POWER SUPPLY
V_S = 18 V
L_S = 50 nH
V^+
6
3
V_{IN}
ASSUME:
ΔI_O = 0.6 A
Δt = 20 ns
$\Delta V = L\frac{di}{dt} = 50\,(10^{-9})\frac{0.6}{20 \times 10^{-9}} = 1.5\ V!$
STRAY INDUCTANCE IN POWER SUPPLY CAN CAUSE VOLTAGE AT V+ TO EXCEED ABSOLUTE MAXIMUM RATING. SOLUTION IS TO BYPASS SUPPLY AS CLOSE TO PINS 6 & 3 AS POSSIBLE.

Figure 5: Stray Supply Lead Inductance Can Decrease Reliability.

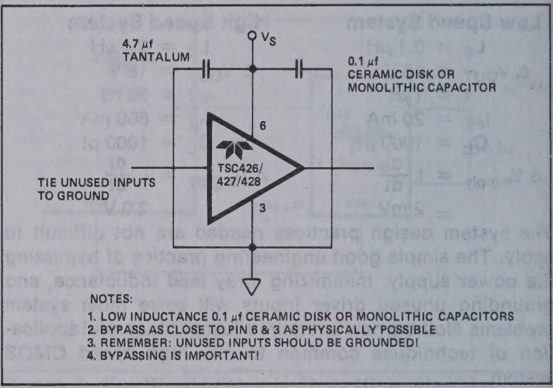
V_S
4.7 µf TANTALUM
0.1 µf CERAMIC DISK OR MONOLITHIC CAPACITOR
6
TSC426/ 427/428
TIE UNUSED INPUTS TO GROUND
3
NOTES:
1. LOW INDUCTANCE 0.1 µf CERAMIC DISK OR MONOLITHIC CAPACITORS
2. BYPASS AS CLOSE TO PIN 6 & 3 AS PHYSICALLY POSSIBLE
3. REMEMBER: UNUSED INPUTS SHOULD BE GROUNDED!
4. BYPASSING IS IMPORTANT!

Figure 6: Suggested Bypass Procedure.

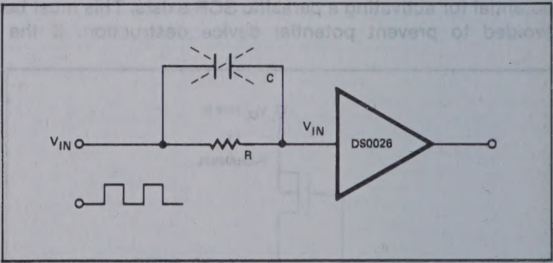
C
V_{IN}
R
V_{IN}
DS0026

Figure 7: TSC426 Has CMOS Inputs. Speedup Capacitors Are Not Required.

Supply bypass capacitors must also be connected between V_{CC} (Pin 6) and Ground (Pin 3). Connections must be close to the actual device pins (approx. 0.5"). A 0.1 μf ceramic disk capacitor in parallel with a 4.7 μf tantalum capacitor is suggested. Without supply bypassing, power supply lead inductance can cause voltage breakdown. The bypass capacitors also supply the transient current needed during capacitive load charging.

A 10 to 15 ohm resistor in series with the power supply filters voltage spikes present at the TSC426/427/428 supply terminal. Should latch up occur, this will also limit current. Rise and fall time will not be affected if the recommended supply bypassing is used. See Figure 8.

The DS0026 has a bipolar input. A speed up capacitor is normally used to decrease switching time. Base storage time is reduced. The capacitor causes a voltage spike drive at the input that extends beyond V_{CC} or ground. The TSC426 input is CMOS and does not require a speed up capacitor. In converting DS0026 sockets to the TSC426/427/428 the capacitor should be removed. This will maximize drive to the device and minimize transition time. Benefits include fewer components and reduced insertion costs. See Figure 8.

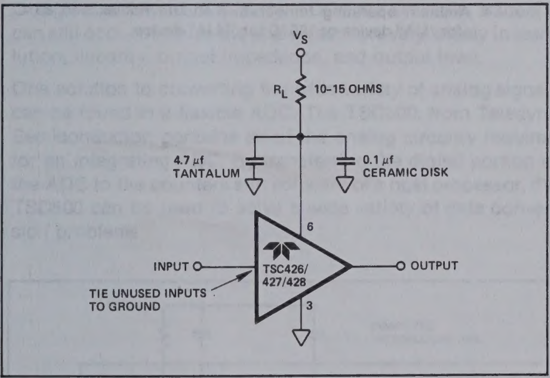

Figure 8: R_L Current Limiting Protects Device and Will Not Degrade Switching Speed.

The TSC426/427/428 outputs feature a low impedance P channel pull-up MOS device and low impedance N channel pull-down MOS device. The low resistance outputs are responsible for the 30 ns rise and fall times. The CMOS construction minimizes current drain.

The output N and P channel devices should not be forced to conduct current simultaneously. This can happen if an unused input is left floating. Unused inputs **must be connected to ground or the positive supply.** A ground connection will minimize steady state supply current. This is common engineering practice followed in CMOS logic system design but is sometimes overlooked during a "quick" bench evaluation. Floating inputs cause excessive current flow and may potentially destroy the driver.

The input drive signal should also have rise and fall times less than 1 μs. This minimizes time spent in the output stage transition region.

Package Power Dissipation

Input signal duty cycle, power supply voltage, and capacitive load influence package power dissipation. Given power dissipation and package thermal resistance the maximum ambient operation temperature is easily calculated. The CerDIP 8-pin package junction to ambient thermal resistance is 150°C/W. At 25°C the package is rated at 800 mW maximum dissipation. Maximum allowable chip temperature is 150°C.

Three components make up total package power dissipation:

- Capacitive load dissipation (P_C)
- Quiescent power (P_Q)
- Transition power (P_T)

The capacitive load caused dissipation is a direct function of frequency, capacitive load, and supply voltage. The package power dissipation per driver is:

EQ. 1: $P_C = f\,C\,V_S{}^2$

where: F = switching frequency
C = capacitive load
V_S = supply voltage

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low power dissipation mode with only 0.4 mA total current drain. Logic high signals raise the current to 8 mA maximum. The quiescent power dissipation per driver is:

EQ. 2: $$P_Q = \frac{V_S}{2}\,(D\,(I_H) + (1\text{-}D)\,I_L)$$

where: I_H = quiescent current with both inputs high (8 mA Max)
I_L = quiescent current with both inputs low (0.4 mA Max)
D = duty cycle

Transition power dissipation is normally not significant. It arises because the output stage N and P channel MOS transistors are on simultaneously for a very short period when the output changes. The transition package power dissipation per driver is approximately:

EQ. 3: $P_T = f\ V_S\ (1.63 \times 10^{-9})$

An example shows the relative magnitude for each term. Both drivers are driven with a 50% duty cycle signal at the same frequency. Capacitive load is the same for each driver.

Example 1:
$C = 1000$ pf
$V_S = 18$ V
$D = 50\%$
$f = 200$ kHz
$P_D =$ Package power dissipation $= P_C + P_T + P_Q$
$= 130$ mW $+ 11.7$ mW $+ 38$ mW
$= 180$ mW
Max. operating temperature $= T_J - \theta_{JA}\ (P_D)$
$= 123\,°C$

where:
T_V = Max. allowable junction temperature (150°C)
θ_{JA} = Junction to ambient thermal resistance (150°C/W, CerDIP)

Table 1 gives the total package power dissipation for several different cases using the formulas developed above. If only one driver is active divide the package power dissipation numbers by two in Table 1.

Table 1: TSC426 Package Power Dissipation

			Package Power Dissipation CerDIP Package [$\theta_{JA} = 150\,°C/W$]				
Capacitive Load [pF]	Input Frequency [kHz]	Supply Voltage [V]	Input Stage Power [mW]	AC Power [mW]	Spike Power [mW]	Total Power [mW]	Max Ambient Operating Temp [° C]
1000	50	18	75	32	2	109	125
1000	100	18	75	64	5	144	125
1000	200	18	75	129	11	215	117
1000	400	18	75	259	23	357	96
1000	1000	18	75	648	58	781	32
1000	50	12	50	14	1	65	125
1000	100	12	50	28	3	81	125
1000	200	12	50	57	7	114	125
1000	400	12	50	115	15	180	122
1000	1000	12	50	288	39	377	93
2000	50	18	75	64	2	141	125
1000	1800	12	50	518	70	638	54
50	4000	18	75	129	234	438	84
1000	100	18	75	64	5	144	125
500	100	18	75	32	5	112	125
500	200	15	63	45	9	117	125
500	100	15	63	22	4	89	125

Notes:
1. Duty Cycle = 50%.
2. Each input driven.
3. Each output with load C.
4. Ambient operating temperature should not exceed 85°C for "IJA" device or 125°C for "MJA" device.

TELEDYNE
SEMICONDUCTOR

Application Note 26

Flexible TSC500 ADC Simplifies Design Tradeoffs

By Wes Freeman

Designers who need to convert analog signals to digital rapidly gain respect for the word "tradeoff." At first glance, the wide variety of analog-to-digital converter (ADC) products available would indicate that the "perfect" ADC for any application is readily available. All of these products, however, involve tradeoffs in speed, power consumption, accuracy, price, and flexibilty, among others. These trade-offs are not mere specmanship, either. Speed, price, and power consumption, for example, can vary by orders of magnitude from product to product.

The overriding ADC tradeoff is usually speed. Digitizing high speed signals typically requires a successive approximation or flash ADC. The designer must then accept the cost and power penalties which usually accompany these devices.

Many analog phenomena, however, change slowly. Commonly measured physical events, for example, include temperature, humidity, pressure, strain, and pH. The dual-slope integrating ADC is the typical choice for low speed conversion, due to its high resolution at low cost and low power. Even though a variety of dual-slope ADCs are available, tradeoffs can still occur because the analog sensors vary widely in resolution, linearity, output impedance, and output level.

One solution to converting the wide variety of analog signals can be found in a flexible ADC. The TSC500, from Teledyne Semiconductor, contains all of the analog circuitry required for an integrating ADC. By transferring the digital portion of the ADC to the counters and software of a host processor, the TSC500 can be used to solve a wide variety of data conversion problems.

The TSC500 gives the design engineer powerful control over the resolution/conversion-speed tradeoff, while adding flexible input voltage scaling. Also, this flexibilty is made available at low cost and with only 10 mW power dissipation.

A typical ADC and microprocessor interface is shown in Figure 1. Notice that the digital functions of the ADC are duplicated in the microprocessor. Replicating these circuits on the ADC simplifies software development, because the conversion result is merely read as one or more memory locations. Although the hardware interface also seems to be simple, the package size and large number of I/O lines necessary can be a real limitation in small systems or with single-chip microcomputers which are not bus oriented.

Figure 2 shows the TSC500 and microprocessor interface. The counters, control logic, and most I/O functions have been moved to the microprocessor. Only three I/O lines are required, and both the size and cost of the ADC are reduced. More importantly, the designer can now specify the ADC resolution instead of selecting whatever is available in an existing product.

The TSC500 permits control of the conversion's resolution because resolution is determined by the host processor's software. With standard ADCs, resolution is determined by hardware on the chip. The designer who needs, for example, .04% resolution is forced to use a 12-bit ADC with .025% resolution. By using the TSC500, however, a 2500-count full-scale output is as easy to design as a 4096 count (12-bit) output, but yields a 40% increase in conversion speed.

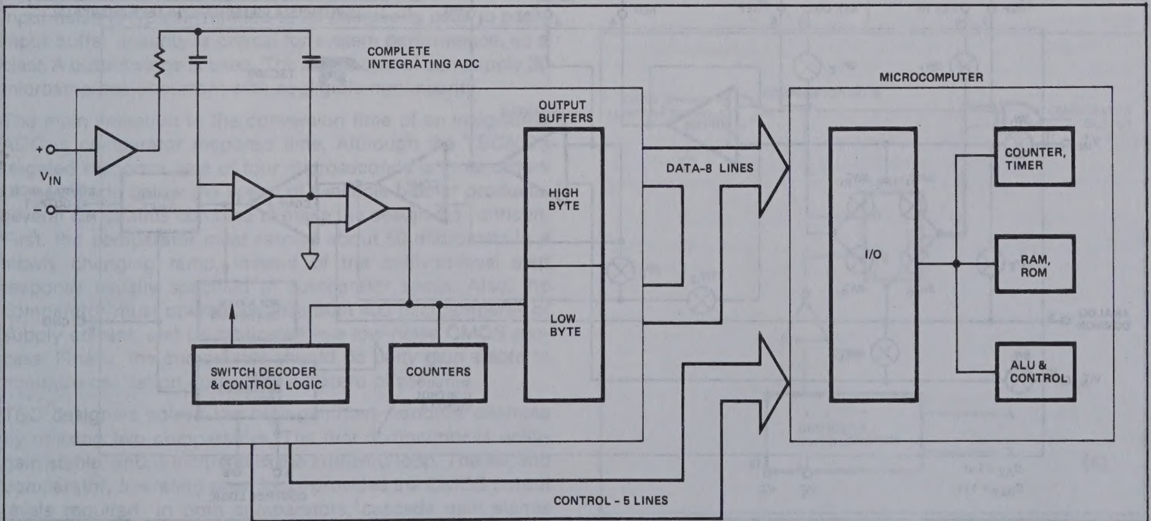

Figure 1: Typical ADC Interface to μC

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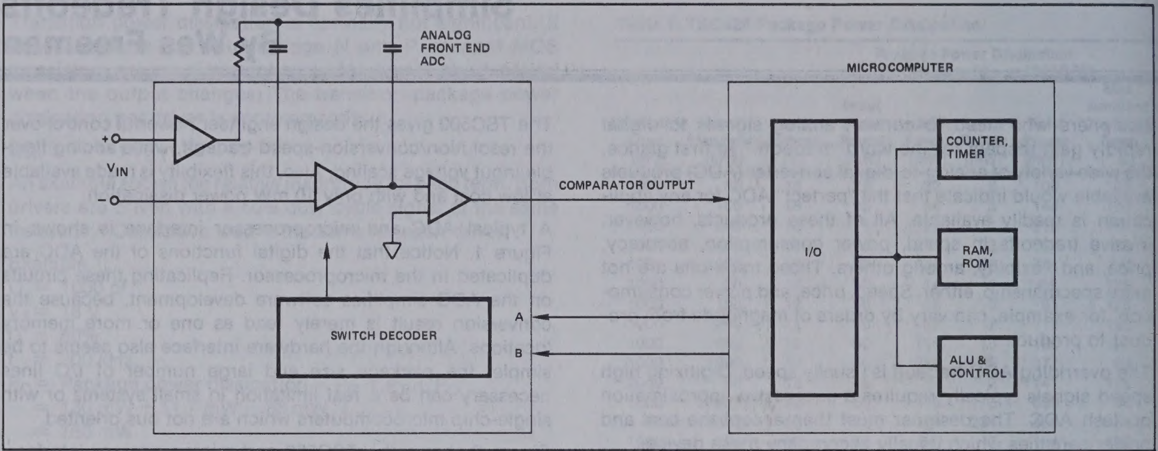
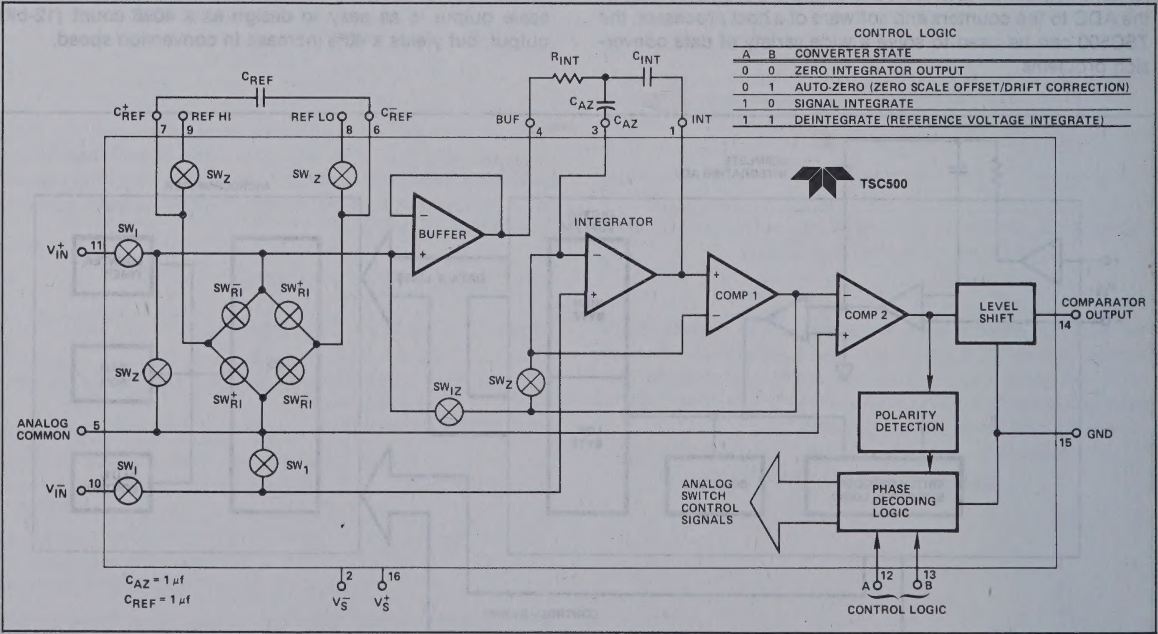

ANALOG
FRONT END
ADC
MICROCOMPUTER
+
V_IN
−
COMPARATOR OUTPUT
COUNTER,
TIMER
I/O
RAM,
ROM
A
B
SWITCH DECODER
ALU &
CONTROL

Figure 2: TSC500 Interface to μC

The ability to select full-scale is useful for measuring outputs which do not fall readily into a binary sequence. One such example is the 150 degree Centigrade operating range limit of IC temperature sensors such as the LM35 from National Semiconductor. By using a 1500 count ADC, the LM35's output can be read directly in tenths of a degree Centigrade. Adjusting the ADC's full-scale range to the sensor's output in engineering units can simplify software for data analysis and display.

The functional diagram of the TSC500 is shown in Figure 3. The design features include low leakage CMOS switches, high impedance input buffer, integrator op-amp, two-stage comparator, and digital control logic. These components, packaged in a 16-pin DIP, form the analog section of an ADC whose resolution can extend from less than 8 to greater than 14 bits.


C_REF
C+_REF
REF HI
REF LO
C−_REF
7
9
8
6
R_INT
C_INT
C_AZ
C_AZ
BUF
4
3
INT
1
TSC500
SW_Z
SW_Z
SW_I
V+_IN
11
SW−_RI
SW+_RI
SW_Z
SW+_RI
SW−_RI
BUFFER
INTEGRATOR
COMP 1
COMP 2
LEVEL
SHIFT
COMPARATOR
OUTPUT
14
SW_IZ
SW_Z
ANALOG
COMMON
5
SW_I
SW_I
V−_IN
10
POLARITY
DETECTION
GND
15
ANALOG
SWITCH
CONTROL
SIGNALS
PHASE
DECODING
LOGIC
C_AZ = 1 μf
C_REF = 1 μf
2
16
V−_S
V+_S
A
12
13
B
CONTROL LOGIC

CONTROL LOGIC

A	B	CONVERTER STATE
0	0	ZERO INTEGRATOR OUTPUT
0	1	AUTO-ZERO (ZERO SCALE OFFSET/DRIFT CORRECTION)
1	0	SIGNAL INTEGRATE
1	1	DEINTEGRATE (REFERENCE VOLTAGE INTEGRATE)

Figure 3: Functional Diagram of the TSC500

The CMOS switches permit very flexible input and reference voltage applications. During the signal integrate phase, the two SWI switches connect V_{IN}^+ to the input buffer and V_{IN}^- to the integrator. These connections provide a fully differential signal input, within the common-mode input range. The signal input common-mode range extends from (V_S^+ minus 1.5) to (V_S^- plus 1.5 V), providing an easy interface for bridge-type and other differential input applications.

A reference capacitor and switch matrix combine to also ease reference voltage limitations. During autozero the SWRC switches close, charging the reference capacitor to V_{REF}. Then, during deintegrate, the SWRI switches connect C_{REF} to the buffer input. Because C_{REF} isolates the reference inputs from the buffer, there are no common-mode limitations on the reference voltage. The REFHI and REFLO inputs can therefore be located anywhere within the power supply range.

The differential reference is especially useful for bridge applications, because the reference can be derived from the same voltage that drives the bridge. Changes in the bridge driving voltage will not, therefore, affect the ADC's output. Since there are no common-mode limits on the reference inputs, simple ratiometric resistance measurements are also possible.

The reference capacitor also combines with CMOS switches to produce a bipolar reference from the single-polarity reference inputs. Four SWDI switches in a bridge configuration connect C_{REF} to the buffer input. By the closure of opposing pairs of switches, C_{REF} can be connected as either a positive or a negative voltage. When the TSC500 deintegrate phase is selected, control logic samples the integrator polarity. Internal control logic then closes the appropriate pair of SWRI switches to select correct reference polarity.

The TSC500's excellent input characteristics are also a function of the low leakage, low noise metal gate CMOS process. Input bias current is only 10 picoamperes maximum, while input noise is typically limited to 30 microvolts peak to peak. Input buffer linearity is critical for system performance, so a class A output stage is used. The buffer output can supply 20 microamperes of current with negligible nonlinearity.

The main limitation in the conversion time of an integrating ADC is comparator response time. Although the TSC500's targeted response time of four microseconds is three orders of magnitude below the speed of available bipolar products, several constraints combine to make the design task difficult. First, the comparator must resolve about 50 microvolts in a slowly changing ramp, instead of the millivolt-level step response usually specified in comparator specs. Also, the comparator must operate on less than 400 microamperes of supply current, and be fabricated in a low-noise CMOS process. Finally, the comparator should be unity gain stable to minimize oscillation during the autozero phase.

TSC designers solved the high-gain/fast-response dilemma by utilizing two comparators. The first comparator is unity-gain stable, and is included in the autozero loop. The second comparator, operating open loop, provides the CMOS output levels required. In both comparators, cascade gain stages were used to minimize Miller capacitance and improve speed.

Input offset voltage (V_{OS}) of the buffer, integrator, and comparator #1 are unimportant because the errors are stored during the autozero phase. Comparator #2 is not in the autozero loop, however, so its V_{OS} must be minimized to reduce potential rollover and zero-offset problems. The input FETs of comparator #2 were therefore implemented as a cross-coupled quad, with close matching of devices and isothermal orientation. The combination of careful layout, low power dissipation on-chip, and the fact that comparator #2's V_{OS} is attenuated by the gain of comparator #1 ensure that rollover errors are held to less than .01% maximum for a 4 1/2 digit conversion.

The TSC500's only feedback path to its host microprocessor is via the comparator output. This output must, therefore, relay both polarity and zero crossing information. For large input signals the method is straightforward. The comparator status is read and stored prior to deintegrate, which establishes polarity. After the ADC is switched to deintegrate mode, the comparator output is monitored for the polarity reversal that signals zero crossing.

This method can fail for signals near zero, however, especially in the presence of normal mode noise. In this case, the comparator state can change several times during signal integrate. If a polarity reversal occurs between reading of polarity and start of deintegrate, the zero crossing will not be detected. This method also makes the polarity of the edge that signals zero crossing dependent on input polarity, which complicates the generation of interrupts.

A unique output circuit, shown in Figure 4a, solves both of these limitations. When the deintegrate phase is selected, comparator #2's polarity data is latched into an internal flip-flop. The inverting output of the flip-flop drives an exclusive-OR gate which ensures that, at the beginning of deintegrate, the comparator output will be driven to a logic high state.

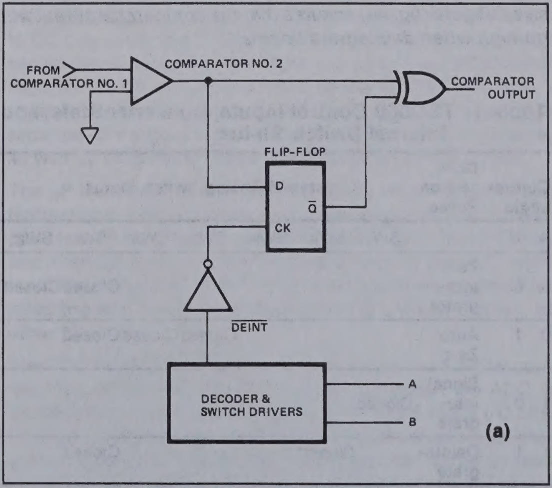


Figure 4a: Simplified Schematic of TSC500 Comparator

Figures 4b and 4c show the TSC500's comparator output for both positive and negative polarity inputs. Notice that polarity status is still valid before deintegrate begins. Even if polarity changes while the comparator output is being read, indicating an input very near zero, the comparator will still switch states when entering the deintegrate phase. In addition, zero crossing is always signalled by a negative-going transition of the comparator output. The negative-edge output is consistent with the interrupt structure of many common microprocessors.

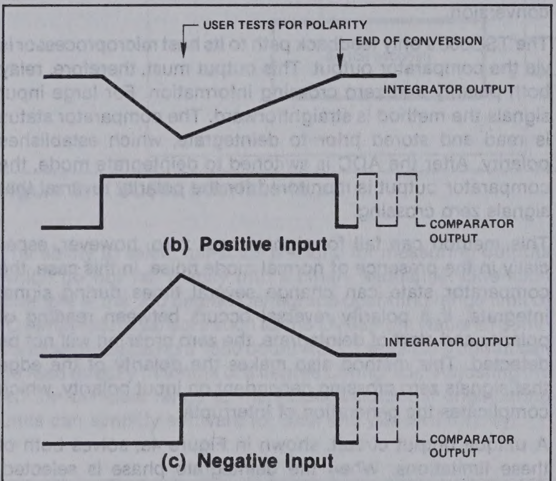


Figure 4b & c: Comparator Output Waveforms

This unusual comparator circuit conveys both polarity and end of conversion information. For a positive input the comparator will be in a high state during integrate (b) while for a negative input the output is low (c). In either case, the exclusive OR gate (fig. 4a) ensures that the comparator output will go high when deintegrate begins.

Table 1: TSC500 Control Inputs, Converter State, and Internal Switch Status.

Control Logic		Conversion Phase	Internal Analog Switch Status						
A	B		SW_I	SW_{RI}^+	SW_{RI}^-	SW_Z	SW_R	SW_I	SW_{IZ}
0	0	Zero Integrator						Closed	Closed
0	1	Auto-Zero				Closed	Closed	Closed	
1	0	Signal Integrate	Closed						
1	1	Deintegrate		Closed*				Closed	

*Assumes positive-polarity input signal. For negative input signal, SW_{RI}^- is closed.

The TSC500's two logic inputs control the phases of the integrating analog-to-digital conversion. (For further information on dual-slope A/D conversion, see appendix A of Teledyne Semiconductor Application Note AN-23). As shown in Table 1, the TSC500 adds an additional phase, zero-integrator, to the conventional autozero, signal integrate, and deintegrate phases. The zero-integrator mode can greatly reduce one of the integrating ADC's drawbacks, slow recovery from an input overrange condition. Slow overrange recovery is a problem when several inputs are multiplexed into one integrating ADC, because an overrange on one channel will affect the accuracy of other channels.

The source of the integrating ADC's slow input overrange recovery is shown in Figure 5. Under normal conditions, the integrator ramps up during signal integrate, then back to zero volts during deintegrate (Figure 5a). When the signal input exceeds full-scale, however, the integrator output does not reach zero volts before the end of deintegrate (Figure 5b). If the ensuing autozero period is not long enough to discharge the integrator to zero volts, succeeding conversions will provide erroneous data. The zero-integrator phase, on the other hand, provides a rapid discharge of the integrator error voltage (Figure 5c). This speedup occurs because, during zero-integrator, the integrator is actively driven toward zero volts.

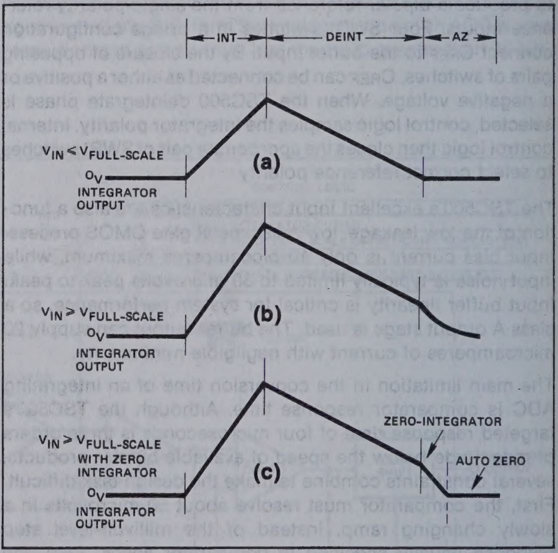


Figure 5: TSC500 Integrator Output Waveforms During:
(a) Normal Operation
(b) Input Overrange
(c) Input Overrange with Zero Integrator Cycle

The integrator output normally returns to 0 V at EOC (a), but an error voltage remains if the input is overranged (b). Adding a zero integrator cycle speeds overrange recovery (c).

Figure 6 demonstrates the difference between autozero and zero-integrator operation. During autozero, the buffer's input is connected to circuit common (Figure 6a). Disregarding offset voltage, the buffer's output will be zero volts. Any charge remaining on the integrator capacitor after deintegrate must discharge through R_{INT}, and the time constant is quite long. The zero-integrator phase speeds the error recovery by connecting the buffer input to comparator #1's output. Since the comparator output swing is greater than plus/minus four volts, discharge time is greatly reduced. Zero integrator must be followed by autozero, so that the buffer offset is cancelled. Typically, if 20% of the normal autozero period is devoted to zero-integrator following an overrange, then the integrator capacitor will be discharged.

Integrating ADCs are suitable for both system and display applications. The system ADC is typically part of a microprocessor based system, with the ADC accessed via a data bus or input/output (I/O) port. System ADCs typically produce binary data, and have three-state, bus compatible outputs. Display converters, on the other hand, are most often used as the heart of a dedicated instrument such as a digital multimeter. Display converters typically operate with decimal data and have binary-coded decimal (BCD) or seven segment outputs for easy interface to a visual display.

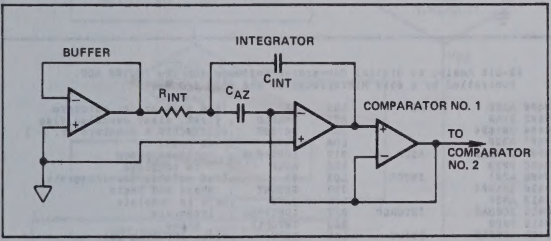


Figure 6a: TSC500 Simplified Schematic During Auto-Zero

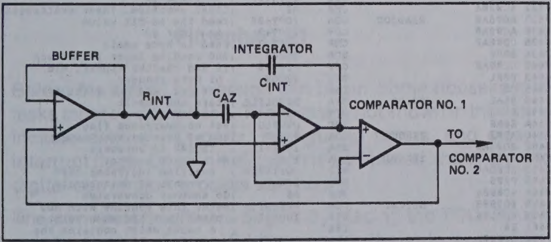


Figure 6b: TSC500 Simplified Schematic During Zero Integrate

Overrange recovery is slow in auto-zero because the buffer is connected to 0 V (a). The zero integrator phase connects the buffer to the comparator output to actively discharge the integrator (b).

The TSC500's flexibility permits it to be used in both system and display applications. Combined with a microprocessor I/O port, the TSC500 forms a binary ADC with resolution of 8 to 14 bits. Conversion rates of the binary ADC range from 400 down to 5 per second, while the high impedance signal inputs and differential reference ensure flexibility in measuring a variety of analog sensors.

When teamed with a single-chip microcomputer, on the other hand, the TSC500 can form an equally flexible display converter. Features which are difficult to implement with a dedicated display ADC become easy with the analog front end approach. Desireable features for a hand-held multimeter, for example, might include autoranging, bargraph display, relative measurements with decibel conversion, or programmable limits with buzzer alarm. Adding features in software can reduce development costs for a product family, as well as permitting product differentiation.

An example of the TSC500 used as a system ADC is shown in Figure 7. Only three active and ten passive components are required, in addition to the μP I/O port, to form a very flexible ADC. Since the TSC500 is available in a 16-pin DIP, PCB area is actually less than that required for a dedicated but less flexible ADC.

All of the analog components, except the reference, are contained in the TSC500. The passive components are inexpensive, and critical tolerances are not required. The integrating capacitor, C_{INT}, must have very low dielectric absorption, so polypropylene is recommended. The other capacitors can be polypropylene, MYLAR, or other low leakage film type.

The ADC's reference voltage is provided by two TSC9491s, which operate like a 2.44 volt Zener diode. Requiring a minimum bias current of only 50 μA, the TSC9491 is available in temperature coefficient grades of 50 or 100 ppm/°C. If the ADC's reference voltage is less than 1.22 V, only one TSC9491 is required.

Although the TSC500 requires +/-5 V power supplies, the circuit operates with a single +5 V connection. A monolithic DC to DC converter, the TSC7660, combines with two electrolytic capacitors to convert a +5 V input into -5 V. The TSC500 only requires 1.5 mA of supply current, so the TSC7660 provides a voltage conversion efficiency of about 98%. Eliminating a separate -5 V supply reduces power supply bulk and expense, as well as simplifying power distribution and PCB layout.

The μP I/O device is a Synertek SY6522, which contains two bidirectional 8-bit I/O ports, four interrupt control/handshake pins, two 16-bit timers and a shift register. Only four I/O bits, one interrupt input, and the timers are used for the ADC interface. The remainder of the I/O port functions are available for selecting multiplexed inputs, accessing a visual display, or other functions.

The TSC500/SY6522 interface only requires three digital connections, which is a significant advantage when the ADC is located some distance from the I/O port. Two SY6522 I/O bits, configured as outputs, control the TSC500's dual slope integration algorithm. The comparator output can either be read by polling an input port or by generating an interrupt. In most cases the interrupt would be used, of course, but input polling is useful while debugging software.

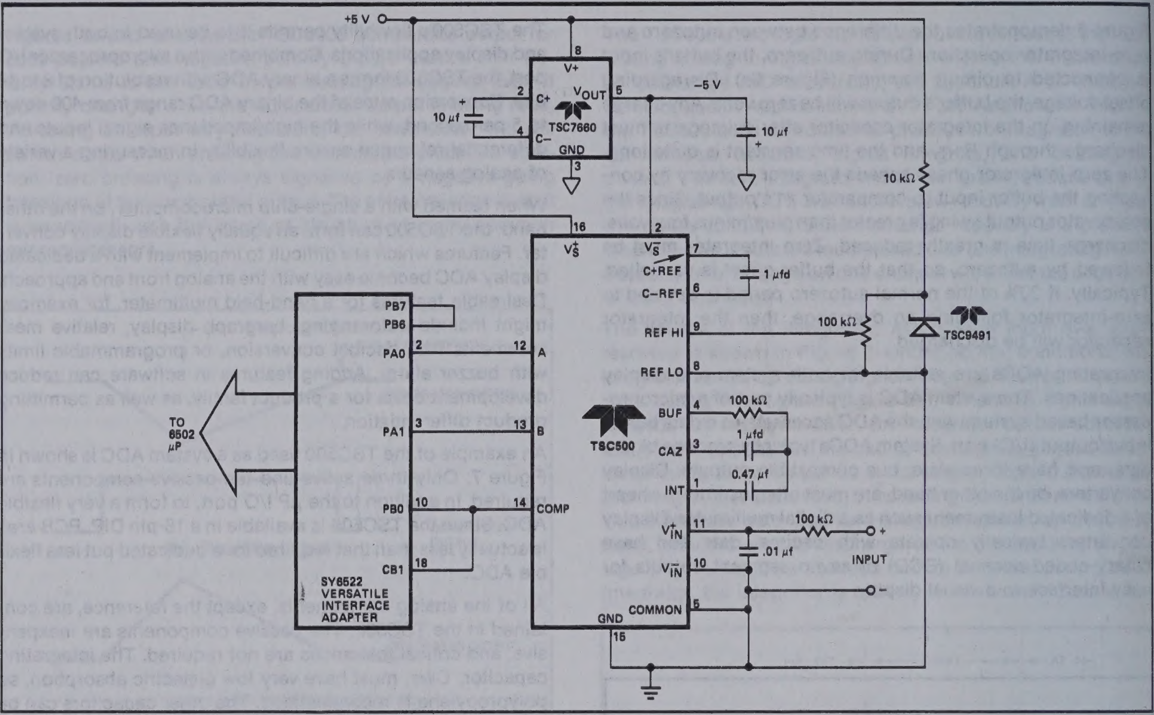


Figure 7: TSC500 Interface to a Typical µP I/O Port

The circuit makes use of both of the SY6522's counter/timers. Timer #1 is used to generate the ADC clock pulses, while timer #2 functions as the ADC's counter. The frequency output of timer #1 therefore controls the ADC conversion speed, while the binary number loaded into the counter determines the ADC resolution. During deintegrate, the count in timer #2 when the comparator output switches to a logic low state is proportional to the analog input voltage.

Timer #1 operates in its "free running" mode to generate the ADC clock. In this mode, the µP's clock is divided by a 16-bit integer stored in the T1 latches. The result is a square wave output on pin PB7. The clock frequency can be modified, by changing the divider constant, to adjust conversion speed or to reject specific normal mode noise frequencies.

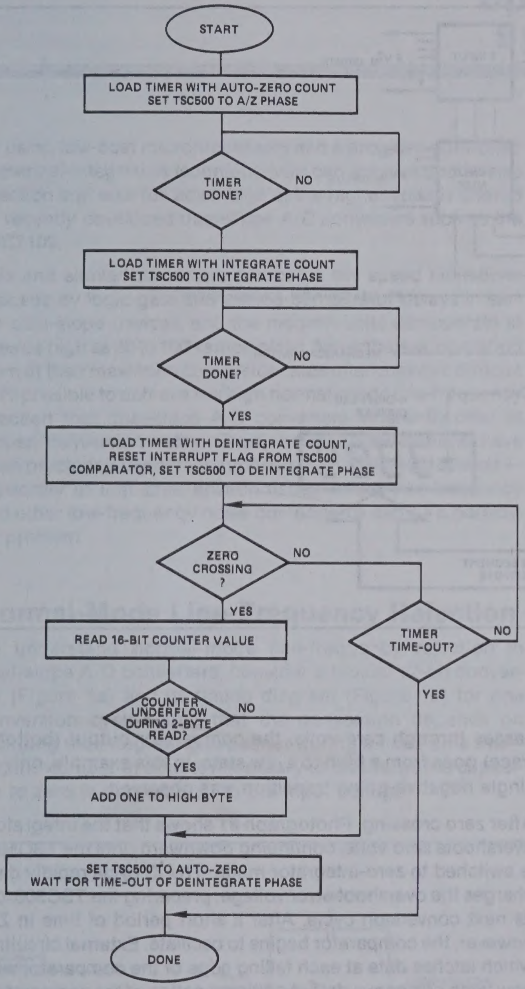
Counter/timer #2 is programmed for its pulse counting mode. When a number is loaded into the T2 latches, the counter will decrement with each negative pulse on input PB6. Connecting PB7 to PB6 permits the counter to operate at the frequency programmed into Timer #1. An interrupt flag is set when the counter underflows, signalling the end of each measurement cycle.

As mentioned previously, the TSC500 hardware combines with µP software to form an ADC. Software for the circuit, written in 6502 assembly language, is shown in Listing 1. The logic flow is shown in Flowchart 1. This program will produce a 12-bit conversion, but the resolution can easily be increased or decreased.

```
;    12-bit Analog to Digital Conversion Software for the TSC500 ADC,
;     controlled by a 6502 Microprocessor and 6522 I/O Port
;
0400 A200         AZ        LDX     #0         ;load pointer for autozero
0402 86A0                   STX     OVRFLG     ; first, clear overflow flag
0404 205B04                 JSR     SETCNT     ;set TSC500 & counters for A-Z
0407 A920                   LDA     #20H       ;loop until
0409 2C0DA0       AZLP      BIT     IOPT+0DH   ;  autozero phase
040C F0FB                   BEQ     AZLP       ;    is complete
040E A201         INTGR     LDX     #1         ;load pointer for integrate
0410 205B04                 JSR     SETCNT     ;  phase and begin
0413 A920                   LDA     #20H       ;wait to complete
0415 2C0DA0       INTGRLP   BIT     IOPT+0DH   ;  integrate
0418 F0FB                   BEQ     INTGRLP    ;    phase
041A AD00A0       DEINT     LDA     IOPT       ;clear INT from CB1
041D 85A1                   STA     SIGN       ; and save sign bit
041F A202                   LDX     #2         ;set up
0421 205B04                 JSR     SETCNT     ;  deintegrate phase
0424 A901         DEINTLP   LDA     #01        ;has comparator changed
0426 2C00A0                 BIT     IOPT       ;  state, indicating EOC?
0429 F00A                   BEQ     READEOC    ;yes, get results
042B A920                   LDA     #20H       ;no, so test
042D 2C0DA0                 BIT     IOPT+0DH   ;  for timeout of
0430 F0F2                   BEQ     DEINTLP    ;    timer #2
0432 4C0004                 JMP     AZ         ;timer overflow, input overranged
0435 AD08A0       READEOC   LDA     IOPT+08    ;read the 16-bit value
0438 AC09A0                 LDY     IOPT+9     ; in timer #2
043B CD08A0                 CMP     IOPT+8     ;read lo byte again
043E B006                   BCS     EOCOK      ;2nd reading lower is correct
0440 CC09A0                 CPY     IOPT+9     ;if 2nd reading higher, did
0443 F001                   BEQ     EOCOK      ; hi byte change?
0445 C8                     INY                ;  if yes, add one to hi byte
0446 85A2         EOCOK     STA     RESULTLO   ;store ADC result
0448 84A3                   STY     RESULTHI   ;  in RAM
044A E6A0                   INC     OVRFLG     ;set no-overrange flag
044C A902         ZEROCR    LDA     #AZIO      ;end of deintegrate, so set
044E 8D01A0                 STA     IOPT+1     ;  TSC500 to autozero
0451 A920         ZERLP1    LDA     #20H       ;wait until counter
0453 2C0DA0                 BIT     IOPT+0DH   ;  overflow indicates 2000
0456 F0F9                   BEQ     ZERLP1     ;    counts of deintegrate
0458 4C0004                 JMP     AZ         ;do another conversion
045B BD0008       SETCNT    LDA     PHZCNT,X   ;enter this routine with ADC
045E 8D01A0                 STA     IOPT+1     ; phase in X reg as a pointer to
0461 E8                     INX                ;  a table which contains the
0462 BD0008                 LDA     PHZCNT,X   ;  TSC500 control bits and timer
0465 8D08A0                 STA     IOPT+8     ;   constant for each phase
0468 E8                     INX                ;set TSC500 to desired phase,
0469 BD0008                 LDA     PHZCNT,X   ; load 6522 down-counter,
046C 8D09A0                 STA     IOPT+9     ;  and return
046F 60                     RTS
0800                        ORG     800H          ;Table for TSC500 control
0800 02000801     PHZCNT    DB      2,00,08,1     ;bits and counter values
0804 0000030010             DB      00,08,3,00,10H
```

Listing 1: Software for 12-bit ADC with TSC500 and 6502 µP

Combine this software with the hardware of Figure 7 to form a 12-bit ADC. The converter's resolution can be adjusted by changing the counter values stored in the "PHZCNT" table.


START
LOAD TIMER WITH AUTO-ZERO COUNT
SET TSC500 TO A/Z PHASE
TIMER DONE?
NO
LOAD TIMER WITH INTEGRATE COUNT
SET TSC500 TO INTEGRATE PHASE
TIMER DONE?
NO
YES
LOAD TIMER WITH DEINTEGRATE COUNT,
RESET INTERRUPT FLAG FROM TSC500
COMPARATOR, SET TSC500 TO DEINTEGRATE PHASE
ZERO CROSSING ?
NO
YES
READ 16-BIT COUNTER VALUE
TIMER TIME-OUT?
NO
YES
COUNTER UNDERFLOW DURING 2-BYTE READ?
NO
YES
ADD ONE TO HIGH BYTE
SET TSC500 TO AUTO-ZERO
WAIT FOR TIME-OUT OF DEINTEGRATE PHASE
DONE

Flowchart #1

Before the actual conversion can begin, some housekeeping tasks must be completed. These tasks, not shown in the listing, include setting I/O ports, configuring timers, and clearing interrupt flags. Once initialization is completed, the analog-to-digital conversion process can begin.

The conversion software begins by placing the TSC500 in its autozero mode. For a 12-bit converter the autozero cycle is 2048 counts, so the counter registers are loaded with this value. The counter immediately begins decrementing at the square wave frequency and the μP waits for the counter underflow that signals the end of autozero.

The signal integrate phase is identical to autozero, except for placing the TSC500 in signal integrate mode. The integrate cycle is also 2048 counts, and the integrate period is selected to provide optimal normal mode noise rejection. After the signal integrate cycle is complete, deintegration begins and the analog input value is determined.

The deintegrate cycle begins by reading the comparator output. This action serves a dual purpose. First, the comparator state at the end of signal integrate establishes input polarity. Second, reading the input port resets the corresponding interrupt bit. The next negative edge on the comparator output will set the interrupt flag and signal the zero crossing.

Deintegrate continues by placing the TSC500 in its deintegrate mode and again loading the down counter. For a 12-bit conversion the counter value is 4096. The software then begins testing for zero crossing and end of conversion.

In the deintegrate loop, a test is first made for zero crossing. If the interrupt bit which corresponds to the comparator is not set, then the program tests for counter underflow. The program continues to loop until either zero crossing or counter underflow occurs.

When zero crossing occurs, the contents of the down counter represent the analog conversion result. The counter value is therefore transferred to memory for further processing. A memory location is also incremented to indicate that zero crossing has occurred. This memory location can be tested during autozero if the user wishes to include an optional zero-integrator phase.

Rather than stopping and restarting the counter, the registers are read "on the fly." Several steps are required to ensure that data does not change between reading the high and low bytes. If the high order byte changes between readings, the result would be 256 counts of error. The program therefore reads the counter registers twice, and tests for a borrow occurring between the two read operations. If the high byte has changed, a correction is applied before data is stored in memory.

Once the conversion result is stored, the program again waits for the deintegrate phase to end. When the counter underflows, the conversion cycle is complete. The program loops back to autozero if another conversion is desired, or jumps to software which processes the ADC data. Since timer #2 is a down counter, the stored data must be subtracted from 4096 to get the actual analog input.

The software shown in Listing 1 keeps the μP in a continuous loop during conversion. In normal practice the conversion would be interrupt driven, so that the μP would be free for other tasks. To convert the software to interrupt operation, routines must be added which will recognize interrupt sources and also keep track of the conversion phases.

The TSC500 interface only requires a small portion of the I/O port's available functions, so additional features are easy to add. Figure 8 shows one possible expansion by adding input multiplexers for eight differential analog signals. A four digit LED display is also included. The TSC701AM accepts BCD data, decodes the data to seven segment display format, and provides 28 LED segment driver outputs with 18 mA current capability. Placing CA2 in its pulse output mode will latch data into the TSC701AM simply by writing to port A. Four bits of I/O are still available for controlling motors, heaters, valves, etc., or for monitoring digital inputs.

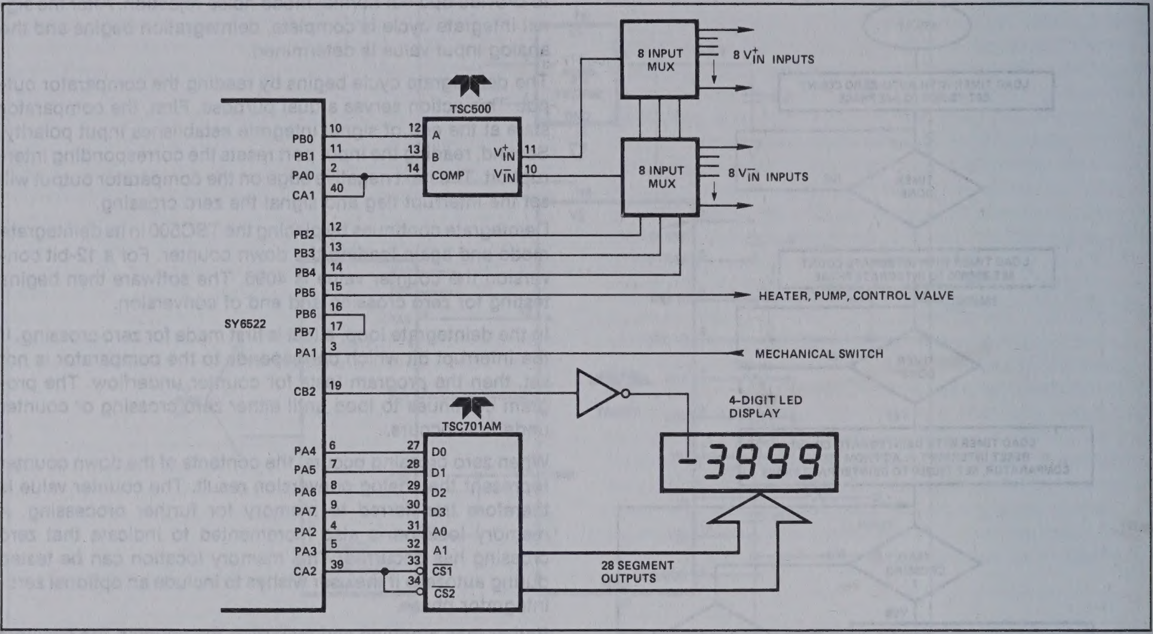

8 INPUT MUX
8 V$^+_{IN}$ INPUTS
TSC500
PB0
PB1
PA0
CA1
10
11
2
40
12
13
14
A
B
COMP
V$^+_{IN}$
V$^-_{IN}$
11
10
8 INPUT MUX
8 V$^-_{IN}$ INPUTS
PB2
PB3
PB4
PB5
PB6
PB7
PA1
CB2
12
13
14
15
16
17
3
19
SY6522
HEATER, PUMP, CONTROL VALVE
MECHANICAL SWITCH
4-DIGIT LED DISPLAY
-3999
TSC701AM
PA4
PA5
PA6
PA7
PA2
PA3
CA2
6
7
8
9
4
5
39
27
28
29
30
31
32
33
34
D0
D1
D2
D3
A0
A1
CS1
CS2
28 SEGMENT OUTPUTS

Figure 8: 8-Channel Data Acquisition System

TSC500 Comparator Behavior After Zero Crossing

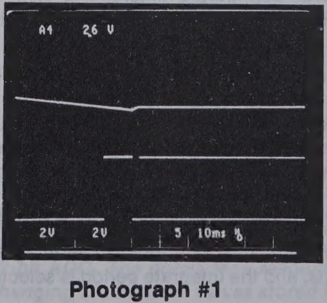
The TSC500 comparator is designed to produce a negative-going edge-triggered output which signals the end of conversion. This transition occurs during the deintegrate phase, when the integrator output passes through zero volts. In most cases, the result will be a single negative-going transition. Occasionally, however, and especially in a noisy electrical environment, the comparator may make more than one transition.

Multiple comparator pulses are seldom a problem in a microprocessor sytem, since most μPs will not respond to a second interrupt until the first one is serviced. The service routine then disables the interrupt until the next deintegrate cycle, so additional comparator transitions are ignored.

Problems do occur, however, in circuits built with discrete logic. If the unbuffered negative comparator edge is used to transfer data to latches, for example, multiple transitions will produce erroneous data. More importantly, additional transitions during auto-zero and integrate cycles will make the latched data meaningless. Therefore, designers of non-μP TSC500 systems should provide logic which will ensure that end of conversion is only determined by the first negative comparator transition which occurs after the TSC500 is placed in deintegrate mode.

Photograph #1 demonstrates the TSC500 comparator output at the end of a conversion. As the integrator output (top trace) passes through zero volts, the comparator output (bottom trace) goes from a high to a low state. In this example, only a single negative-going transition was observed.

After zero crossing, Photograph #1 shows that the integrator overshoots zero volts, continuing downward until the TSC500 is switched to zero-integrator mode. The ZI cycle rapidly discharges the overshoot error voltage, preparing the TSC500 for its next conversion cycle. After a short period of time in ZI, however, the comparator begins to oscillate. External circuitry which latches data at each falling edge of the comparator will now latch erroneous data. Additional gating of the comparator output, as outlined above, will prevent this error. (Note that the oscillations observed are comparator #2. This does not imply that the ZI loop, which uses feedback from the output of comparator #1, is unstable).



TOP-TSC500 INTEGRATOR OUTPUT

BOTTOM-TSC500 COMPARATOR OUTPUT

Photograph #1

TELEDYNE SEMICONDUCTOR

Application Note 27
Numerical-Integration Techniques Speed Dual-Slope A/D Conversion
By Gary Grandbois and Wes Freeman

By using low-cost microprocessors and a program-controlled numerical-integration technique, you can achieve good noise rejection and take full advantage of the higher speeds offered by recently developed dual-slope A/D converters such as the TSC7109.

This and similar converters overcome the speed limitations imposed by logic-gate and analog-comparator delays in earlier dual-slope devices, and the modern units can operate at rates as high as 30 to 100 samples/sec. Nevertheless, operating them at their maximum conversion rates often makes it difficult or impossible to achieve the high normal-mode line-frequency rejection that dual-slope A/D converters inherently offer at slower conversion rates. Thus, noise considerations have often precluded use of these converters at their rated speeds — especially in industrial environments, where line-frequency and other low-frequency noise components can be a particular problem.

Normal-Mode Line-Frequency Rejection

To understand normal-mode line-frequency rejection in dual-slope A/D converters, consider a typical 12-bit converter (Figure 1a) and its timing diagram (Figure 1b) for one conversion cycle. Note that the conversion depends on charging the integrating capacitor during a fixed time interval; the number of counts necessary to discharge the capacitor to zero is proportional to the input voltage.

The integrating A/D converter integrates the signal only in a certain time window, as Figure 1b shows. This limited integration period results in normal-mode noise rejection only when the integration period is equal to one or more periods of the noise signal (Figure 2a). The time integral of this noise over integer multiples of the noise period is, of course, zero.

Normal-mode noise-rejection performance can thus be represented as a function (Figure 2b) that reaches peaks at the fundamental and harmonic frequencies of the period defined by the signal-integrate time T. The minimum period T, which must equal the noise period, has been the limiting factor for conversion speed. At 60 Hz, for example, the minimum signal-integrate time is 16.7 msec; at 50 Hz, it's 20 msec.

Because the signal-integrate time is only a portion of the total conversion time, conversion rates are significantly less than 1/T. A standard, high-performance, dual-slope A/D converter includes a reference deintegrate phase, typically 2T long, and an autozero period equal to the signal-integrate period T. The total conversion time is thus 4T, which, for 60-Hz rejection, yields a maximum conversion rate of 15 samples/sec; for 50 Hz, it yields 12.5 samples/sec.

The most serious constraint arises when you want to offer an instrument for international use that can reject both 60 *and* 50 Hz. This feature is attainable only when the signal-integrate period T can contain six cycles of 60-Hz noise and five cycles of 50-Hz noise. The resulting 100-msec signal-integrate period dictates a 2.5-conversion/sec rate.

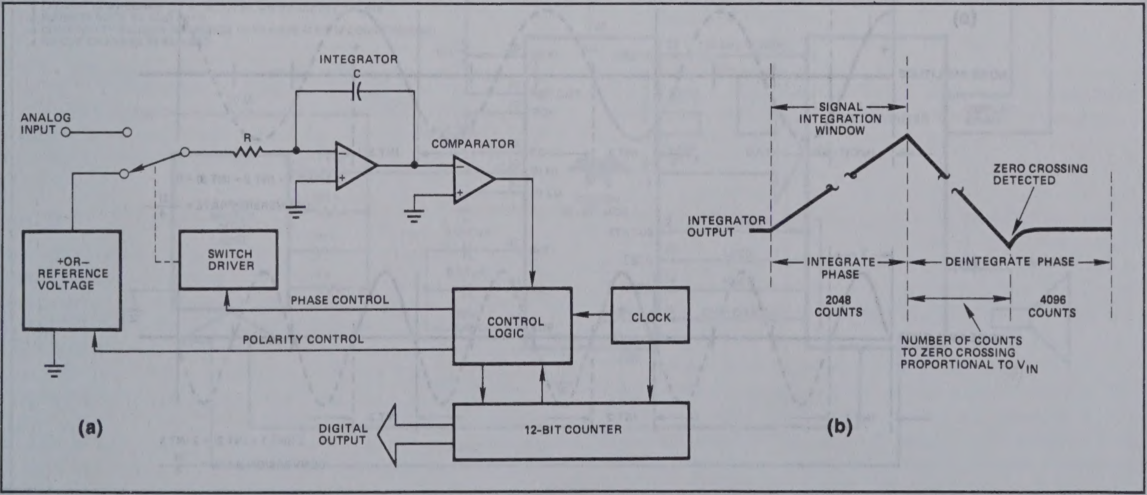


Figure 1: A dual-slope A/D converter *operates by charging a capacitor from the input voltage during a fixed time, then discharging it to zero. The number of clock periods in the discharge time corresponds to the analog input voltage. The size of the integrating time window determines which normal-mode noise signals are rejected.*

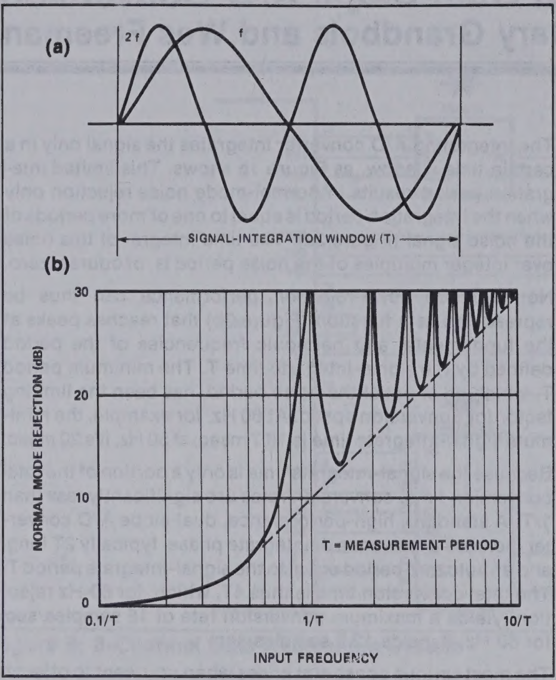


Figure 2: In a dual-slope A/D converter, *high normal-mode noise rejection occurs when the integration period is a multiple of the noise signal's period.*

You can, however, overcome the inherent conversion-speed limitation of integrating A/D converters. A microprocessor with program-controlled numerical integration that complements the A/D converter's analog integration will speed dual-slope conversion considerably.

You can achieve high normal-mode rejection for specific frequencies with this method if three conditions are met. First, the signal-integrate period must be defined such that noise integration takes place on a segmented basis. In Figure 3a, for example, the integrate window opens on a noise-waveform segment that's one-third of a period long.

Next, the second signal-integrate period must begin at a point corresponding exactly to the point at which the first one ended, and the third's beginning must correspond to the point at which the second ended. This condition can be met only if the A/D converter has a fixed conversion time, irrespective of the signal input. Finally, the microprocessor must sum all three conversions to achieve the total integration of a cycle of noise. A consideration of all these constraints for the TSC7109 A/D converter, for example, leads to the relationship

$$f_{NOISE} = \frac{1}{XT} = \frac{4C}{X}$$

where C is the conversion rate, f the noise frequency and X the number of conversion results added. X must be an odd number; Figure 3b shows why X cannot be an even number. A frequency that would require an even number of samples is one at which the integrate window is locked in phase with the signal (ie, the converter and signal periods are synchronized). For $C_V = (f_{NOISE})(X/4)$ and $X = 2$ (as in Figure 3b), the result is two times the error of one conversion.

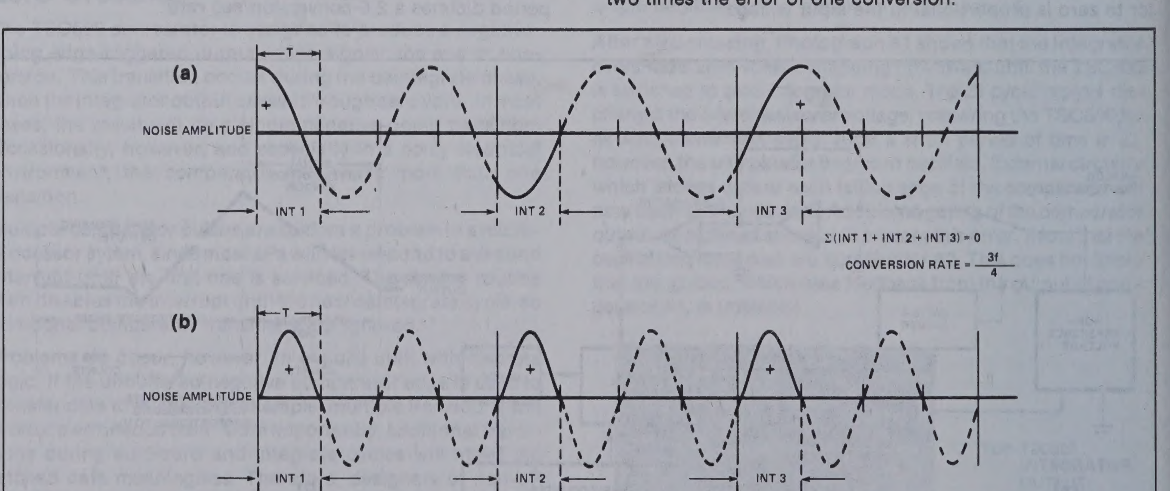


Figure 3: Data-conversion systems employing a numerical-integration technique *furnish noise rejection when an odd number of samples are summed* **(a)***. Adding the results of two conversions, though, can yield twice as much error as does one conversion* **(b)** *if the A/D converter and noise frequency are synchronized.*

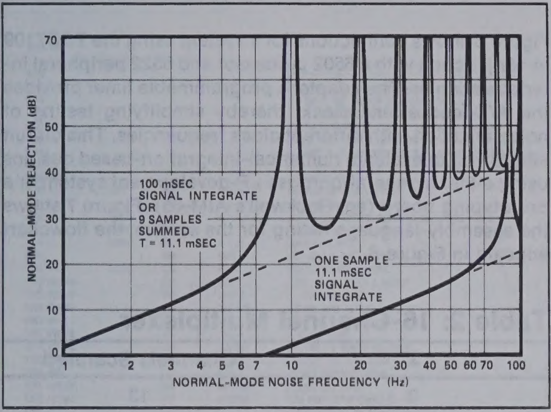


Figure 4: The normal-mode-rejection capability *illustrated by the upper curve here demonstrates the effectiveness of taking nine conversion samples; the system that the curve represents rejects noise at all multiples of 10 Hz. The lower curve shows the result of acquiring only one sample and employing an 11.11-msec signal-integration period.*

To achieve the desired normal-mode rejection, you must, therefore, sum an odd number of A/D-converter results. You can accomplish this summation with firmware or with user-interactive software. Consider an example using a TSC7109 A/D converter operating at 22.5 samples/sec. The equation yields the results in Table 1.

As Table 1 indicates, an A/D converter operating at 22.5 samples/sec can reject harmonics of 10 Hz if you maintain a rolling average of nine samples. This technique rejects 50 *and* 60 Hz; it's equivalent to one sample taken at the rate of 2.5 samples/sec. The curves in Figure 4 show the normal-mode rejection resulting from 1- and 9-sample averages at the rate of 22.5 conversions/sec (or one sample at 2.5 conversions/sec).

Table 1: TSC7109 at 22.5 Samples/Sec

f_{NOISE} (Fundamental) In Hz	X Samples Summed
90	1
30	3
18	5
12.8	7
10	9

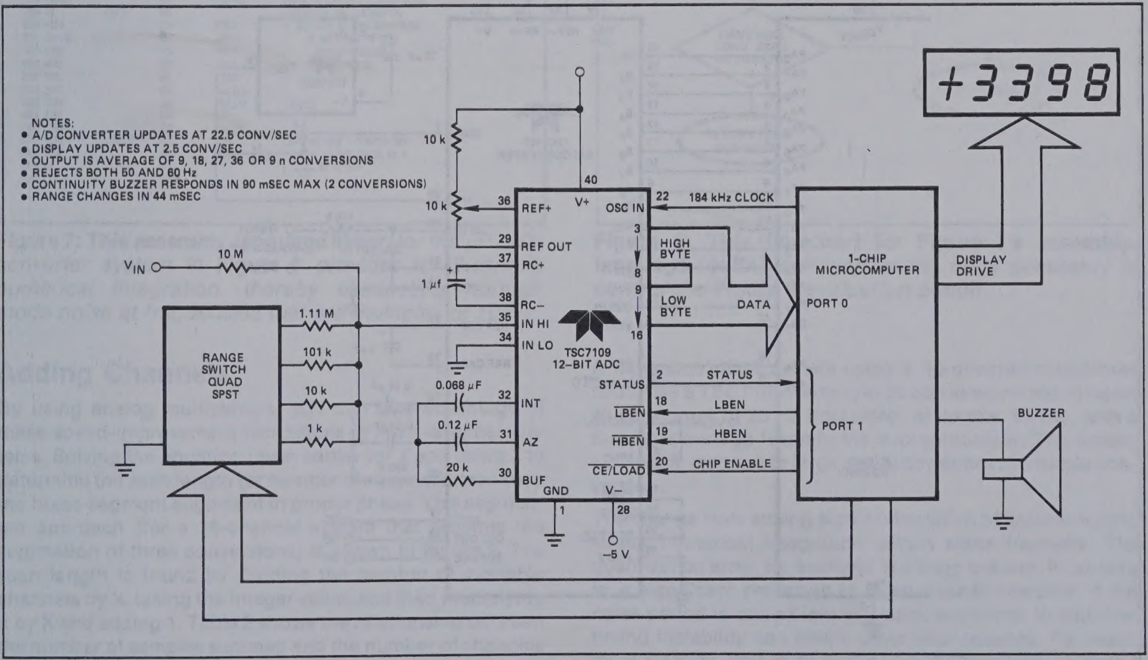

NOTES:
• A/D CONVERTER UPDATES AT 22.5 CONV/SEC
• DISPLAY UPDATES AT 2.5 CONV/SEC
• OUTPUT IS AVERAGE OF 9, 18, 27, 36 OR 9 n CONVERSIONS
• REJECTS BOTH 50 AND 60 Hz
• CONTINUITY BUZZER RESPONDS IN 90 mSEC MAX (2 CONVERSIONS)
• RANGE CHANGES IN 44 mSEC
+3398
10 k
10 k
40
V+
36
REF+
29
REF OUT
37
RC+
1 µf
38
RC–
35
IN HI
34
IN LO
TSC7109
12-BIT ADC
0.068 µF
32
INT
0.12 µF
31
AZ
20 k
30
BUF
GND
1
V–
28
–5 V
V_{IN}
10 M
RANGE
SWITCH
QUAD
SPST
1.11 M
101 k
10 k
1 k
OSC IN
22
184 kHz CLOCK
3
HIGH
BYTE
8
9
LOW
BYTE
16
DATA
1-CHIP
MICROCOMPUTER
PORT 0
DISPLAY
DRIVE
STATUS
2
STATUS
LBEN
18
LBEN
HBEN
19
HBEN
CE/LOAD
20
CHIP ENABLE
PORT 1
BUZZER

Figure 5: This 3 3/4-digit multimeter *uses a numerical-integration technique to reject both 50-and 60-Hz normal-mode noise. Although the DMM's display updates at 2.5 samples/sec, conversions take place at 22.5 samples/sec.*

What's the point, you may ask, of sampling at the higher rate if you must wait for the result during a 9-period numerical integration? After the first 9-period wait, the system's pipeline is full, and you can then obtain a new result for *each cycle* at the 22.5-samples/sec rate.

The numerical-integration technique has many practical applications. The Figure 5 circuit, for example, is a 3 3/4 digit DMM that uses a TSC7109 13-bit A/D converter. The DMM updates the display at a 2.5 sample/sec rate for easy readability, yet it converts at a 22.5 sample/sec rate for fast response during autoranging and continuity checking. Because the circuit averages nine samples, it rejects both 50- and 60-Hz noise. Because it can carry a rolling average, the μP is capable of changing the number of conversions summed; it can therefore accommodate specific, user-programmable rejection frequencies.

Figure 6 shows connections for a system using the TSC7109 in conjunction with a 6502 processor and 6522 peripheral interface adapter. The adapter's programmable timer provides the A/D converter's clock, thereby simplifying testing of noise rejection with different clock frequencies. This circuit allows you to evaluate numerical-integration-based designs using either a general-purpose μP-development system or a prototyping board (eg, Rockwell's AIM-65). Figure 7 shows the assembly-language listing for the system; the flowchart appears in Figure 8.

Table 2: 16-Channel Multiplexer

X	Channels Scanned
3	13
5	16
7	15
9	10

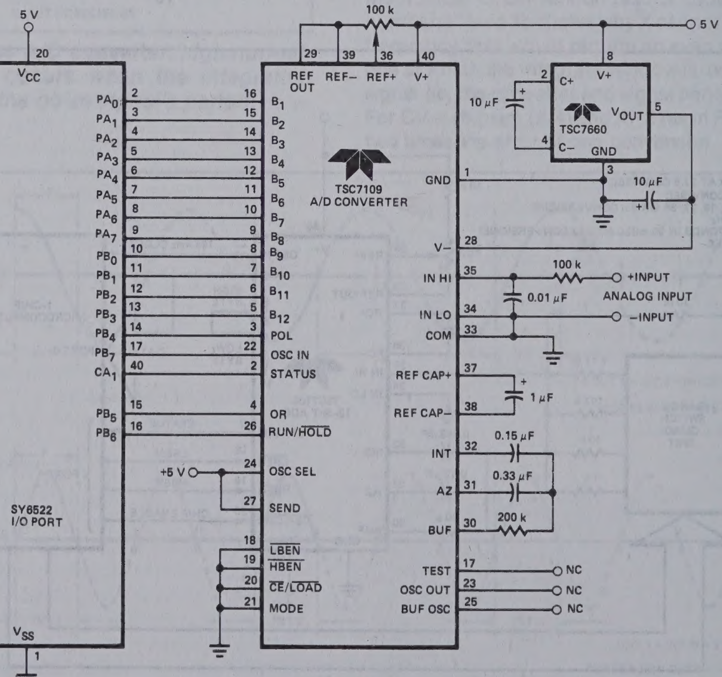

5 V
20
V_{CC}
PA_0
PA_1
PA_2
PA_3
PA_4
PA_5
PA_6
PA_7
PB_0
PB_1
PB_2
PB_3
PB_4
PB_7
CA_1
PB_5
PB_6
SY6522
I/O PORT
V_{SS}
1
+5 V
100 k
5 V
29
39
36
40
REF OUT
REF−
REF+
V+
B_1
B_2
B_3
B_4
B_5
B_6
B_7
B_8
B_9
B_{10}
B_{11}
B_{12}
POL
OSC IN
STATUS
OR
RUN/$\overline{HOLD}$
OSC SEL
SEND
$\overline{LBEN}$
$\overline{HBEN}$
$\overline{CE/LOAD}$
MODE
TSC7109
A/D CONVERTER
GND
V−
IN HI
IN LO
COM
REF CAP+
REF CAP−
INT
AZ
BUF
TEST
OSC OUT
BUF OSC
10 µF
C+
V+
TSC7660
V_{OUT}
C−
GND
10 µF
100 k
0.01 µF
+INPUT
ANALOG INPUT
−INPUT
1 µF
0.15 µF
0.33 µF
200 k
NC
NC
NC

Figure 6: You can evaluate numberical integration with the circuit *detailed in this schematic. The 6522 peripheral-interface adapter provides clocking and the µP interface for the dual-slope A/D converter.*

```
094D.ASM

000D                                  ;----------------------------------------------------
000D                                  ; SOFTWARE TO DEMONSTRATE NUMERICAL INTEGRATION
000D                                  ;   USING THE TSC7109 INTERFACED TO A 6502
000D                                  ;     MICROPROCESSOR VIA A 6522 I/O PORT
000D                                  ; RESULTS STORED AT 'RESLT' IN ZERO-PAGE MEMORY
000D                                  ; USER MUST PROVIDE INTERRUPT VECTOR FROM THE
000D                                  ;   6522'S CA1 INTERRUPT TO SVC ROUTINE AT "INTSVC"
000D                                  ;----------------------------------------------------
000D                                  ;SYSTEM EQUATES
A800          IOPT     EQU     0A800H ;ADDRESS OF 6522 I/O PORT
0080                   ORG     80H    ;RESERVE ZERO-PAGE MEMORY
0080          RESLT    DS      3      ;16-BIT ACCUMULATOR FOR RESULTS, 1 BYTE FOR SIGN
0083          STORX    DS      1      ;STORAGE FOR LOOP COUNTER
0084          STORHI   DS      1      ;SAVE HIGH BYTE
0280                   ORG     0280H  ;SET UP I/O PORT TO CONTROL TSC7109
0280 A9C0     CLOCK    LDA     #0C0H  ;PB6 & PB7 ARE OUTPUTS,
0282 8D00A8            STA     IOPT   ; PB7 IS THE TIMER 1 OUTPUT
0285 8D02A8            STA     IOPT+2 ;  (FOR 7109 CLOCK)
0288 8D0BA8            STA     IOPT+0BH ;SQUARE WAVE OUTPUT ON PB-7
028B A912              LDA     #12H   ;LOAD THE CONSTANT FOR
028D 8D04A8            STA     IOPT+4 ;  CLOCK TIMER
0290 20FA02            JSR     SETREG ;INITIALIZE MEMORY REGISTERS
0293 8D05A8            STA     IOPT+5 ;  START THE 7109 CLOCK
0296 A982              LDA     #82H   ;ENABLE INTERRUPT FROM
0298 8D0EA8            STA     IOPT+0EH ;  6522 CA1 INPUT
029B 4C2303            JMP     MAINPRG ;I/O PORT SETUP COMPLETE, SO
029E                                  ; JUMP TO O.S. OR TO MAIN PROGRAM
029E                                  ;INTERRUPT SERVICE ROUTINE
02B0                   ORG     02B0H
02B0 AD00A8   INTSVC   LDA     IOPT   ;GET HIGH BYTE
02B3 AA                TAX            ;SAVE IT
02B4 290F              AND     #0FH   ;ZERO MSBs FOR ARITHMETIC
02B6 8584              STA     STORHI ;SAVE IT
02B8 8A                TXA            ;GET SIGN BIT BACK
02B9 2910              AND     #10H   ;ANALOG INPUT NEGATIVE?
02BB F017              BEQ     SUBTR  ; YES, SO SUBTRACT
02BD 18                CLC            ;RESULT POSITIVE SO ADD
02BE A580              LDA     RESLT  ;GET LS BYTE OF THIS CONVERSION
02C0 6D01A8            ADC     IOPT+1 ; ADD TO PREVIOUS READINGS
02C3 8580              STA     RESLT  ;  SAVE LS BYTE
02C5 A581              LDA     RESLT+1 ;GET MS BYTE OF CONVERSION
02C7 6584              ADC     STORHI ; ADD TO SUM
02C9 8581              STA     RESLT+1 ;  SAVE MS BYTE
02CB A582              LDA     RESLT+2 ;GET SIGN
02CD 6900              ADC     #00    ; ADD CARRY BIT, IF ANY
02CF 8582              STA     RESLT+2 ;   AND SAVE
02D1 4CE802            JMP     LOOPCNT ;JUMP TO TEST FOR 9 CONVERSIONS
02D4 38       SUBTR    SEC            ;SET CARRY FOR SUBTRACTION
02D5 A580              LDA     RESLT  ;  POLARITY OF THIS CONVERSION
02D7 ED01A8            SBC     IOPT+1 ;    IS NEGATIVE, SO DO A
02DA 8580              STA     RESLT  ;      DOUBLE-PRECISION
02DC A581              LDA     RESLT+1 ;       SUBTRACTION
02DE E584              SBC     STORHI ;
02E0 8581              STA     RESLT+1
02E2 A582              LDA     RESLT+2 ;
02E4 E900              SBC     #00    ;
02E6 8582              STA     RESLT+2 ;
02E8 C683     LOOPCNT  DEC     STORX  ;HAVE WE DONE 9 CONVERSIONS?
02EA F001              BEQ     DIVID  ;  YES, SO NOW DIVIDE BY 9
02EC 40                RTI            ;  NO, SO RETURN
02ED                   PAGE
```

Figure 7: This assembly-language listing *for the µP A/D-converter system in* **Figure 6** *provides for 9-sample numerical integration, thereby eliminating normal-mode noise at frequencies that are multiples of 10 Hz.*

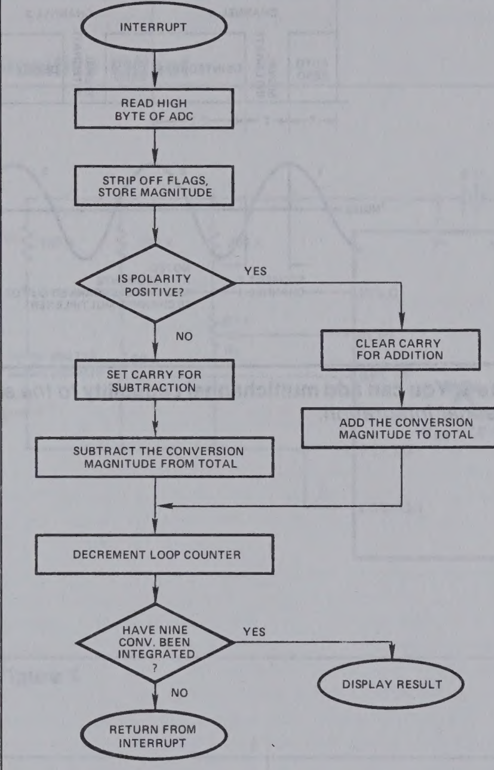

INTERRUPT
READ HIGH BYTE OF ADC
STRIP OFF FLAGS, STORE MAGNITUDE
IS POLARITY POSITIVE?
YES
NO
CLEAR CARRY FOR ADDITION
SET CARRY FOR SUBTRACTION
ADD THE CONVERSION MAGNITUDE TO TOTAL
SUBTRACT THE CONVERSION MAGNITUDE FROM TOTAL
DECREMENT LOOP COUNTER
HAVE NINE CONV. BEEN INTEGRATED ?
YES
NO
DISPLAY RESULT
RETURN FROM INTERRUPT

Figure 8: This flowchart for Figure 7's assembly-language routine *summarizes the code necessary to control the* **Figure 6** *evaluation circuit.*

Adding Channels

By using analog multiplexers, you can take advantage of these speed-improvement techniques in multi-channel systems. Solving the equation given earlier for X and using X to determine the scan length (or number of channels), you keep the noise-segment alignment in proper phase. This segmented approach (for a 16-channel system that requires the summation of three conversions) is shown in Figure 9. The scan length is found by dividing the number of available channels by X, taking the integer value, and then multiplying it by X and adding 1. Table 2 shows the relationship between the number of samples summed and the number of channels scanned for a 16-channel multiplexer.

A data-acquisition system using a 16-channel multiplexer could use a TSC7109 running at 25 conversions/sec to reject all harmonics of 20 Hz (including, of course, 60 Hz), with a 5-sample average taken in the microprocessor. The system would still respond to large signal deviations in a single conversion.

The change from analog signal integration of noise to hybrid analog/numerical integration entails some tradeoffs. The quantization error, for example, is always present; it can lead to a significant reduction in normal-mode rejection if the noise period is carved into too many segments. In addition, timing instability can create other error sources. For maximum stability, you must control the A/D converter's timing with a crystal oscillator.

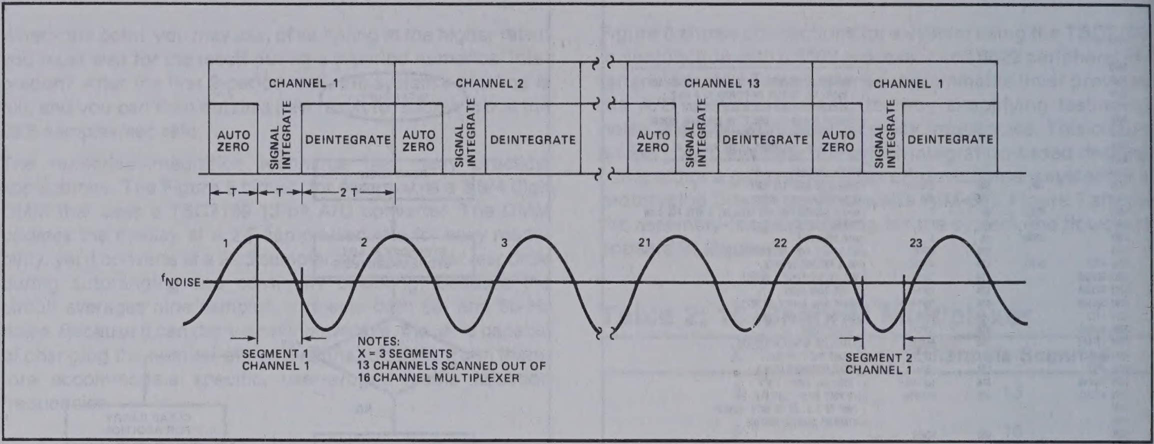

CHANNEL 1
CHANNEL 2
CHANNEL 13
CHANNEL 1
AUTO ZERO
SIGNAL INTEGRATE
DEINTEGRATE
T
T
2 T
1
2
3
21
22
23
f_{NOISE}
SEGMENT 1
CHANNEL 1
NOTES:
X = 3 SEGMENTS
13 CHANNELS SCANNED OUT OF
16 CHANNEL MULTIPLEXER
SEGMENT 2
CHANNEL 1

Figure 9: You can add multichannel capability *to the enhanced-speed A/D-converter designs employing μP-based numerical integration.*

TELEDYNE SEMICONDUCTOR

Application Brief 7
Solve Sensor Offset Problems with the TSC7106
By Wes Freeman

Design Engineers sometimes have to interface our TSC7106 and similar ADCs to "non-ideal" sensors. A very common problem is that the sensor often does not give a "zero" output where the design wants a zero reading.

One example of a "non-ideal" sensor is a diode used as a temperature sensor. The diode typically changes -2 mV per degree Celsius, but the change is from the diode's forward voltage of 600 mV or so. In order for the display to read "000" at 0.0 degrees, an offset must be provided.

The differential inputs of the TSC7106 yield an easy solution to the offset problem. Figure 1 shows a simple thermometer with a diode sensor. Because the diode voltage decreases as temperature increases, IN LO is connected to the diode temperature sensor. The IN HI input is connected to a trimpot which is used to cancel the diode's forward voltage.

The offset problem gets a little more difficult, however, if a sensor requires a negative offset. The easiest way, shown in Figure 2, is to use a TSC9491 reference. This will provide an offset of up to -1.22 V. The only "trick" to this circuit is that Resistor R1 must source enough current for the TSC9491 plus a few extra microamps for the COMMON input.

Figure 2 also demonstrates the utility of the TSC7106 families' differential reference. The effective reference voltage is simply the difference between the REF HI and REF LO inputs. In this way, the same TSC9491 can be used to produce both input offset and reference voltages.

Positive Offset

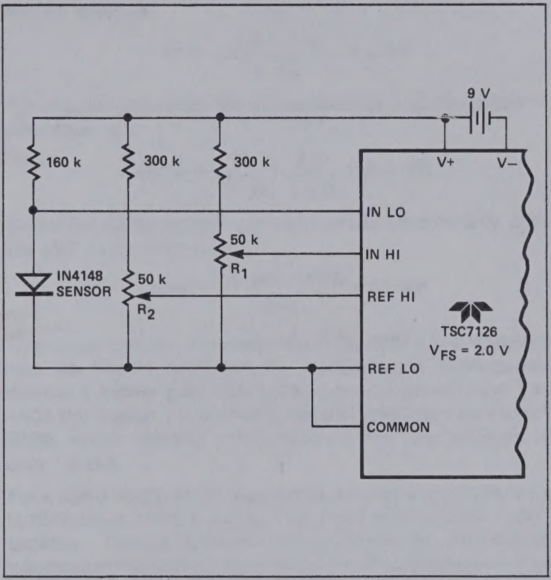

9 V
160 k
300 k
300 k
V+
V–
IN LO
50 k
IN HI
R_1
IN4148
SENSOR
50 k
R_2
REF HI
TSC7126
V_{FS} = 2.0 V
REF LO
COMMON

Figure 1

Negative Offset

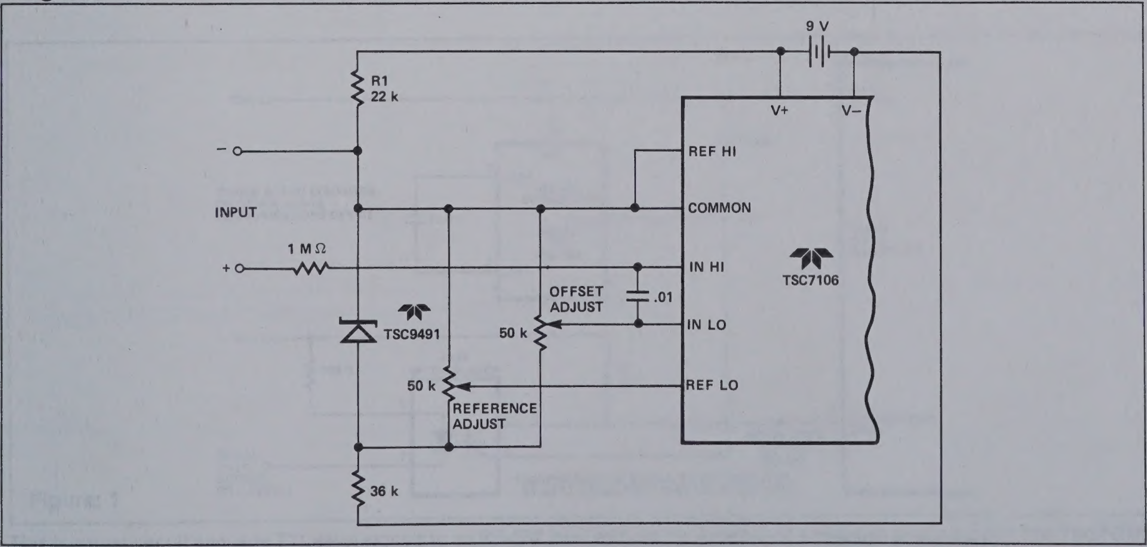

9 V
R1
22 k
V+
V–
–
REF HI
INPUT
COMMON
1 MΩ
+
IN HI
TSC7106
OFFSET
ADJUST
.01
TSC9491
50 k
IN LO
50 k
REF LO
REFERENCE
ADJUST
36 k

Figure 2

Notes

TELEDYNE SEMICONDUCTOR

Application Brief 8
TSC7660 Powers RS-232 Data Loop
• Low Cost Adapter
By Wes Freeman

The introduction of single-voltage EPROMS and dynamic RAMs has permitted designers to produce complete digital systems powered by a single 5 volt supply. One area which has not yielded to single-supply operation, however, is the RS-232 interface. If a system must communicate with an RS-232 serial device, such as a printer or another computer, a separate power supply is required.

The circuit in Figure 1 provides an RS-232 driver without requiring a second power supply. Originally built for downloading files from an IBM PC to an AIM-65, the circuit is applicable to a wide variety of single-board computers as well as single chip microprocessors such as Intel's 8051. In 100-piece quantities the component cost is less than $3.00, and pc board space is only a little more than is occupied by a 20-pin socket.

Understanding the circuit's operation is easy. U1 is the CMOS TSC7660 DC-to-DC converter. It contains an oscillator and matrix of switches which convert the +5 volt supply to -5 volts. The optoisolator converts the TTL-level input current into a voltage which swings between the plus and minus supply rails, producing RS-232 compatible output levels.

Resistor R1 determines the RS-232 output voltage swing. R1's value is determined by the input specifications of the receiving device, current transfer ratio of the optoisolator, and the driving circuit's output current capability.

The RS-232 input voltage spec is ±3 volts. The minimum input resistance of the MC1489, a typical RS-232 receiver, is about 3 kΩ. Therefore, 1 mA of current must be supplied, and R1 must be:

$$R_1 = \frac{5\text{ V} - 3\text{ V}}{1\text{ mA}} = 2\text{ k}\Omega$$

For reliable operation the optoisolator should be biased to saturation, so:

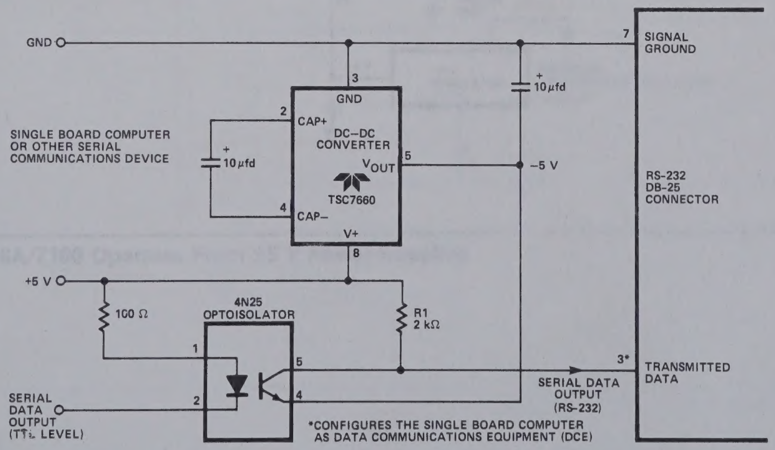
$$I_{OPTO} = \frac{10\text{ V}}{2\text{ k}\Omega} + \frac{5\text{ V}}{3\text{ k}\Omega} = 6.6\text{ mA}$$

Since the optoisolator's current transfer ratio is only 20%, the LED current must be:

$$I_{LED} = \frac{6.6\text{ mA} * 100\%}{20\%} = 33\text{ mA}$$

This value is within the capability of the 7438 driver supplied with the AIM-65 computer. For interfacing to lower-power devices a higher gain optoisolator can be substituted. The 4N33 Darlington, for example, has a current transfer ratio of 500%, which reduces input drive current requirements to only 1.3 mA.

For a cable length of six feet, the circuit operates properly up to 9600 baud. Unfortunately, high baud rates are not always useable. This is because many computer prototyping boards seem to have software serial-communications routines which are designed for 110 baud teleprinters. These routines do not make use of the handshaking signals which RS-232 provides. Unless the serial communications routines are rewritten, lower baud rates may be required for proper operation.



*CONFIGURES THE SINGLE BOARD COMPUTER AS DATA COMMUNICATIONS EQUIPMENT (DCE)

Figure: 1

This low cost circuit converts TTL-level signals to an RS-232 level without the expense of a negative power supply. The TSC7660's -5 V output permits the optoisolator to swing to RS-232 levels at up to 9600 baud.

Notes

TELEDYNE SEMICONDUCTOR

Application Brief 9
±5 V Power Supply Operation with TSC7106A/TSC7107A

By Dave Gillooly

The TSC7106A/7106 3 1/2 digit analog-to-digitial converters with liquid crystal display drive can be powered from ±5 V power supplies easily. Low cost voltage regulators such as the LM7805 (+5 V) and LM7905 (-5 V) power the TSC7106A/7106 in Figure 1. Analog common, internally referenced to 3 V below the positive supply potential, is used to supply the converter reference.

If only +5 V is available the low cost TSC7660 DC to DC converter easily generates the -5 V supply as in Figure 2. A TSC7107A/7107 LED display converter can also be powered by a TSC7660.

An external voltage reference replaces the internal reference in Figure 3. Chip temperature variations caused by changing LED display drive current can cause full-scale drift if the internal reference does not have a low temperature coefficient. Input signal magnitude and the corresponding seven segment display code determine how many LED segment drivers are active. The TSC7107A features an improved low temperature drift internal voltage reference.

The TSC7107A is directly pin compatible with the first generation ICL7107 device and lowers temperature induced full-scale drift (See the TSC7107A Data Sheet Also).

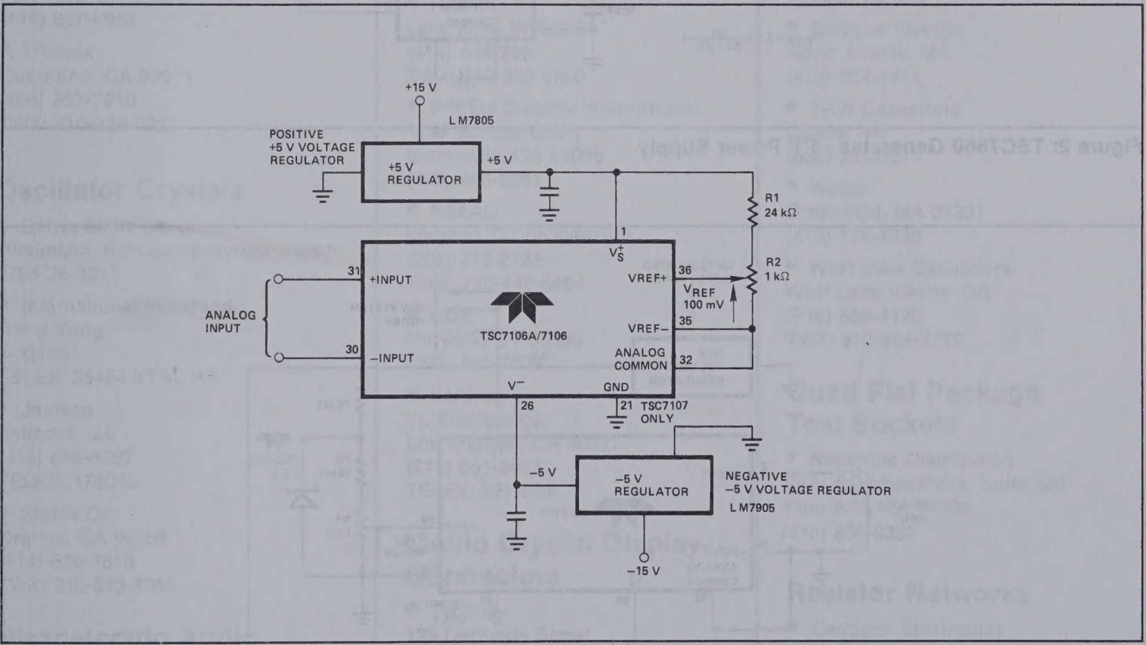

+15 V
LM7805
POSITIVE +5 V VOLTAGE REGULATOR
+5 V REGULATOR
+5 V
R1 24 kΩ
1
V_S^+
31
+INPUT
VREF+
36
R2 1 kΩ
V_{REF} 100 mV
ANALOG INPUT
TSC7106A/7106
VREF−
35
30
−INPUT
ANALOG COMMON
32
V⁻
GND
26
21 TSC7107 ONLY
−5 V
−5 V REGULATOR
NEGATIVE −5 V VOLTAGE REGULATOR
LM7905
−15 V

Figure 1: TSC7106A/7106 Operates From ±5 V Power Supplies

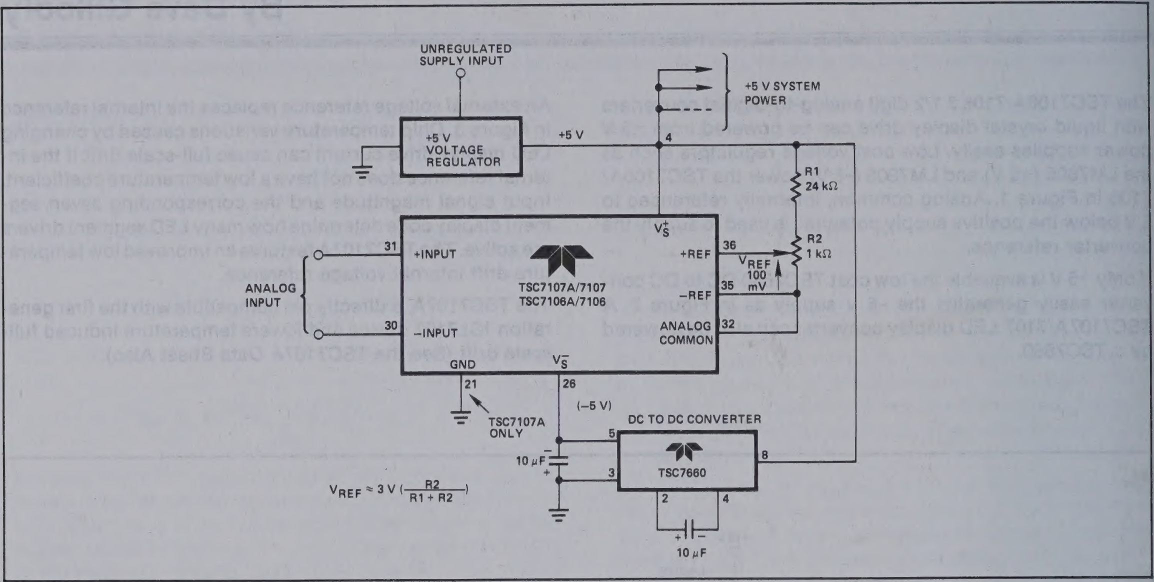

UNREGULATED SUPPLY INPUT
+5 V VOLTAGE REGULATOR
+5 V
+5 V SYSTEM POWER
4
R1 24 kΩ
R2 1 kΩ
V_S^+
31
+INPUT
36
+REF
V_{REF} 100 mV
ANALOG INPUT
TSC7107A/7107
TSC7106A/7106
35
−REF
30
−INPUT
ANALOG COMMON
32
GND
V_S^-
21
26
TSC7107A ONLY
(−5 V)
DC TO DC CONVERTER
5
10 µF
3
TSC7660
8
2
4
10 µF
$V_{REF} \approx 3\ V\ (\frac{R2}{R1 + R2})$

Figure 2: TSC7660 Generates −5 V Power Supply

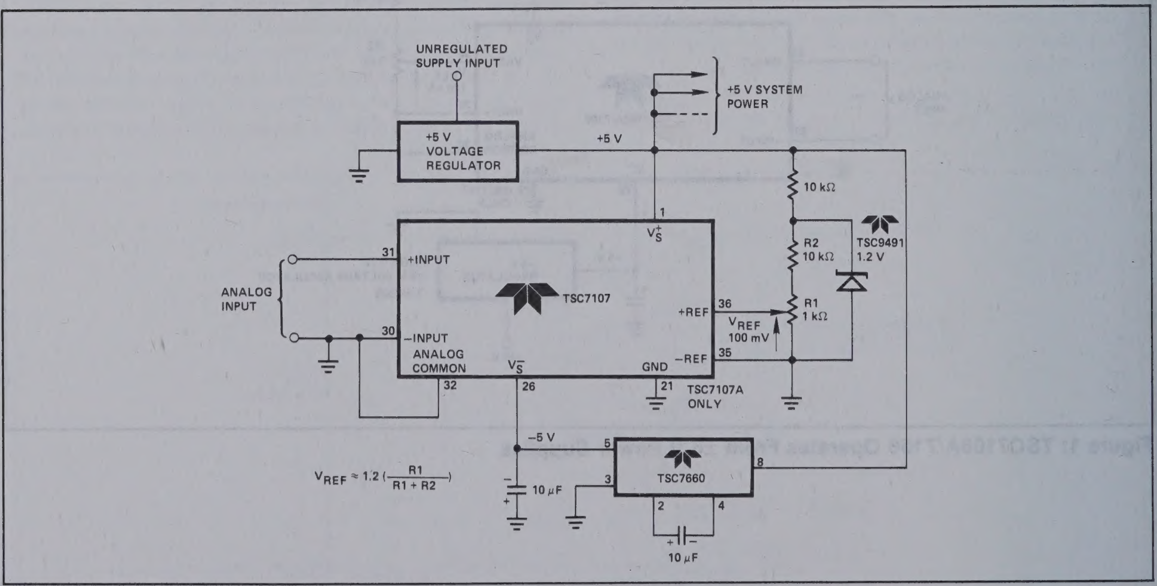

UNREGULATED SUPPLY INPUT
+5 V VOLTAGE REGULATOR
+5 V
+5 V SYSTEM POWER
10 kΩ
1
V_S^+
TSC9491 1.2 V
R2 10 kΩ
31
+INPUT
ANALOG INPUT
TSC7107
36
+REF
R1 1 kΩ
V_{REF} 100 mV
30
−INPUT
ANALOG COMMON
V_S^-
GND
−REF
35
32
26
21
TSC7107A ONLY
−5 V
5
TSC7660
8
3
10 µF
2
4
10 µF
$V_{REF} \approx 1.2\ (\frac{R1}{R1 + R2})$

Figure 3: External Reference in ±5 V System

TELEDYNE SEMICONDUCTOR

Application Brief 10
Vendors for Support Components

Many Teledyne Semiconductor products use displays, crystals and capacitors. A partial list of potential suppliers for components is given below. Although not exhaustive, the list should help development. Additional vendors can be found in the U.S. Industrial Directory, Electronic Design's Gold Book, and Who's Who in Electronics.

LED Displays

- AND
  Burlingame, CA 94010
  (415) 347-9916
  TWX: 910-374-2353
- General Instrument
  Opto Electronics Division
  Palo Alto, CA 94304
  (415) 493-0400
- Hewlett Packard
  Opto Electronics
  640 Page Mill Road
  Palo Alto, CA 94304
  (415) 857-5948
- Litronix
  Cupertino, CA 95014
  (408) 257-7910
  TWX: 910-338-0022

Oscillator Crystals

- Daiwa Sinku Corp.
  Hirakacho, Kakogowa Hyogo, Japan
  0794-26-3211
- International Piezo Ltd.
  Hong Kong
  3-351051
  TELEX: 35454 XTAL HX
- Jameco
  Belmont, CA
  (415) 592-8097
  TELEX: 176043
- Statek Co.
  Orange, CA 92668
  (714) 639-7810
  TWX: 910-593-1355

Piezoelectric Audio Transducers

- Murata Erie
  Marietta, GA 30067
  (404) 952-9777
  TWX: 810-766-1531
- Piezoelectric Products
  Gulton Industries
  Metuchen, NJ 08840
  (201) 548-2800

Liquid Crystal Displays

- Amperex
  Slatersville, RI 02876
  (401) 762-3800
  TWX: 710-382-6332
- Crystaloid
  Hudson, OH 44236
  (216) 655-2429
- Epson
  Torrance, CA 90505
  (213) 534-0360
  TELEX: 182412
- Hamlin
  Lake Mills, WI 53551
  (414) 648-2361
  TWX: 910-260-3740
- Printed Circuits International
  1145 Sonora Court
  Sunnyvale, CA 94086
  (408) 980-0591
- REFAC
  Winsted, CT 06098-0809
  (203) 379-2731
  TWX: 710-449-6464
- UCE
  Norwalk, CT 06855
  (203) 838-7509
- Varitronix
  VL Electronics
  Los Angeles, CA 90027
  (213) 661-8883
  TELEX: 821-554

Liquid Crystal Display Connectors

- Tecknit
  129 Dermody Street
  Cranford, NJ 07016
  (201) 272-5500
  TWX: 710-996-5951

Polypropylene Capacitors

- International Components
  Melville, NY 11747
  (516) 293-1500
  TELEX: 143130
- S&EI Manufacturing
  Northridge, CA 91324
  (213) 349-4111
  TWX: 910-493-1252
- Seacor
  Westwood, NJ
  (201) 666-5600
  TELEX: 135354
- Sprague Electric
  North Adams, MA
  (413) 664-4411
- TRW Capacitors
  Ogalla, NE
  (308) 284-3611
- Wesco
  Greenfield, MA 01301
  (413) 774-4358
- West Lake Capacitors
  West Lake Village, CA
  (818) 889-4120
  TWX: 910-494-4779

Quad Flat Package Test Sockets

- Nepenthe Distribution
  2471 East Bayshore, Suite 520
  Palo Alto, CA 94303
  (415) 856-9332

Resistor Networks

- Caddock Electronics
  1717 Chicago Avenue
  Riverside, CA 92507
  (714) 788-1700
  TWX: 910-332-6108

This listing does not represent an endorsement of manufacturer's product or a guarantee of suitablity. Contact the supplier for specific product information.

Notes

SECTION 16

Glossary of Terms and Abbreviations

Brief Glossary For TSC Products

Analog-to-Digital Converter

Electronic device that converts Analog (continuous) information into a Digital word (number). Analog quantities can be temperature, pressure, weight, chemical concentration, noise level, and fluid level.

The Digital result can be a number in binary, decimal, or binary-coded-decimal (BCD).

Auto-Zero

A self-correcting system that insures a Zero output of the ADC for a Zero input.

Binary

Number system with only two values — 0 or 1 — in each numeric position. This is the number system used in computer systems.

Binary-Coded-Decimal (BCD)

A number system whereby binary numbers are grouped in sets of four to represent decimal (Ten system) numbers. This system is shown below.

BCD #	Decimal #
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9

This number system is useful for some A/D converters intended to be used in displaying the output as decimal numbers.

Bit

A single binary number unit, 0 or 1. An 8-bit number could appear as:

10011110 (158 in decimal)
or
01000011 (67 in decimal)

or any other combination
from 00000000
to
11111111

Code

Output format of A/D converter. Usually binary, BCD, or sign-magnitude binary.

Digit

A single decimal number unit that can range in value from 0 to 9.

Thus, a 3 1/2 digit A/D converter goes from 0000 to 1999;

a 4 1/2 digit A/C converter can provide outputs from 00000 to 19999;

and a 3 digit converter can provide outputs from 000 to 999.

Note that the "1/2 digit" merely doubles the output range by adding a Most Significant Bit to the output.

Display ADC

An A/D converter normally designed to convert and display the numeric value representing the analog signal. Display ADC's may have the Display Driver built in (as the TSC7106, 7107, 7116, 7117 have), or may provide multiplexed BCD for use by external drivers (the TSC14433, TSC7135, and TSC8750 do this).

Least-Significant-Bit (or Digit)

The lowest number position

for Decimal 1287
↑
Least Significant Digit (LSD)

for Binary 10010011
↑
Least Significant Bit (LSB)

Multiplexed

Signals sharing a common connection but separated in time are said to be multiplexed. Multiplexed BCD is characterized by the 4 BCD signal paths in which the appropriate digits are separated in time.

Resolution

Number of output states offered by the A/D converter. For a binary ADC, the resolution is 2^n; where n equals the number of bits,

thus:
$2^8 = 256$
$2^{10} = 1024$
$2^{12} = 4096$
$2^{14} = 16384$
$2^{16} = 65536$

For decimal and BCD ADCs, the resolution equals 10^n; where n is the number of digits (see "Digit" definition).

Sign

An additional output in some ADCs that are capable of measuring both + and – voltage. The sign bit identifies this polarity (typically, "1" for + and "0" for –). The coding format resulting is called Sign-Magnitude Code.

Notes

Glossary of Data Conversion Terms

Absolute Accuracy
The worst-case input to output error of a data converter referred to the NBS standard volt.

Accuracy
The conformance of a measured value with its true value; the maximum error of a device such as a data converter from the true value. See *relative accuracy* and *absolute accuracy*.

A/D Converter
Analog-to-digital converter. A circuit which converts an analog (continuous) voltage or current into an output digital code.

Auto-Zero
A stabilization circuit which serves an amplifier or A/D converter input offset to zero during a portion of its operating cycle.

Bandgap Reference
A voltage reference circuit which is based on the principle of the predictable base-to-emitter voltage of a transistor to generate a constant voltage equal to the extrapolated bandgap voltage of silicon (≈1.22 V).

Binary Code
A positive weighted code in which a number is represented by

$$N = a_0 2^0 + a_1 2^1 + a_2 2^2 + a_3 2^3 + \ldots + a_n 2^n$$

where each coefficient "a" has a value of zero or one. Data converters use this code in its fractional form where:

$$N = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \ldots a_n 2^{-n}$$

and N has a fractional value between zero and one.

Binary Coded Decimal (BCD)
A binary code used to represent decimal numbers in which each digit from 0 to 9 is represented by four bits weighted 8-4-2-1. Only 10 of the 16 possible states are used.

Bipolar Mode
For a data converter, when the analog signal range includes both positive and negative values.

Busy Output
See Status Output

Charge Balancing A/D Converter
An analog-to-digital conversion technique which employs an operational integrator circuit within a pulse generating feedback loop. Current pulses from the feedback loop are precisely balanced against the analog input by the integrator, and the resulting pulses are counted for a fixed period of time to produce an output digital word. This technique is also called *quantized-feedback.*

Clock
A circuit in an A/D converter that generates timing pulses which synchronize the operation of the converter.

Common-Mode Rejection Ratio
For an amplifier, the ratio of differential voltage gain to common-mode voltage gain, generally expressed in dB.

$$\text{CMRR} = 20 \log_{10} \frac{A_D}{A_{CM}}$$

where A_D is differential voltage gain and A_{CM} is common mode voltage gain.

Conversion Time
The time required for an A/D converter to complete a single conversion to specified resolution and linearity for a full-scale analog input change.

Differential Linearity Error
The maximum deviation of any quantum (LSB change) in the transfer function of a data converter from its ideal size of $FSR/2^n$.

Dual Slope A/D Converter
An indirect method of A/D conversion whereby an analog voltage is converted into a time period by an integrator and reference and then measured by a clock and counter. The method is relatively slow but capable of high accuracy.

End of Conversion
See Status Output

Frequency-To-Voltage (F/V) Converter
A device which converts an input pulse rate into an output analog voltage.

Full-Scale Range (FSR)
The difference between maximum and minimum analog values for an A/D converter input or D/A converter output.

Integral Linearity Error
The maximum deviation of a data converter transfer function from the ideal straight line with offset and gain errors zeroed. It is generally expressed in LSB's or in percent of FSR.

Integrating A/D Converter
One of several types of A/D conversion techniques whereby the analog input is integrated with time. This includes dual slope, triple slope, and charge balancing type A/D converters.

Least Significant Bit (LSB)
The rightmost bit in a data converter code. The analog size of the LSB can be found from the converter resolution:

$$\text{LSB Size} = \frac{FSR}{2^n}$$

where FSR is full-scale range and n is the resolution in bits.

Linearity Error
See Integral Linearity Error and *Differential Linearity Error.*

Missing code
In an A/D converter, the characteristic whereby not all output codes are present in the transfer function of the converter. This is caused by a non monotonic D/A converter inside the A/D.

Monotonicity
For a D/A converter, the characteristic of the transfer function whereby an increasing input code produces a continuously increasing analog output. *Nonmonotonicity* may occur if the converter differential linearity error exceeds ±1 LSB.

Most Significant Bit (MSB)
The leftmost bit in a data converter code. It has the largest weight, equal to one half of full-scale range.

Multiplying D/A Converter

A type of digital-to-analog converter in which the reference voltage can be varied over a wide range to produce an analog output which is the product of the input code and input reference voltage. Multiplication can be accomplished in one, two, or four algebraic quadrants.

Noise Rejection

The amount of suppression of normal mode analog input noise of an A/D converter or other circuit, generally expressed in dB. Good noise rejection is a characteristic of integrating type A/D converters.

Offset Drift

The change with temperature of analog zero for a data converter operating in the bipolar mode. It is generally expressed in ppm/°C of FSR.

Parallel Type A/D Converter

An ultra-fast method of A/D conversion which uses an array of $2^n - 1$ comparators to directly implement a quantizer, where n is the resolution in bits. The quantizer is followed by a decoder circuit which converts the comparator outputs into binary code.

Power Supply Sensitivity

The output change in a data converter caused by a change in power supply voltage. Power supply sensitivity is generally specified in %/V or in %/% supply change.

Ratiometric A/D Converter

An analog-to-digital converter which uses a variable reference to measure the ratio of the input voltage to the difference.

Relative Accuracy

The worst case input to output error of a data converter, as a percent of full-scale, referred to the converter reference. The error consists of offset, gain, and linearity components.

Resolution

The smallest change that can be distinguished by an A/D converter or produced by a D/A converter. Resolution may be stated in percent of full-scale, but is commonly expressed as the number of bits n where the converter has 2^n possible states.

Status Output

The logic output of an A/D converter which indicates whether the device is in the process of making a conversion or the conversion has been completed and output data is ready. Also called *busy output* or *end of conversion* output.

Temperature Coefficient

The change in analog magnitude with temperature, expressed in ppm/°C.

Three-State Output

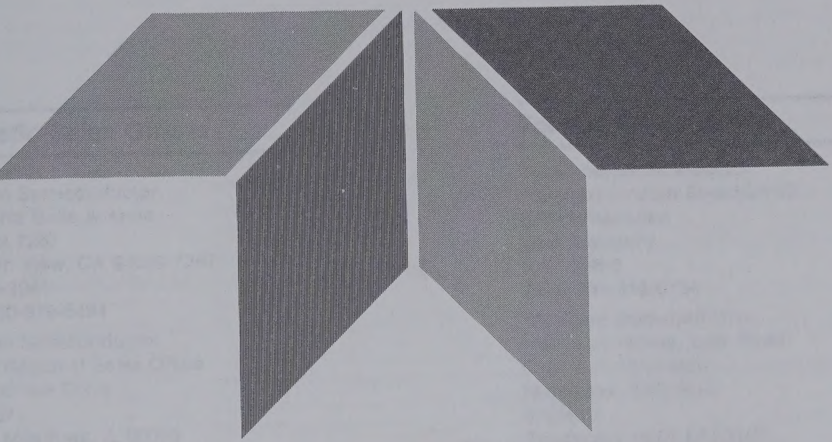
A type of a/D converter output used to connect to a data bus. The three output states are logic 1, logic 0, and off. An *enable* control turns the output on or off.

Voltage-To-Frequency (V/F) Converter

A device which converts an analog voltage into a train of digital pulses with frequency proportional to the input voltage.

Zero Drift

The change with temperature of analog zero for a data converter operating in the unipolar mode. It is generally expressed in μV/°C.



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TLX: 17825 SENIS AR

Australia

Promark Electronics Pty. Ltd.
Suite 102, 6-8 Clarke Street
Crows Nest, NSW 2065
Australia
Telephone: 439-6571 or 439-6965
TLX: 20474

Belgium

Microtron PVBA/SPRL
Tremelobaan 131
B-2850 Keerbergen
Telephone: 016-534186
TLX: 22606

Brazil

Hitech Comerciale Industrial Ltd.
Av. Eng. Luiz Carlos Berrini, 801
Conjunto 111/121
Brooklin
Telephone: (011) 533-9566
TLX: 391-53288

Denmark

Nordisk Elektronik AS
Tranformervej 17
DK-2730 Herlev
Telephone: 02-842000
TLX: 35200

Finland

Fintronic OY AB
Melkonkatu 24A
SF-00210 Helsinki 21
Telephone: 80-6926022
TLX: 124224

France

Tekelec Airtronic SA
Cité des Bruyères
Rue Carle Vernet
F-92310 Sèvres
Telephone: 01-5347535
TLX: 204552

Germany

Adelco Elektronik GmbH
Boxholmstr. 5
2085 Quickborn
Telephone: 04106-2024
TLX: 2180619

Emtron
Electronic Vertriebs GmbH
Waldstr. 55
6085 Nauheim
Telephone: 06152-6003
TLX: 4191175

Ing. T. Henskes GmbH
Badenstedter Str. 9
3000 Hannover 91
Telephone: 0511-456082
TLX: 923509

Hot Elektronik
Wendelsteinweg 11
Postfach 1261
8028 Taufkirchen — Potzham
Telephone: 089-6121092
TLX: 529528

Metronik GmbH
Kapellenstr. 9
8025 Unterhaching
Telephone: 089-6114063
TLX: 529524

Rein Elektronik GmbH
Lötscher Weg 66
4054 Nettetal 1
Telephone: 02153-733-0
TLX: 854251

Semitron W. Röck GmbH
Im Gut 1
7891 Kussaberg 6
Telephone: 07742-7011
TLX: 7921472

Isreal (Representative)

M.L.R.N. Electronics Ltd.
15, Kineret Street
Bney-Brak
P.O. Box 20168
Tel-Aviv 61200
Israel
Telephone: 03-708174/5
TLX: 342107

Italy

Eledra 3S Spa
Viale Elvezia 18
I-20154 Milano
Telephone: 02-349751
TLX: 332332
314155

Japan

Tomen Electronics Corp.
1-1, Uchisaiwai-Cho 2-Chome
Chiyoda-Ku, Tokyo 100
Telephone: (03) 506-3694
TLX: J-23548

Sil-Walker Inc.
1-1, Shinjuku 5-Chome
Shinjuku-Ku, Tokyo 160
Telephone: (03) 341-3651
TLX: 0232-3398

Korea

Vine-Overseas Trading Corp.
Rm. 308, Korea Electric
Association Bldg.,
11-4, Supyo-Dong, Jung-Ku
Seoul
Telephone:
266-1663/265-9875/269-0832
TLX: K24154

Mexico

Dicopel
Tochtli 368
Fracc Ind. San Antonio
Azcapotzalco C.P. 02760 Mexico D.F.
Telephone: 561-32-11
TLX: 1773780 DICOME

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Netherlands

Alcom Electronics bv
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NL-2908 LJ Capelle a/d IJssel
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TLX: 26160

New Zealand

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22A, Milford Rd., Milford,
Auckland
Telephone: 493-048/029
TLX: NZ21084

South Africa

Fairmont Electronics (Pty) Ltd.
4th Fl., 312 Kent Avenue,
Ferndale
Randburg 2194, South Africa
Telephone: (011) 789-1230/4
TLX: 8-24842

Spain

Amitron S.A.
Avenida Valladolid, 47-A
E-28008 Madrid
Telephone: 01-2479313
TLX: 45550

Sweden

Nordisk Elektronik AB
Huvudstagatan 1
P.O. Box 1409
S-17127 Solna
Telephone: 08-7349770
TLX: 10547

Switzerland

ENA AG
Hermetschloostr. 75
CH-8048 Zurich
Telephone: 01-645757
TLX: 822303

Omni Ray AG
Industriestr. 31
CH-8305 Dietlikon
Telephone: 01-8352111
TLX: 53239

Taiwan

Timkuo Taiwan Ltd.
8F-2, 157 Fu Hsing S. Road
Sec. 2, Taipei
Telephone: (02) 709-2246
TLX: 26206

United Kingdom

Macro Marketing Ltd.
Burnham Lane
Slough, Berks. SL1 6LN
Telephone: 06286-4422
TLX: 847945

Phoenix Electronics
(Airdrie) Ltd.
Western Buildings
Vere Road
Kirkmuirhill
Lanarkshire, Scotland
Telephone: 0555-892393
TLX: 777404

Semicomps Ltd.
Halifax Road
Keighley
West Yorkshire BD21 5HR
Telephone: 0535-65191
TLX: 517343

Semiconductor Supplies
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Dawson House
128/130 Carshalton Road
Sutton, Surrey SM1 4RS
Telephone: 01643-1126
TLX: 946650

Trident Microsystems Ltd.
53 Ormside Way
Holmethorpe Industrial Estate
Redhill, Surrey RH1 2LS
Telephone: 0737-65900
TLX: 8953230

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